Contribution ID: 26 Type: not specified

Data Processing with FPGAs: Parallel Computing on Compact Configurable Logic

Thursday 27 March 2025 11:30 (1 hour)

In particle physics, Field-Programmable Gate Arrays (FPGAs) play an increasing role in acquiring, processing, and filtering data at experiments with high data rates. Today their advanced technology allows for complex processing, rather than just being used as glue logic on the hardware level. The high degree of parallelism, flexibility, and number of IOs in combination with low power consumption and size make them a valid choice for many applications in science and industry.

A drawback is the high complexity of designing efficient and optimized firmware using Hardware Description Languages (HDL). High-Level Synthesis (HLS) approaches, however, gain more and more popularity. They allow for comparatively simple and effective implementation of complex algorithms, for example in real-time image processing or deep learning.

In this lecture, I will discuss how FPGAs operate, their building blocks, properties, advantages, challenges, and general feasibility in an experimental context. I will go through the general process of designing logic on the RTL level with a beginner-friendly code example to provide a more tangible treatment. Recent developments, comparisons to other widely used computing architectures, and exemplary use cases will conclude with a short view of HLS as an alternative approach suitable for software engineers.

Number of lecture hours

1

Number of exercise hours

0 (no exercises)

Attended school

tCSC 2024 (Belgrade)

Author: HINDERBERGER, Peter (Technical University of Munich)

Presenter: HINDERBERGER, Peter (Technical University of Munich)

Track Classification: Computing Architectures for Experiment Online Triggers and Event Filters