

# Automated Tests of the Tileboards for the High Granularity Calorimeter upgrade of the CMS experiment

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# Outline

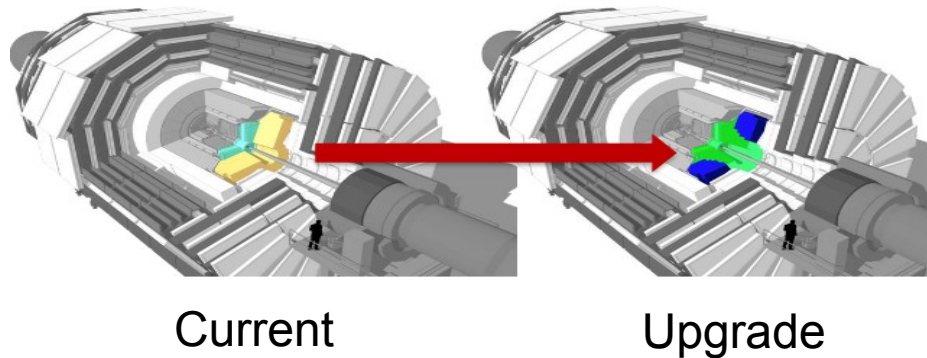
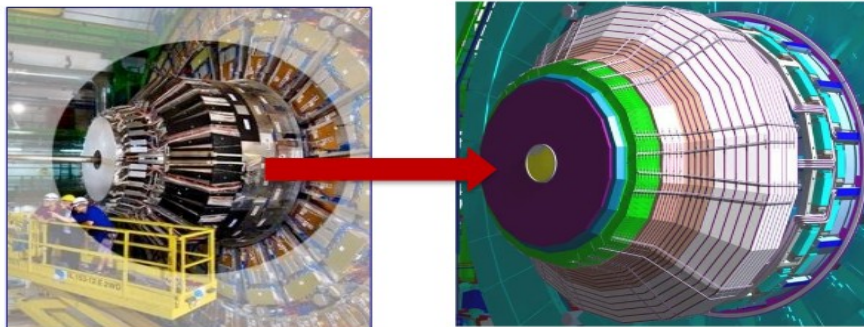
- 1) Introduction
- 2) Tileboard Testing & Initial Configuration
- 3) Electromagnetic Stack Test



# Introduction

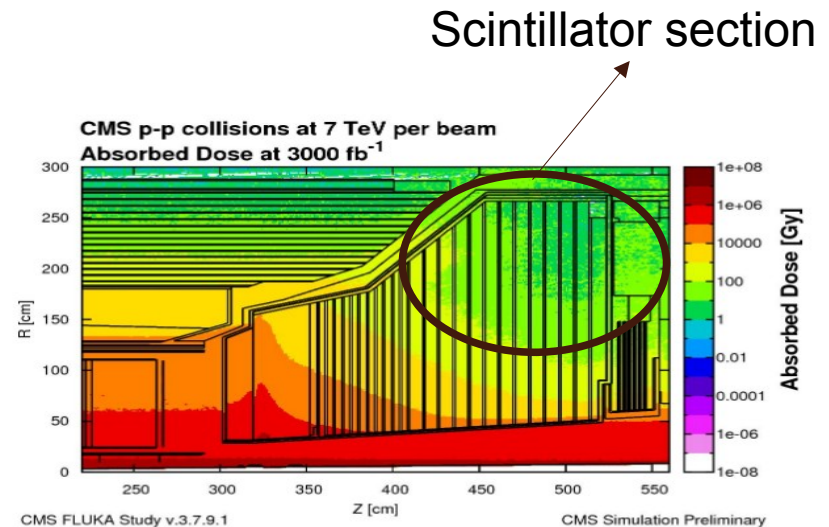
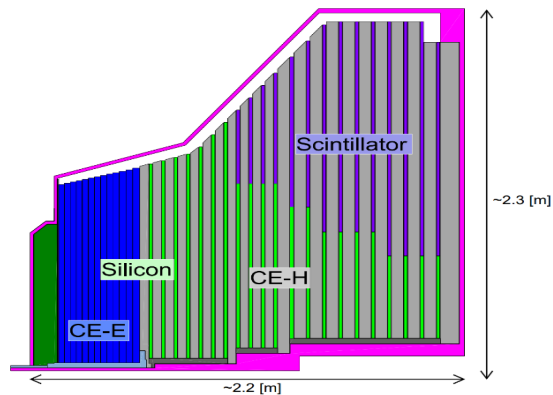
# Introduction

- The High-Luminosity Large Hadron Collider (HL-LHC) => increased luminosity of the current LHC by a factor of  $\sim 10$ .
- Increased pileup and radiation (factor of  $\sim 10$ ). Calls for upgrade of current detectors
- CMS will upgrade its endcap calorimeter with the new High Granularity Calorimeter (HGCAL)
- High granularity key for pileup rejection. HGCAL: 6 million channels
- 2 different technologies are used
  - Silicon
  - Scintillator/SiPM-on-tile



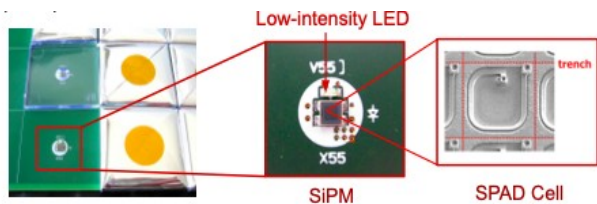
# Why Scintillator technology

- Different integrated radiation at the end of lifetime
- Scintillator technology used towards the back where lower radiation doses are expected
- Allows reduction of overall costs
- 16 scintillator layers, ~4000 boards and ~280,000 channels
- The read-out ASIC is kept as similar as possible between silicon and SiPM-on-Tile technology

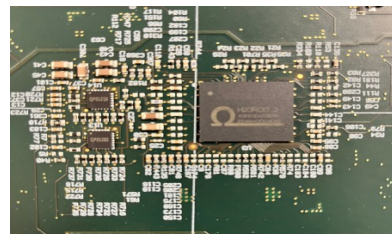


# SiPM-on-Tile Technology

- The scintillator tiles are trapezoidal (considering the geometry of the end-cap region) shaped plastic wrapped in reflective foil.
- Tiles optically linked to silicon photo multipliers (SiPM)
- SiPMs integrated into read-out electronics

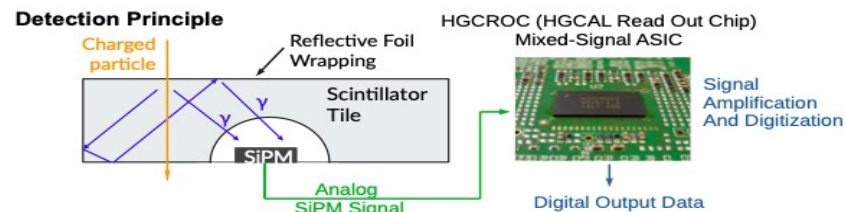


SiPMs consists of thousands of single photon avalanche diodes (SPAD) working in Geiger-Mode



- Signals are processed by the HGCROC chip and sent to backend
- 1 chip = 72 channels

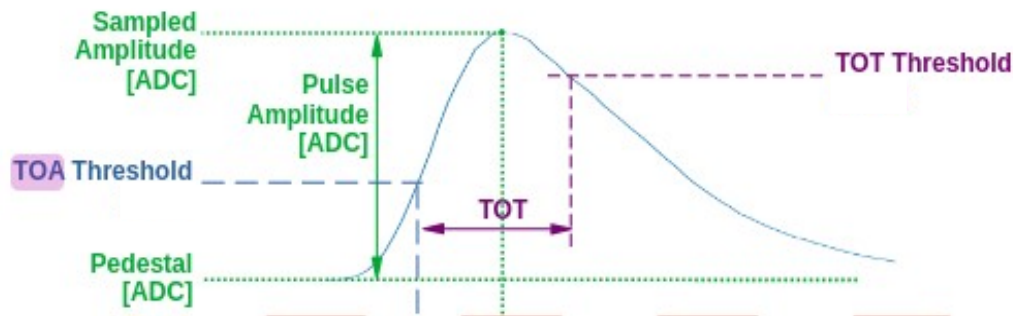
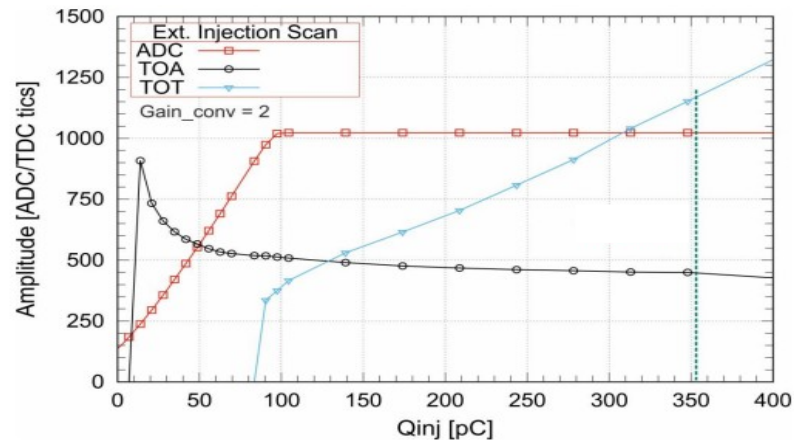
Output => Amplitude and Timing information



# ADC, ToA Threshold and ToT Threshold

- ADC [10 bit] and ToT [12 bit] :  
Amplitude of the signal
- ToA: timing information.
- Need to equalise these parameters for all channels.
- ~300 parameters/board
- Need an automated process.

Private Work

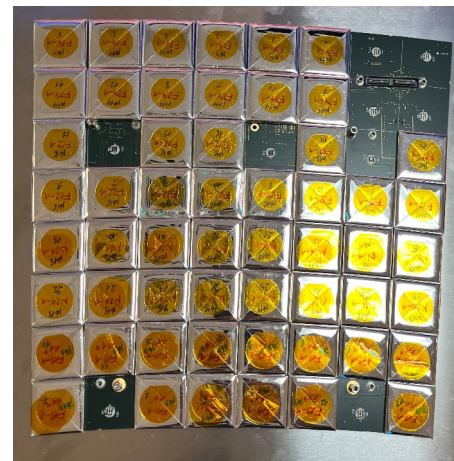


# Small aside: Jargon

- Tileboard = PCB + electronics
- Tilemodule = Tileboard + tiles
- DESY is one of 2 assembly centers for the tileboards and tilemodules, hence a natural center for testing the assembly.



- Tileboard



- Tilemodule

# Production flow



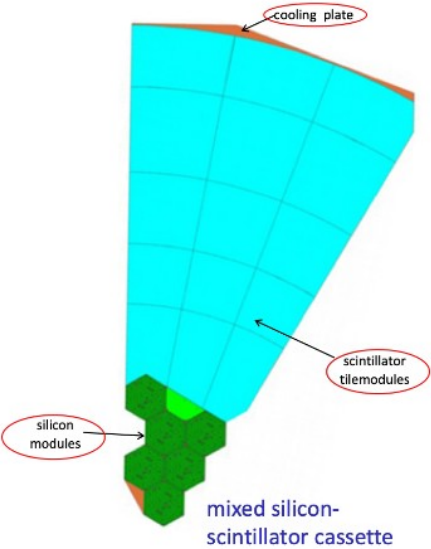
Tileboard testing and initial configuration



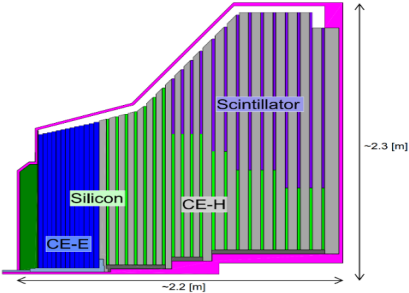
Tilemodule assembly testing



Scintillator tile testing



Cassette Assembly and testing

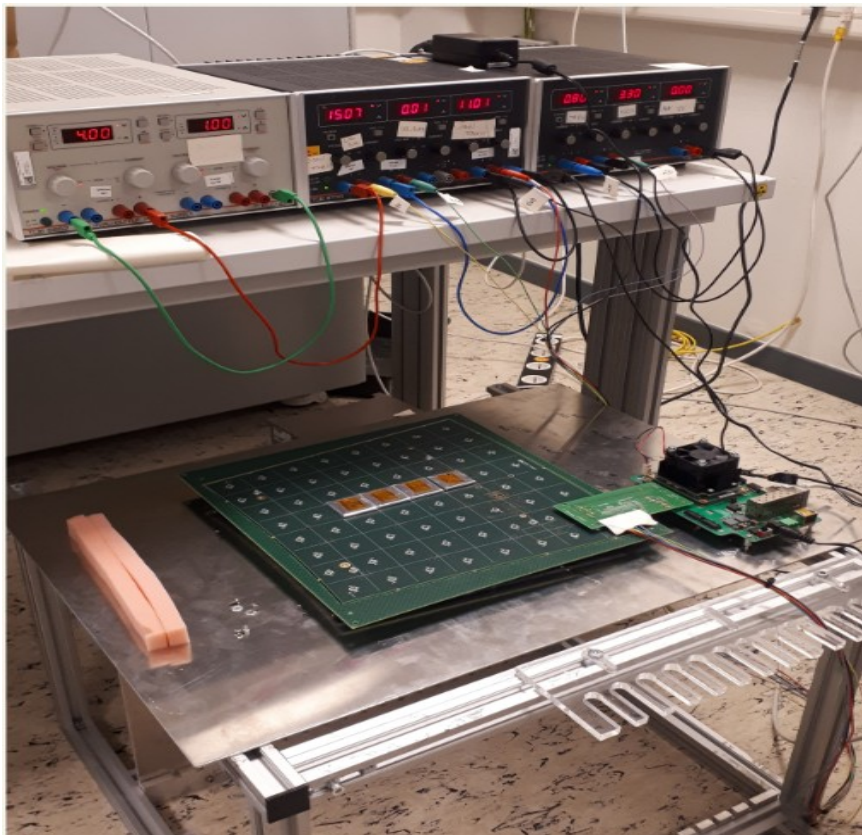


Detector Assembly

# Tileboard Testing & Initial Configuration



# Tileboard Testing & Initial Configuration

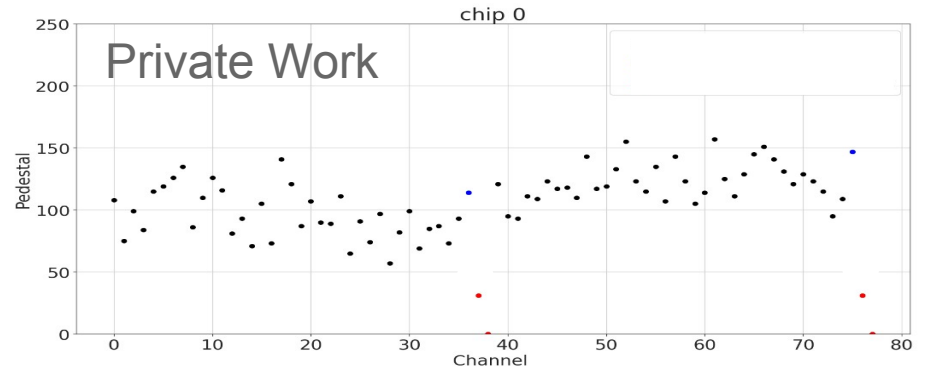


- To get a uniform response of the detector we need to equalise parameters across all channels.
- Also need to get calibration factor between ADC and ToT.
- ~300 parameters/board
- Testing and producing the Initial Configuration also acts as a Quality Control procedure.
- Moving towards production: want to test ~ 8 boards per day => ~ 1 hour per board.

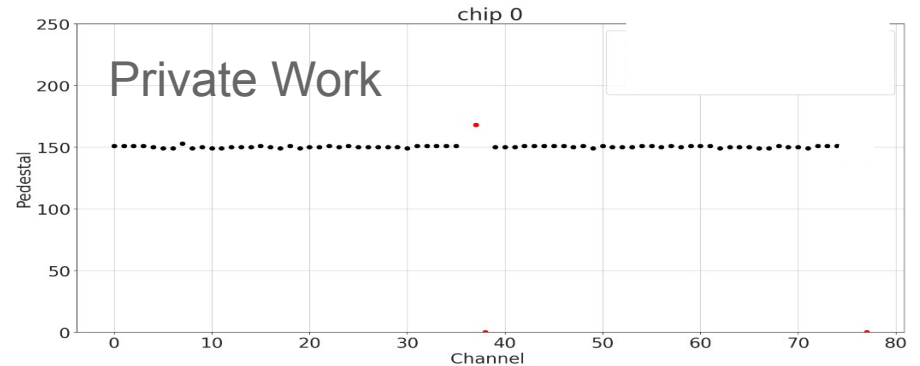
# Example: Pedestal Equalisation

- Two step process:
  - 1) Global adjustment: adjust average value
  - 2) Channel-wise to equalise pedestal

No tuning



Final channel-wise tuning





# Electromagnetic Stack Beam Test



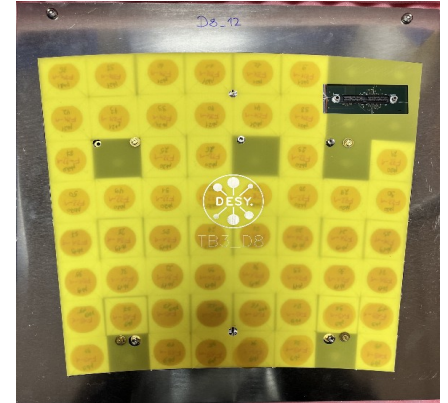
# DESY EM stack beam test Objectives

- First time assembly of an absorber stack with HGICAL's scintillator tile modules
- First time systematically configured 8 boards before beam.
- EM showers are more predictable => more stringent testing
- Main aim:
  - Take different beam energies to probe high-amplitude ToT regime and linearity of stack.
  - Commissioning of the absorber stack
    - Check that the full readout chain works (For more details: talk by Fabian Hummer (Karlsruhe Institute of Technology) May 22, 2025, 10:20)
    - Take data to check that the configuration is reliable for each board.

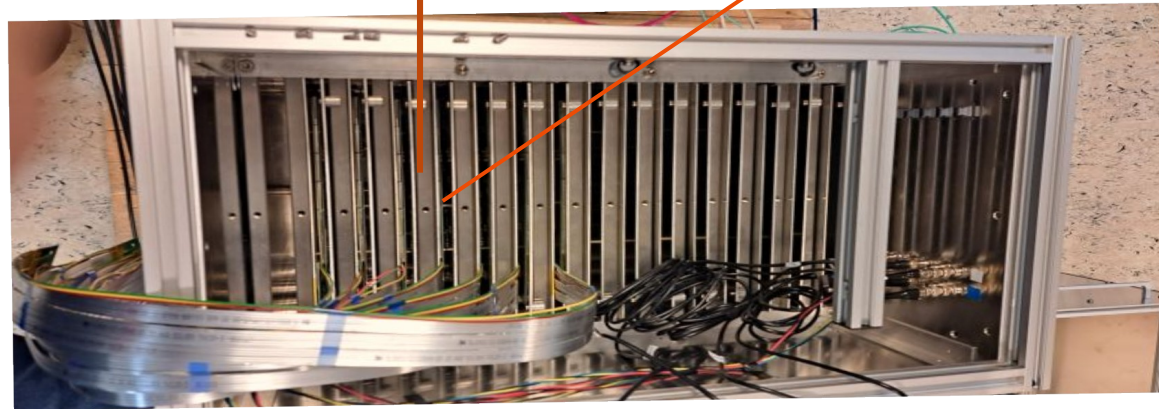
# DESY EM stack beam test

- Stack test at DESY beam facility. (TB 21, March 3 - 10, 2025)
- 8 boards assembled in stack.
- Absorber material = steel with thickness of 1.7 cm/layer
- Much finer sampling since absorber layer is smaller compared to final detector (~12cm).

Example Boards



Absorber



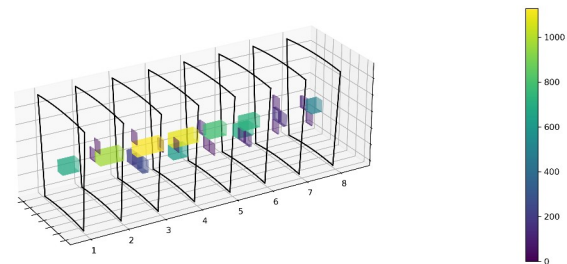
# DESY EM stack beam test



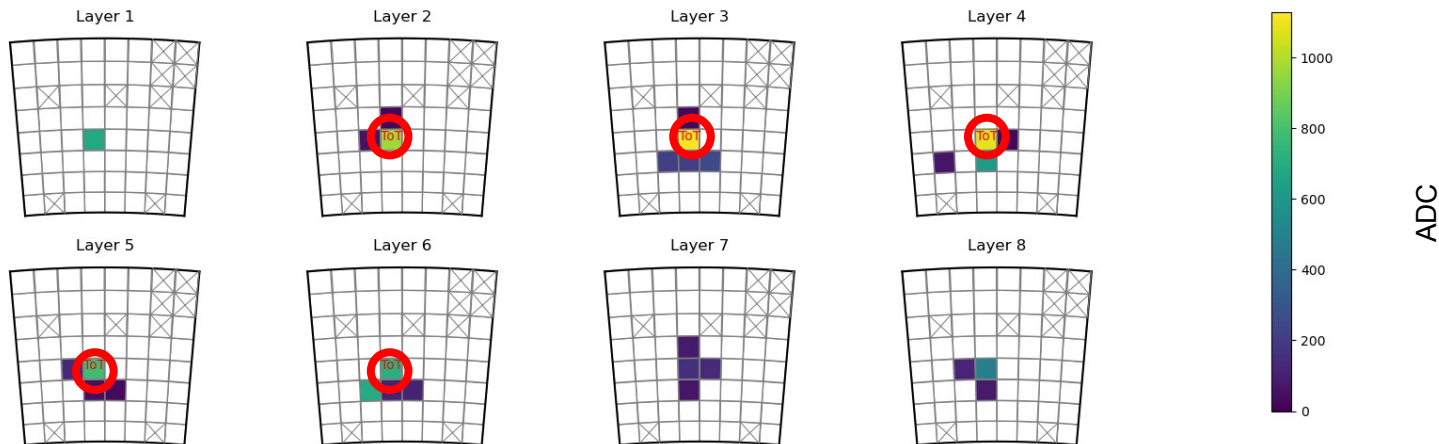
# Timing Alignment Check

5 GeV energy deposition for single event

- Check timing alignment using 5GeV beam.
- Graph of ADC (Signal - pedestal) response to a single event.
- Can see some ToT hits through layers 2-5.



5 GeV energy deposition for single event

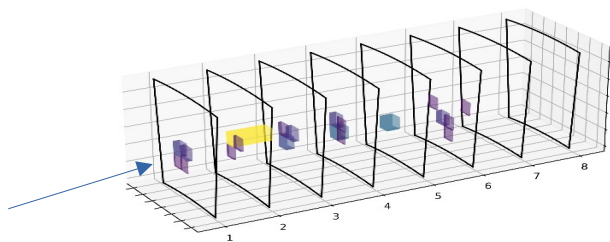


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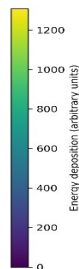
# Energy deposition

- Energy deposition for single event with 2 different beam energies.
- Penetrates deeper in the stack for higher energies.

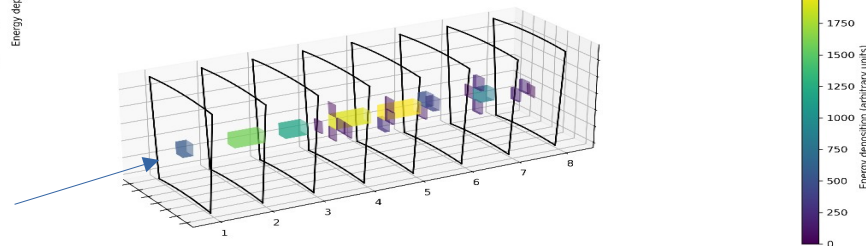
2 GeV energy deposition for single event



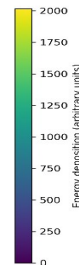
Private Work



5 GeV energy deposition for single event

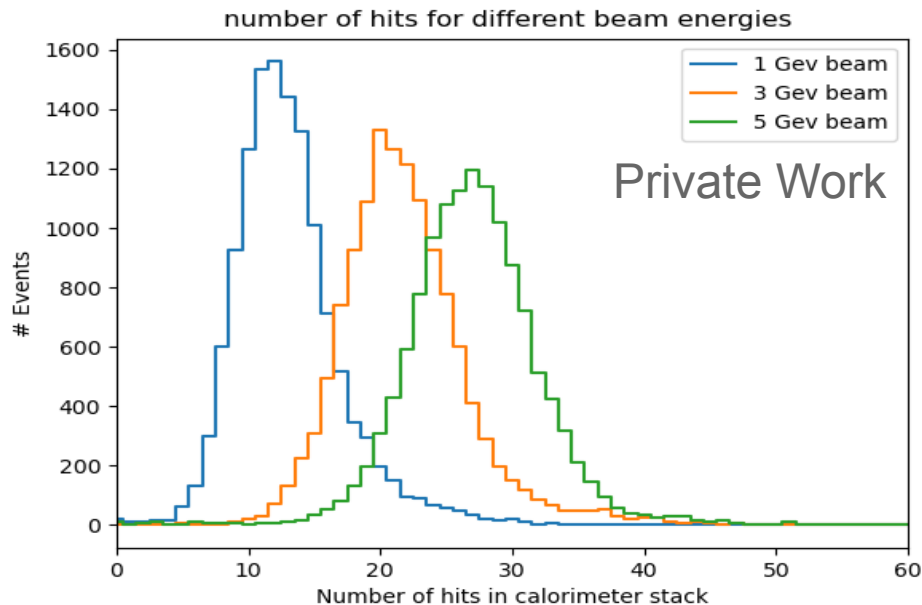


Private Work



# Number of Hits for different Beam Energies

Expectation: higher beam energy => more number of hits



# Summary and Future

# Summary and the Future

- HGICAL has to cope with a large number of objects and of high complexity
- Successful automation of tests and initial configuration of integrated read-out boards
- First results from stack with electron beams to probe high amplitude TOT regime.



# Thank you

## **Contact**

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