

Advancements and future expansions of the Caribou DAQ system

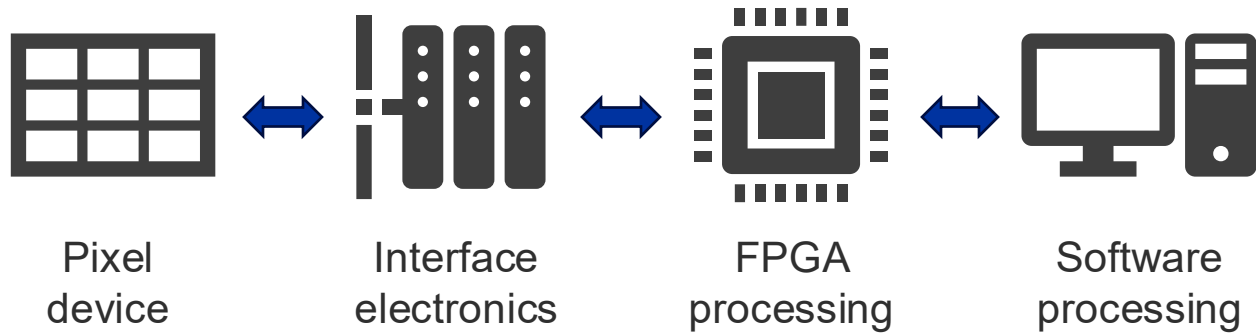
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13th Beam Telescopes & Test Beams Workshop – 20 May 2025

Introduction & System Overview

A particular solution to a particular need

Most silicon pixel detectors share the same power, control and readout concepts
(voltage/current supply, high speed data, communication protocols)

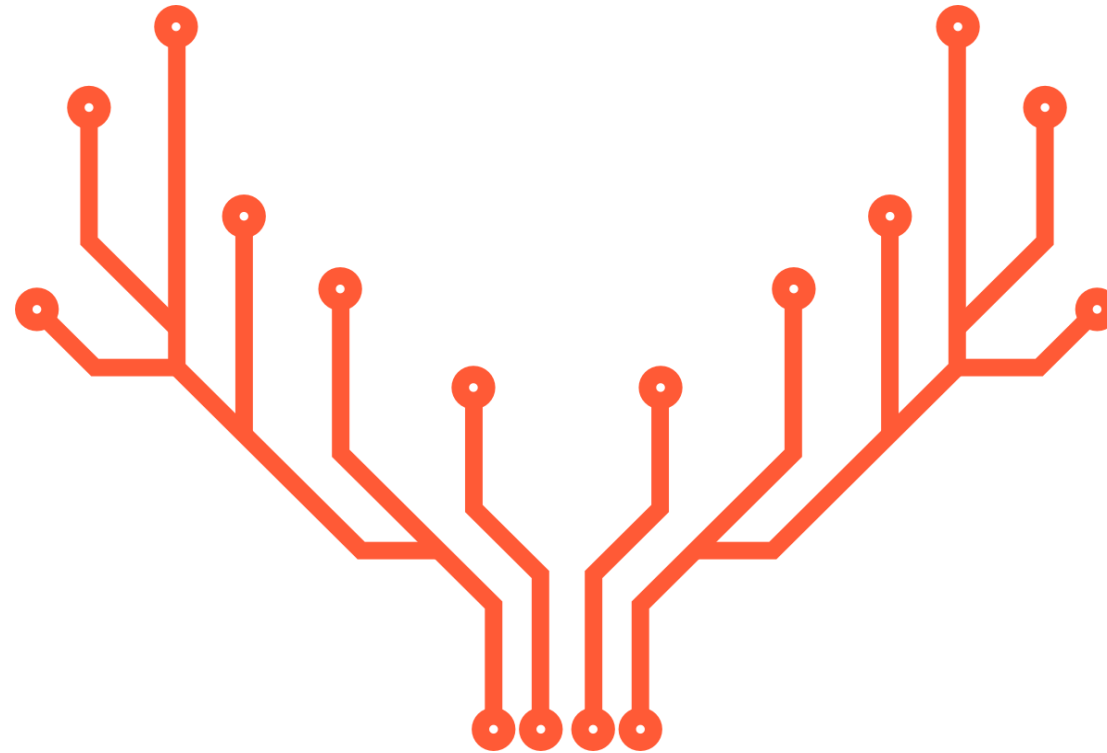


Every new prototype drives the development of a new DAQ system or modification of an existing one
(time consuming, not very efficient)

Why not a common versatile DAQ system ?

(Common hardware, firmware and software suit, keeping the focus of users on detector integration)

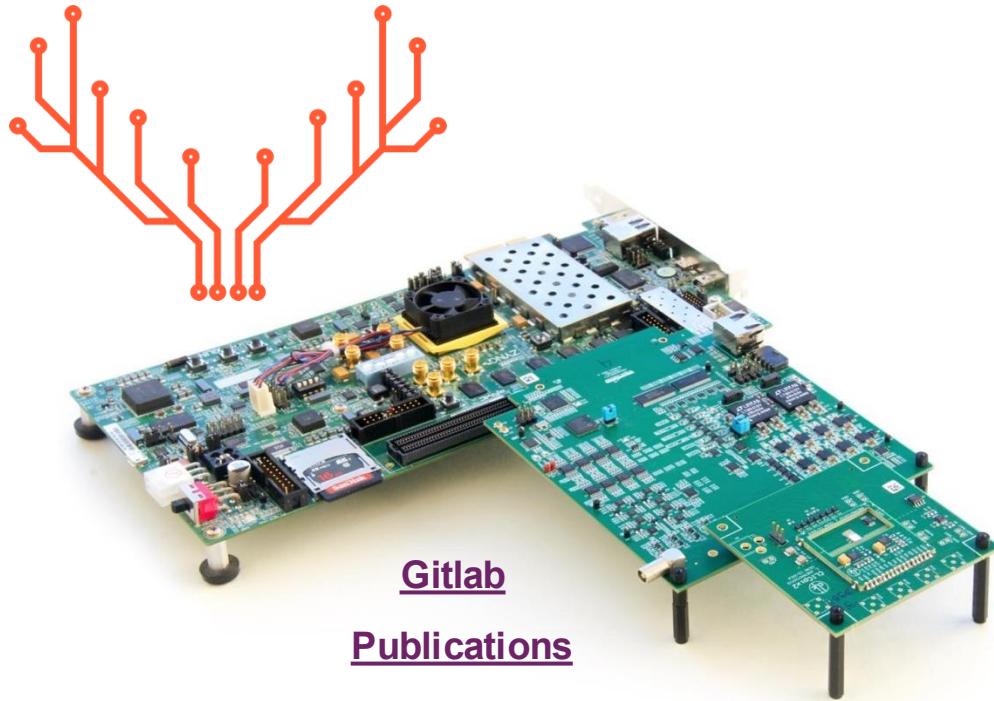
A particular solution to a particular need



Caribou

An open source common platform

Open source hardware, firmware and software for laboratory and beam tests

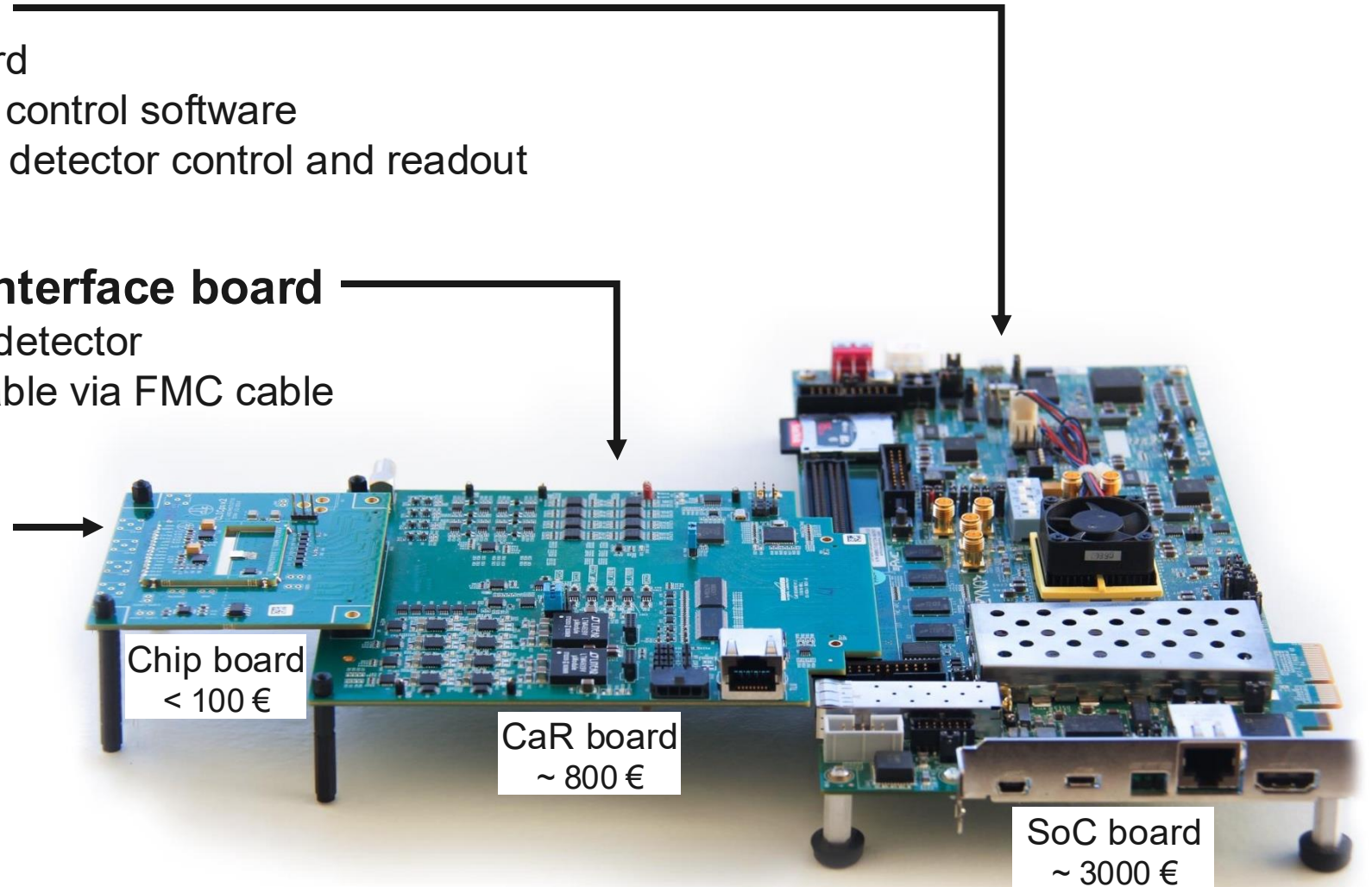


Developed by a collective effort of hardware, firmware and software developers



A modular system architecture

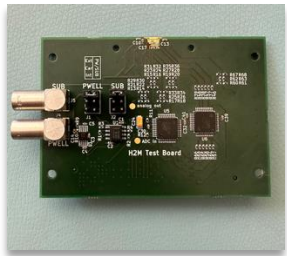
- **System-on-Chip (SoC) board**
 - ie: Xilinx ZC706 evaluation board
 - Embedded CPU runs DAQ and control software
 - FPGA runs custom firmware for detector control and readout
- **Control and Readout (CaR) interface board**
 - Physical interface from SoC to detector
 - CaR – SoC connection extendable via FMC cable
- **Detector (chip) carrier board**
 - Custom low-cost PCB
 - Designed by users



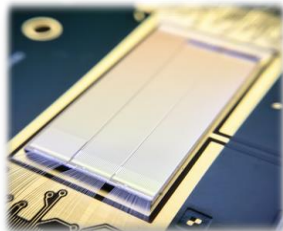
A custom detector chip board

- **Detector-specific**
 - Physical hardware hosting the detector
 - Only provide passives and detector-specific components
- **Multiple detectors already integrated and tested:**

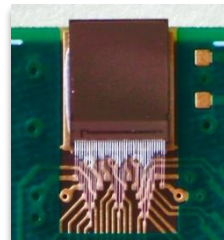
H2M



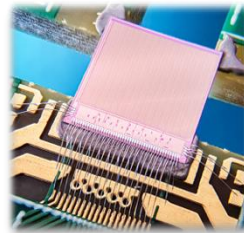
ATLASpix



CLICpix2



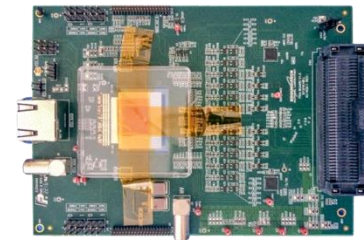
CLICTD



FASTPIX



H35Demo/FEI4



RD50-MPW1



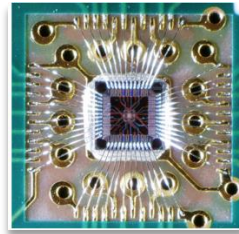
RD50-MPW2



RD50-MPW3



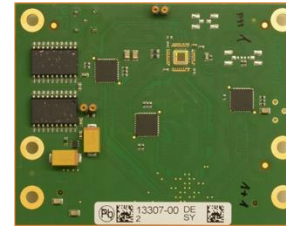
APTS



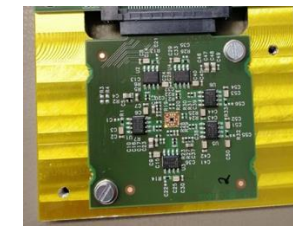
DPTS



dSiPM



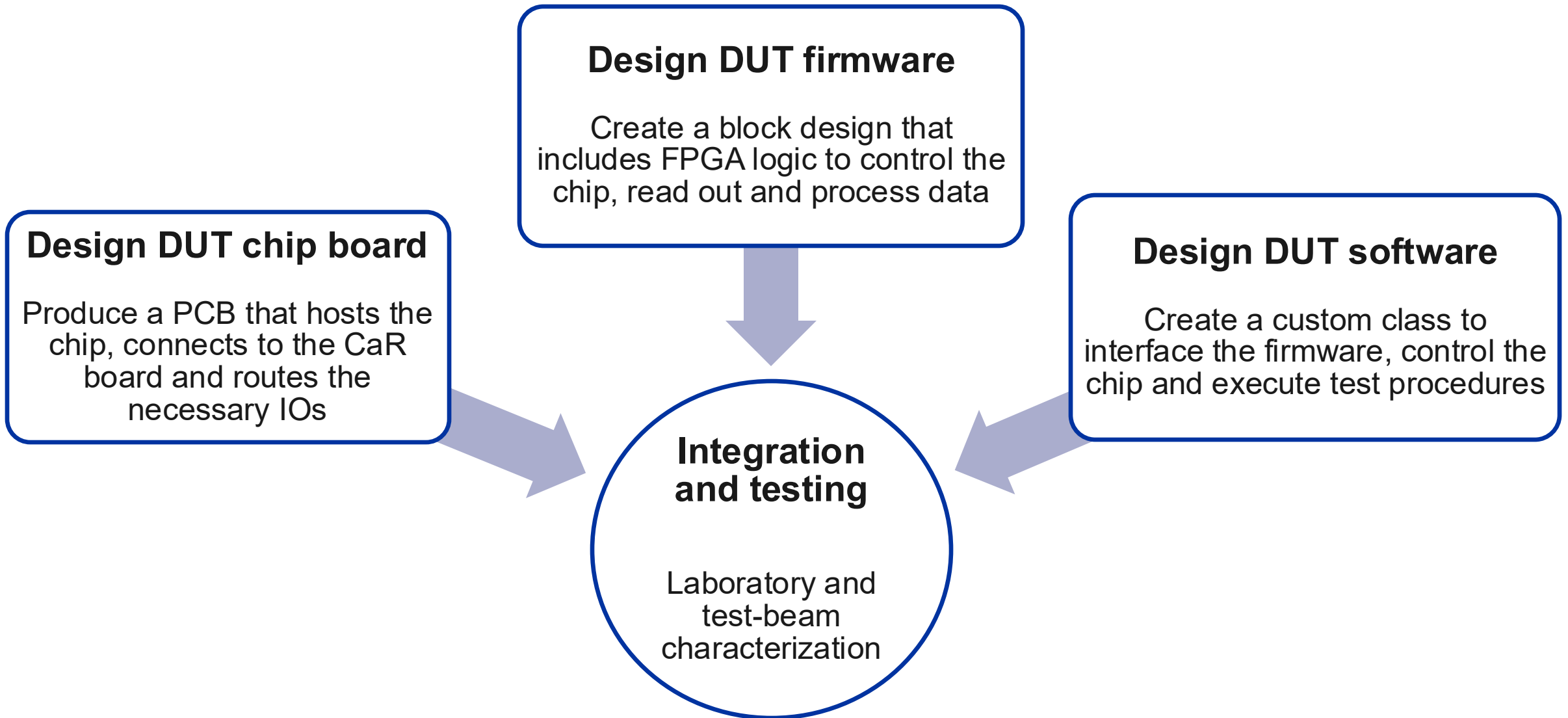
MLR1



CoRDIA



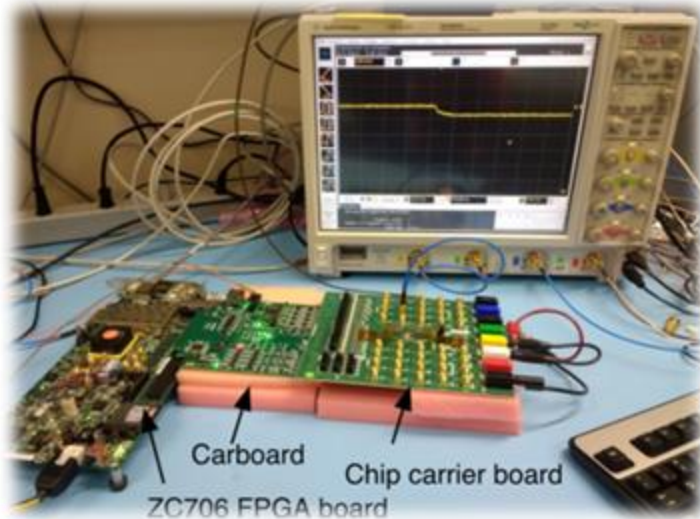
Device integration workflow



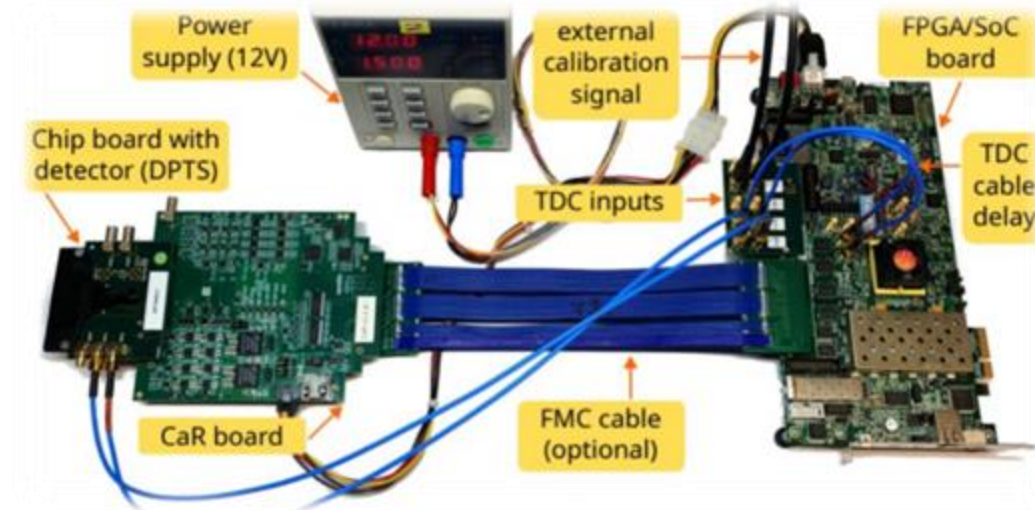
Application examples

- Support for various readout schemes
 - Digital interface via GTx or LVDS
 - Analogue waveforms (ADC or oscilloscope)
- Integration in beam telescope setups
 - Timepix3/SPIDR, Mimosas/EUDAQ, ALPIDE

FASTpix with oscilloscope readout



DPTS with TDC in FPGA readout



Telescope integration



CLICdp Timepix3 @ CERN

MIMOSA @ DESY

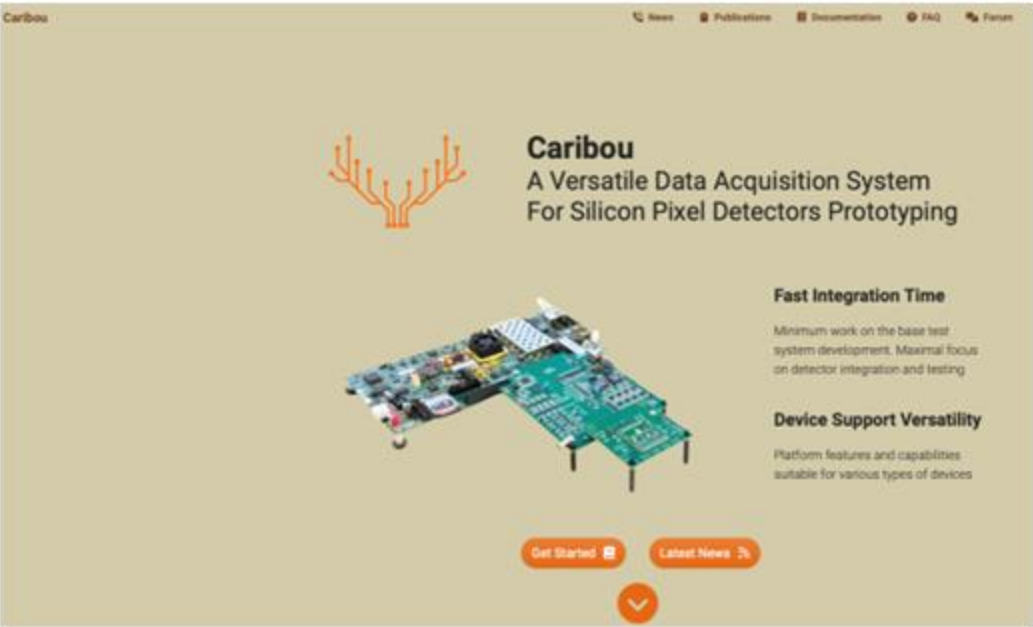


ALPIDE @ MAMI



Recent Developments & Future Plans

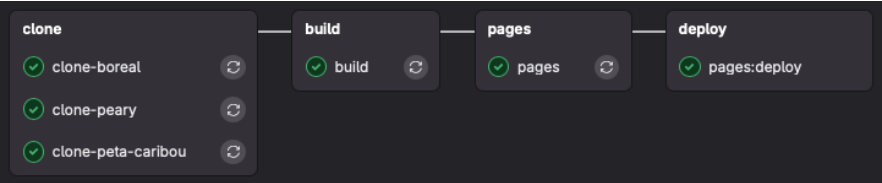
Project website and documentation



Project website

- Documentation
- Mattermost channel
- Publications
- Forum
- ...

Automatic documentation builds and website deployments



Website Gitlab project

CaR board v1.5 release

- Response to high CaR board demands
- Respin of CaR board v1.4
 - Replacement of obsolete components
 - Small improvements and bug fixes
- Production and distribution of 43 boards
 - RD50 + DRD3 common funds
 - Distributed to 15 institutes

To purchase
CaR boards



Contacts:

caribou-developers@cern.ch

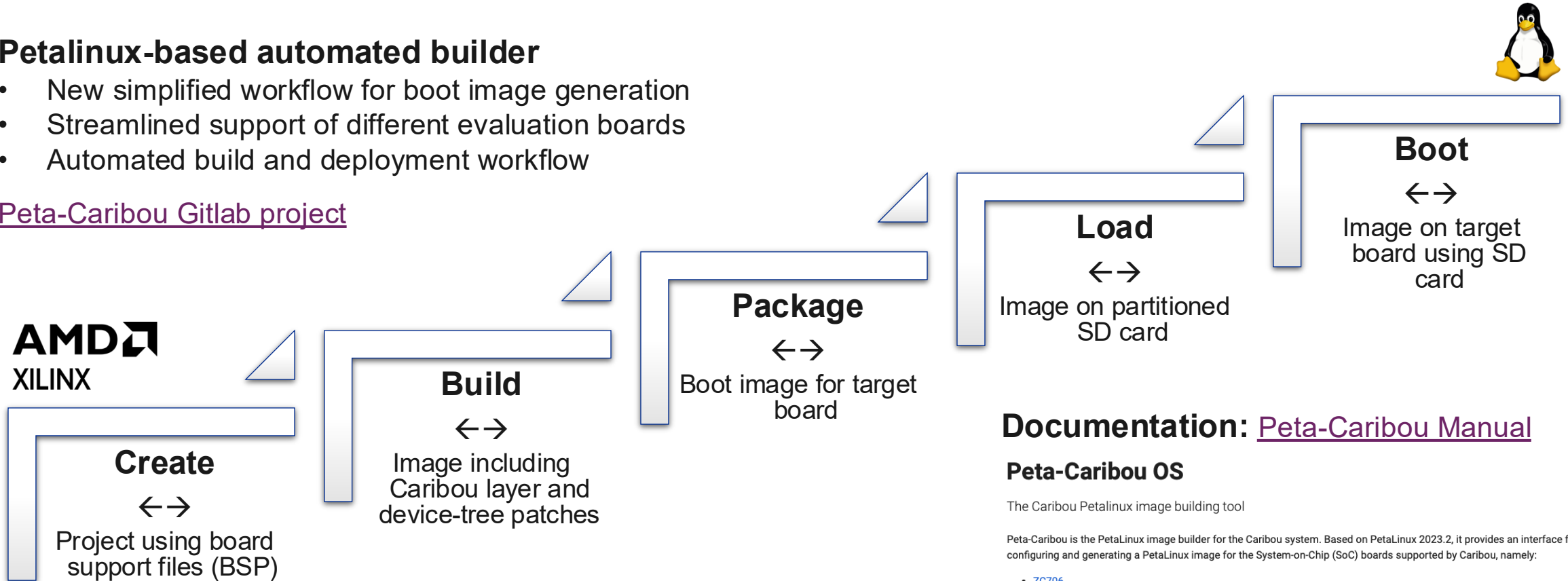


Peta-Caribou: Embedded Linux builder

Petalinux-based automated builder

- New simplified workflow for boot image generation
- Streamlined support of different evaluation boards
- Automated build and deployment workflow

[Peta-Caribou Gitlab project](#)



Documentation: [Peta-Caribou Manual](#)

Peta-Caribou OS

The Caribou Petalinux image building tool

Peta-Caribou is the PetaLinux image builder for the Caribou system. Based on PetaLinux 2023.2, it provides an interface for configuring and generating a PetaLinux image for the System-on-Chip (SoC) boards supported by Caribou, namely:

- ZC706
- ZCU102
- Mercury+ ST1 with a Mercury+ XU1 System-on-Module (SoM)

For details on installing PetaLinux, refer to the [Setup Environment](#) section.

At the core of Peta-Caribou is the Peta-Manager tool, an automation script that provides a command-line interface for configuring, building, loading, updating, and deploying the PetaLinux image. A detailed overview of the supported workflow and commands can be found in the [Peta-Caribou Manager](#) section.

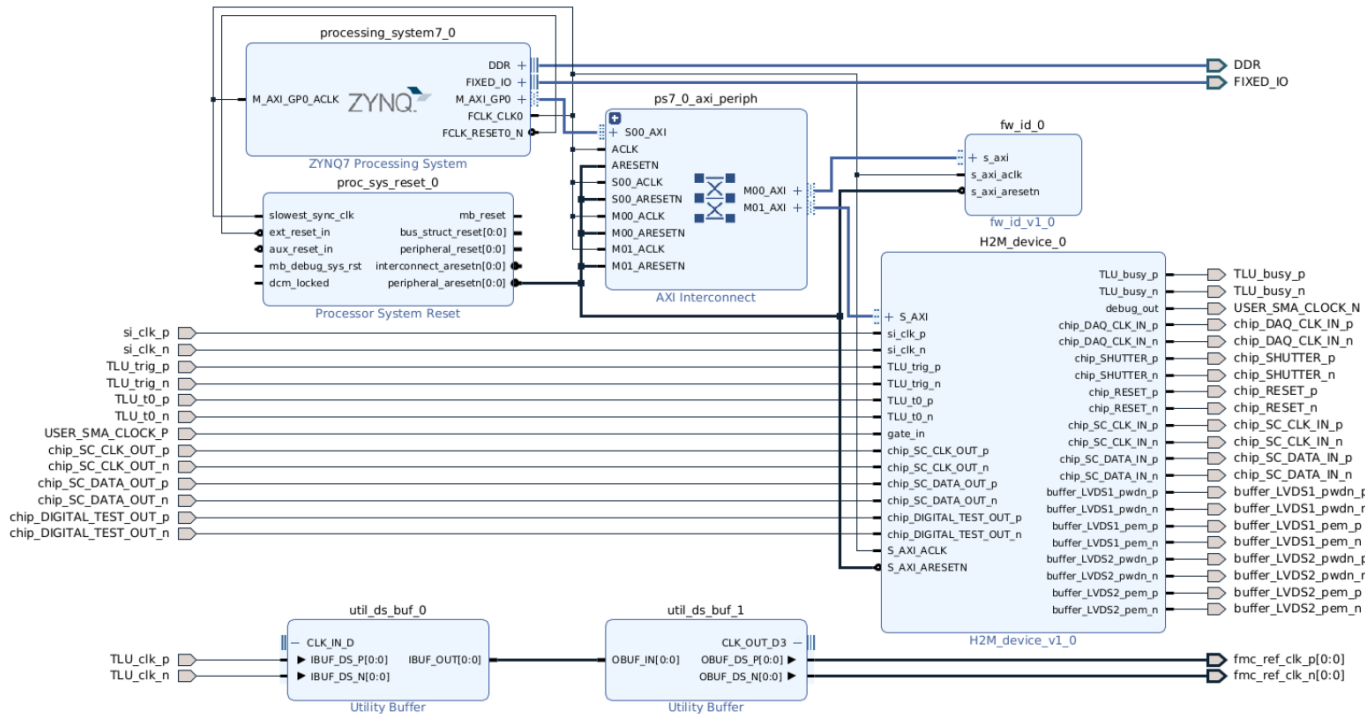
The Peta-Caribou Git repository is available at this [link](#)

Boreal: Unified FPGA firmware framework

Unified and modular framework

Easy and fast device integration

[Boreal Gitlab project](#)

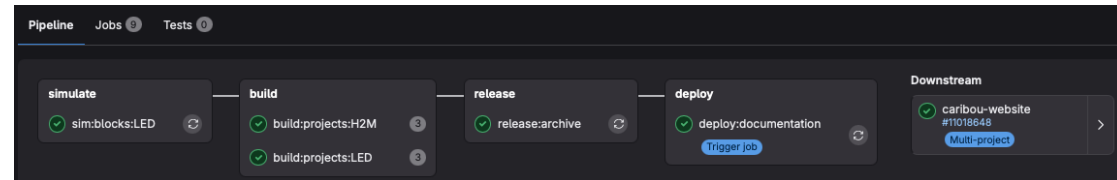


Pilot project
H2M : DESY, CERN

Reusable modules: [boreal-modules](#)

Name	Last commit	Last update
..		
fw_id	do not include vivado project	1 month ago
pattern_generator/hdl	pushing latest versions of pattern generator and syncers	1 month ago
pulser/src	bringing some modules from the legacy repo	6 days ago
reg_map	adding simulation check script	1 week ago
shutter_delay/src	bringing some modules from the legacy repo	6 days ago
syncers/hdl	pushing latest versions of pattern generator and syncers	1 month ago
timestamps/src	bringing some modules from the legacy repo	6 days ago
ad9249_interface @ 48863919	adding high speed ADC to boreal modules	1 week ago

Streamlined CI/CD workflow
Simulation, building and bitfile release



Documentation: [Boreal Manual](#)

Boreal Firmware

The Caribou FPGA design framework

Introduction

The Boreal project is the unified FPGA design framework for the Caribou base system and all its supported devices. It offers a common development environment consolidated that simplifies the integration of new devices across multiple platforms. Boreal provides various commercial or custom IPs, project management tools and a streamlined development workflow.

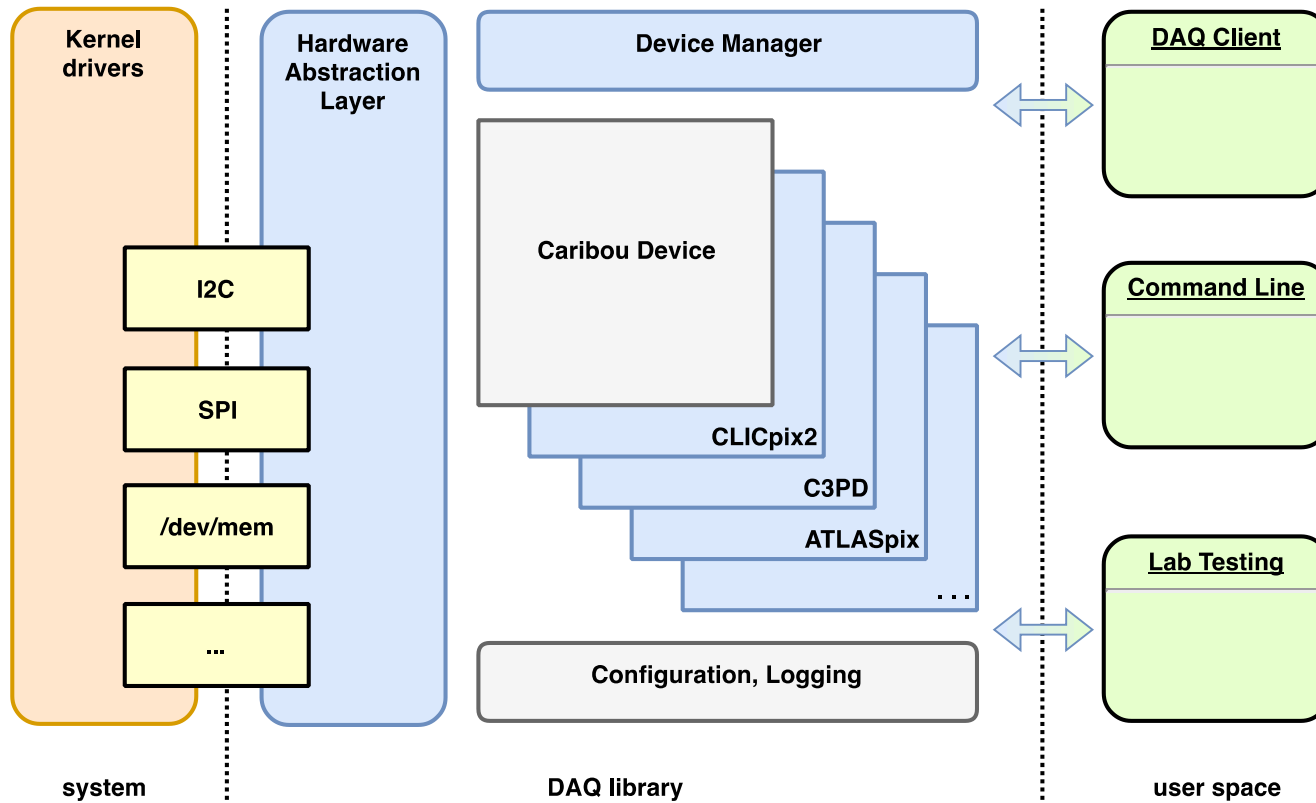
The firmware name derives from the North American subspecies of reindeer, the Boreal woodland caribou, found primarily in Canada ([Wikipedia](#))

Peary: Software Framework

Unified, modular

Provides many features needed in laboratory and test-beam

[Peary Gitlab project](#)



Documentation: [Peary Manual](#)

Peary Software

The Caribou DAQ software framework

This is the user manual for the Peary Caribou software, a DAQ framework for the Caribou DAQ system. It aims to provide an overview of the software framework and facilitating the implementation of new devices.

Introduction

The Peary DAQ software framework provides hardware abstraction for periphery components such as voltage regulators and simplifies direct detector configuration and data acquisition through a common interface.

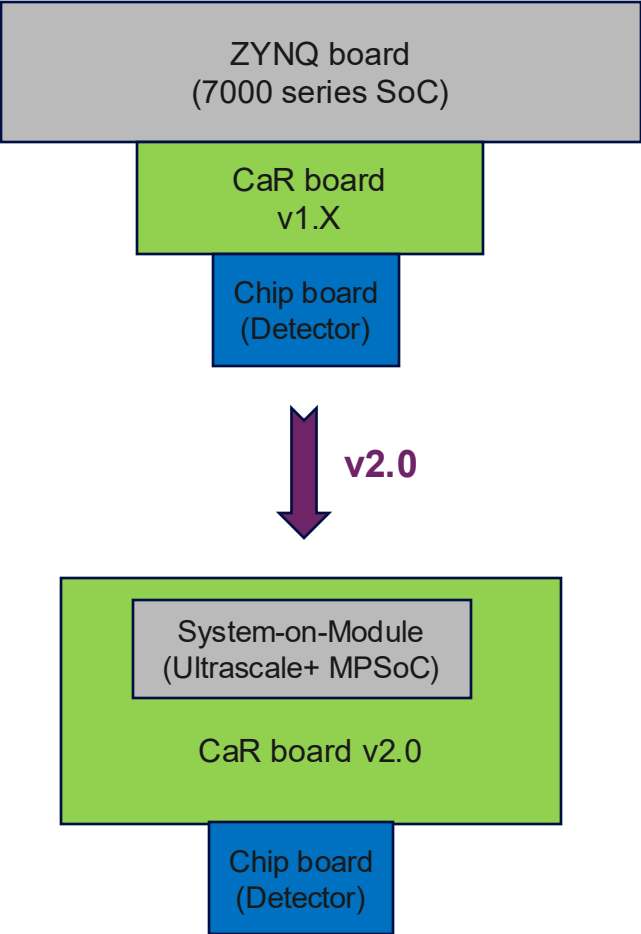
A command line tool as well as a producer for EUDAQ2.0 integration is provided.

The software name derives from the smallest of the North American caribou subspecies, found in the high Arctic islands of Canada ([Wikipedia](#)).

Peary Workshop / Hackaton

Objective: Rethink the framework architecture, software hierarchy, device classes and hardware abstraction in view of expanding the portfolio of supported boards

Caribou v2.0



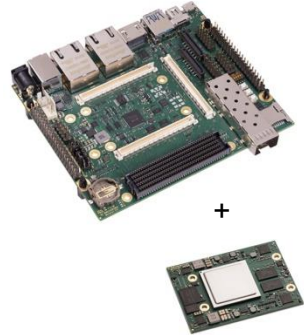
- Based on commercial **System-on-Module (SoM)**
 - Integrated to the CaR board
 - Optimize system cost, increase flexibility and performance
- Targeting Mercury+ XU1 (UltraScale+) System-on-Module
- Test-board design finalized; Final board design progressing
- Expanding portfolio of supported boards



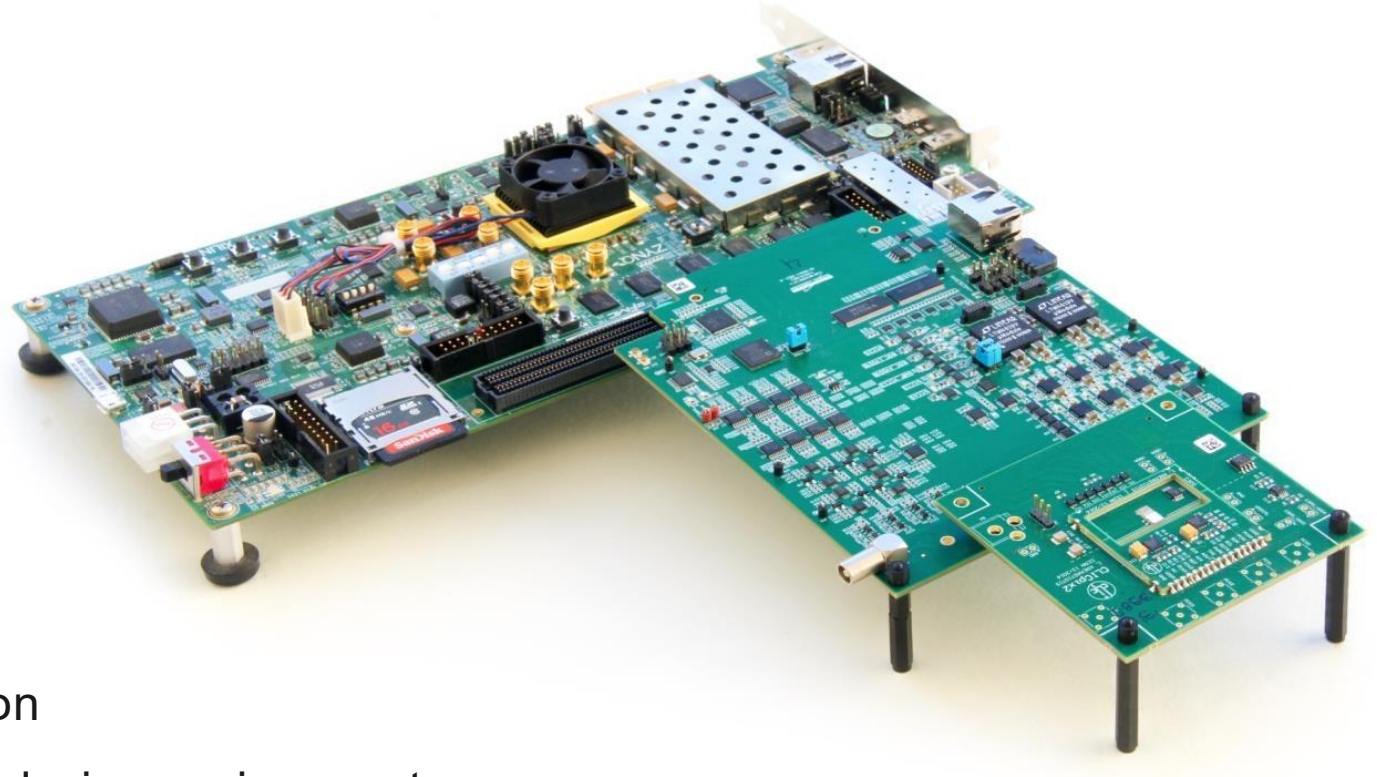
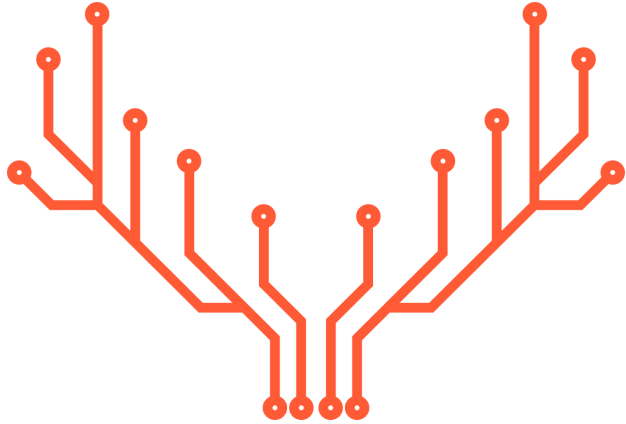
Supported
But discontinued for purchase



Supported
Intermediate step towards Caribou v2.0



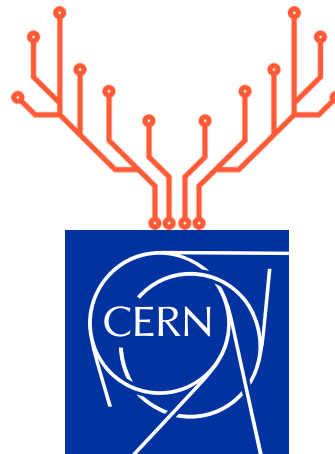
Summary



- Release of project website
- Release of new CaR board version
- Unification of the FPGA firmware design environment
- Development of a new embedded Linux build workflow
- Expanding portfolio of supported boards
- Development of Caribou v2.0 with new SW and HW architectures



Thank you



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