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Test beam results of 65 nm CMOS monolithic sensors with Operational Amplifier output buffer for the ALICE ITS3 upgrade

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During the 3^{rd} LHC Long Shutdown (LS3) that will take place in the years 2026-2030 the three innermost layers of the ALICE Inner Tracking System (ITS) will be replaced by a truly cylindrical tracker (ITS3) consisting of Monolithic Active Pixel Silicon (MAPS) sensors in a 65 nm technology.

A thickness reduction to 50 µm will allow the bending of silicon sensors to realize a semi-cylindrical self-sustaining half layer. Therefore, a very low material budget (0.07 X/X_0 per layer) will be achieved thus improving the tracking capability and efficiency at low transverse momentum (p_T < 0.1 GeV/c) by a factor of two.

An Analog Pixel Test Structure (APTS) has been developed by the ALICE and CERN R&D in the context of the Multi-Layer Reticle 1 submission to validate the candidate technology. It consists of a 6 x 6 pixel matrix with 10, 15, 20 and 25 µm pitch characterized by a low dose n-implant in the epitaxial layer near the collection diode. Two different output buffers have been developed: one based on a high-speed individual operational amplifier (APTS-OA) that allows to explore timing performance, and a classical one based on source-follower stage (APTS-SF).

Test beam campaigns have been performed at the CERN-SPS facility (120 GeV/c particles) to investigate the APTS-OA using ALPIDEs as tracking planes and an APTS-SF as trigger plane.

In this contribution, timing measurements indicating 63 ps time resolution, a detection efficiency exceeding 99%, together with the ongoing activities will be presented to demonstrate the suitability of the technology to the ITS upgrade requirements.

Moreover, due to the different characteristics of the telescope planes a particular focus on the integration readout systems will be shown.

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