

# Large-scale Integrated Circuits with 2D MoS<sub>2</sub> for Neuromorphic Computing

Prof. Andras Kis

22.11.24.



# Science and Engineering with 2D Semiconductors

## “Classical” semiconductor devices

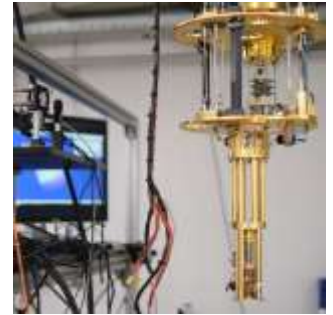
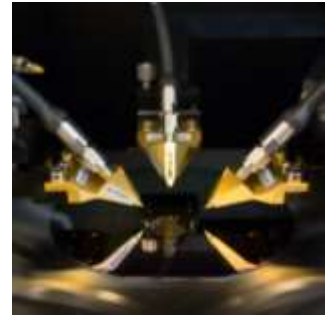
- Mobility, current density, high-frequency performance
- Memory devices, neural networks

## New concepts

- Valley/spin optics and electronics
- Excitonic devices and circuits

## Material growth

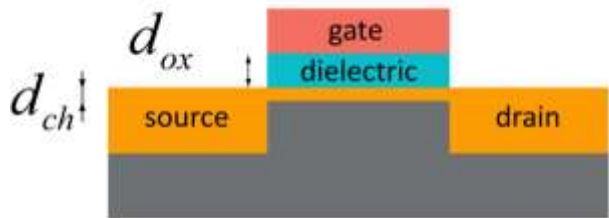
- MOCVD and CVD growth of TMDCs and heterostructures
- MBE growth of TMDCs and heterostructures



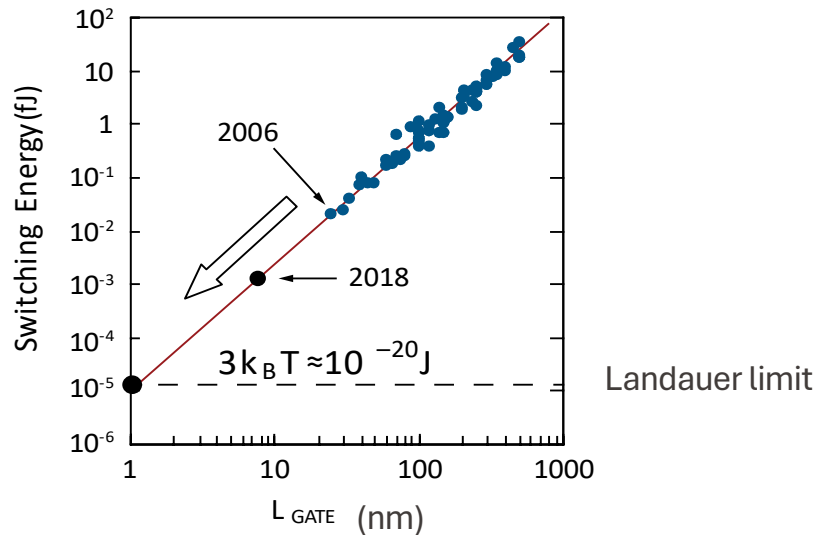
# IT Energy Problem



[http://www.phys.ncku.edu.tw/~htsu/humor/fry\\_egg.html](http://www.phys.ncku.edu.tw/~htsu/humor/fry_egg.html)



## Single device:



Cavin et al. J Nanopart Res (2006)

## System level:

Intel Core i7 8700K processor (2017)

**$10^9 \times$  worse!** (2.5 GFLOPS/W)

Frontier supercomputer (ORNL, 2022)

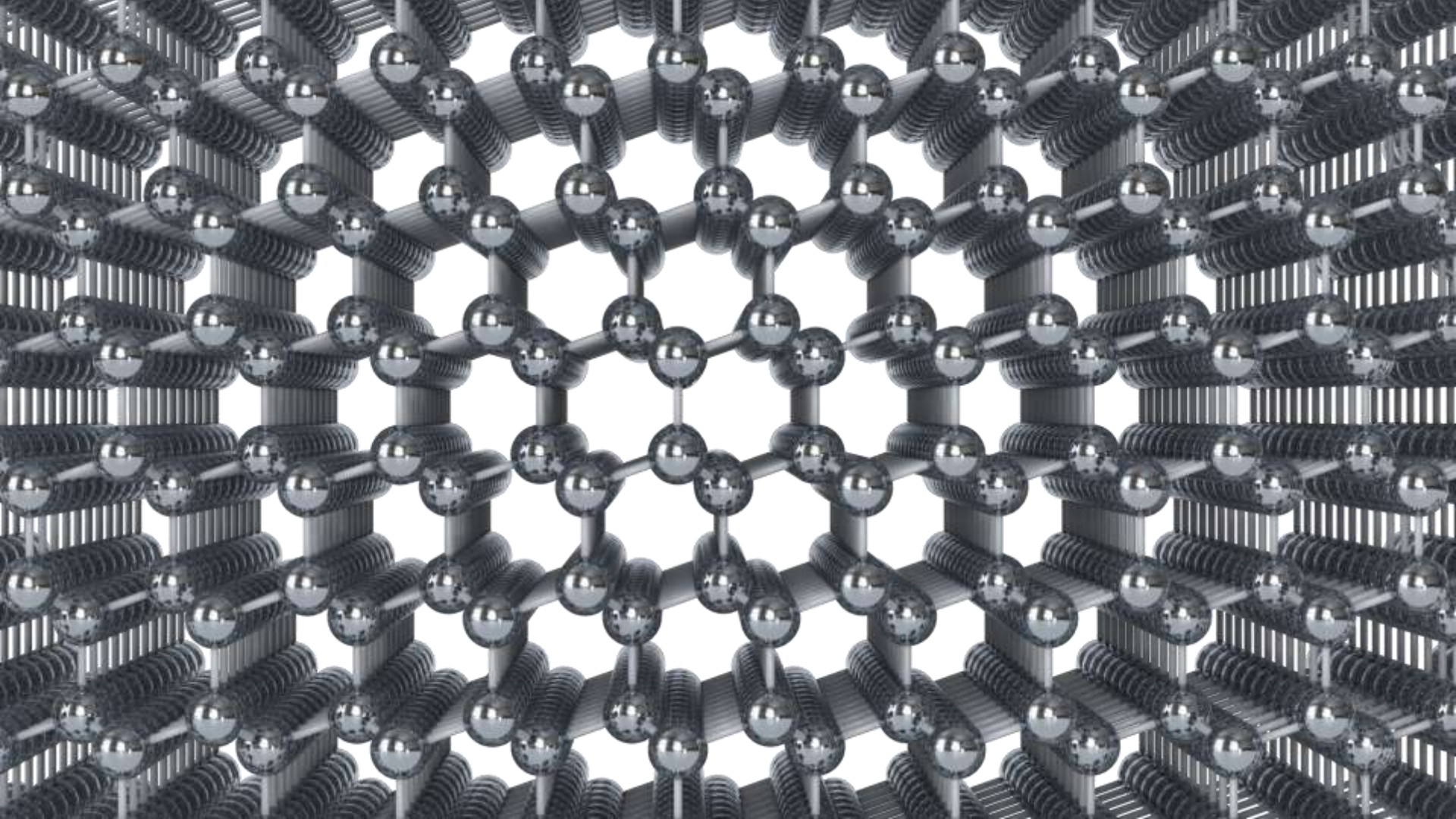
**$4 \cdot 10^7 \times$  worse** (62.68 GFLOPS/W)

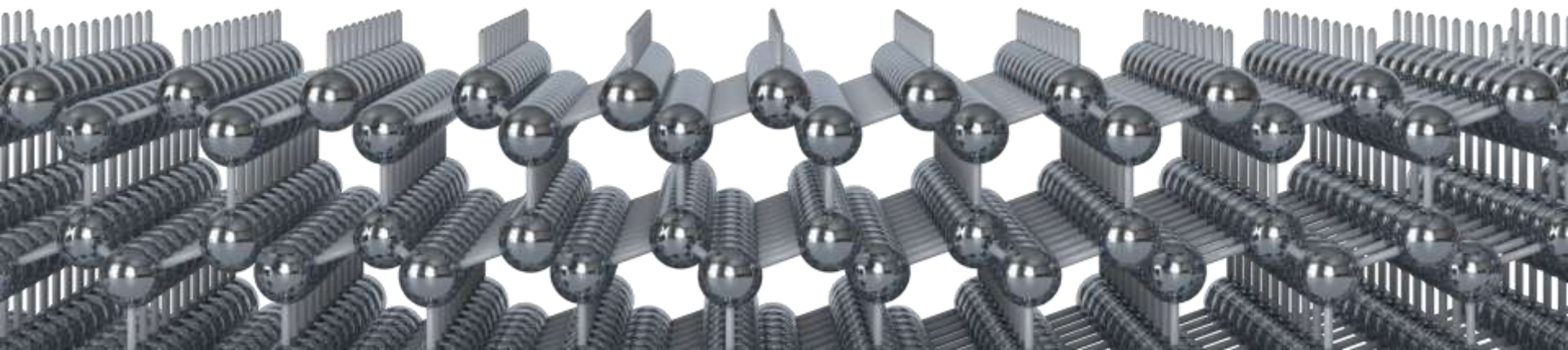
A100 40 GB (NVIDIA, 2023)

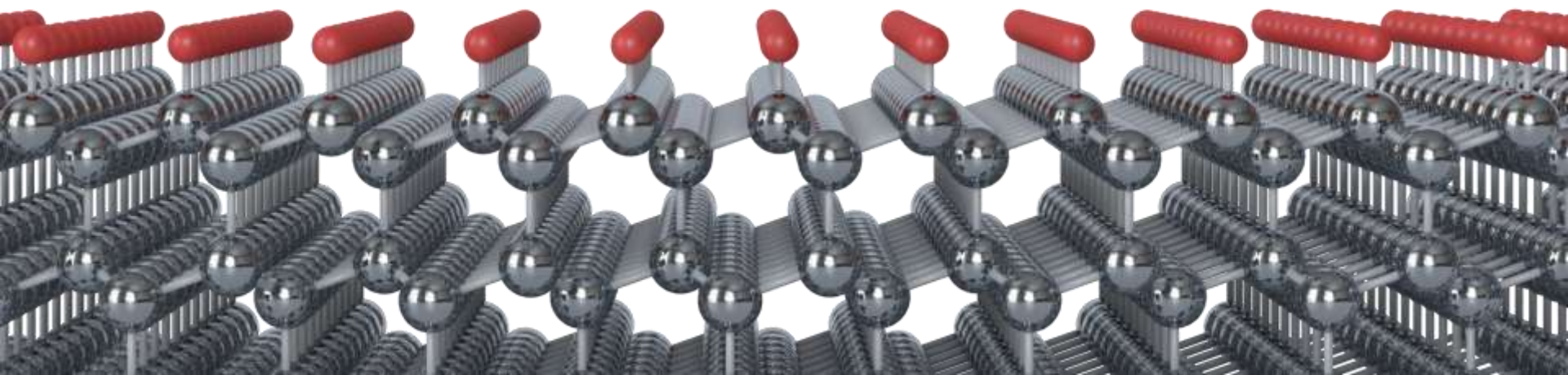
**$3.7 \cdot 10^7 \times$  worse** (78 GFLOPS/W)



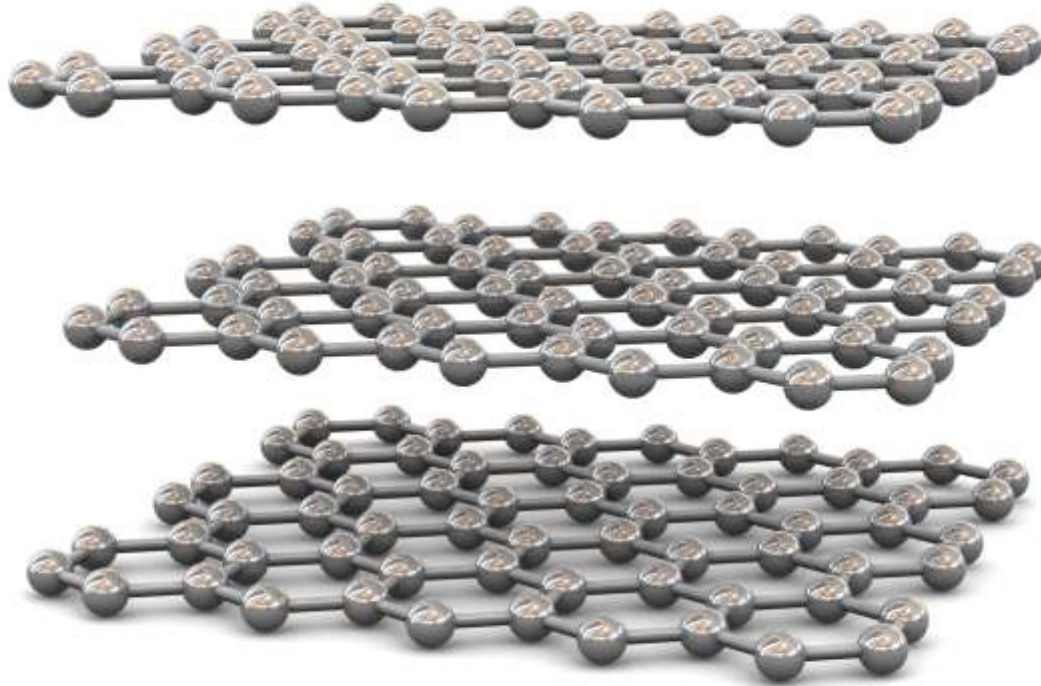
John von Neumann





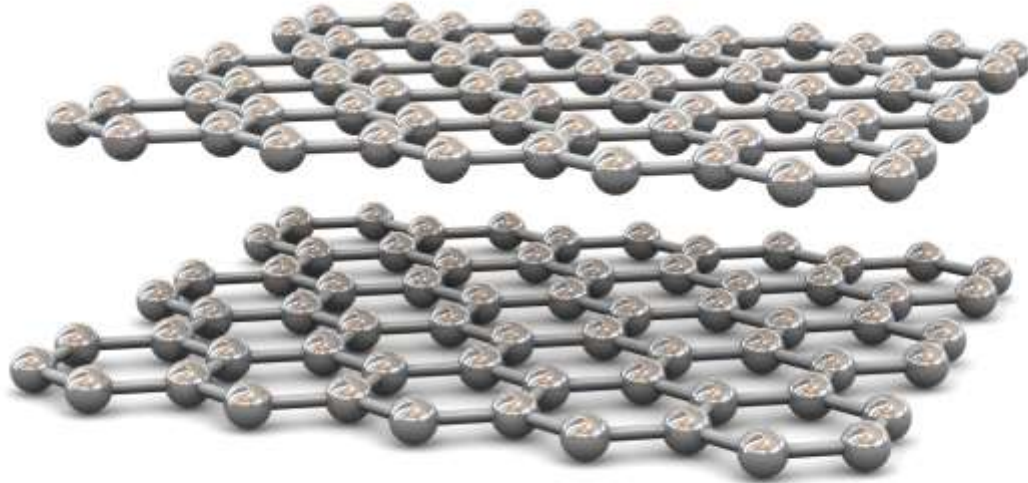


# Graphite and Graphene



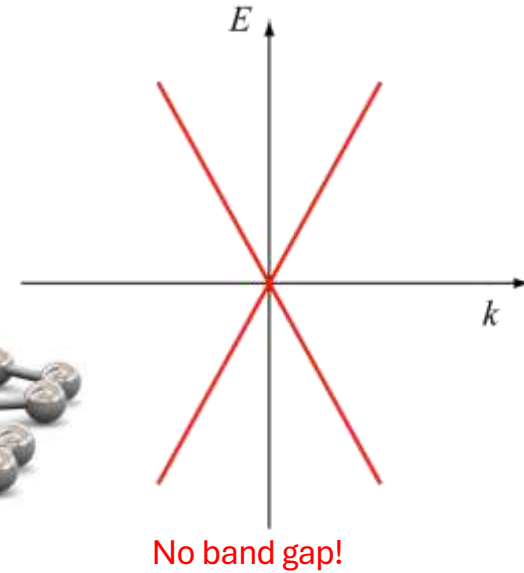


# Graphite and Graphene



# Graphite and Graphene

2010 Physics Nobel Prize (Andre Geim, Konstantin Novoselov)

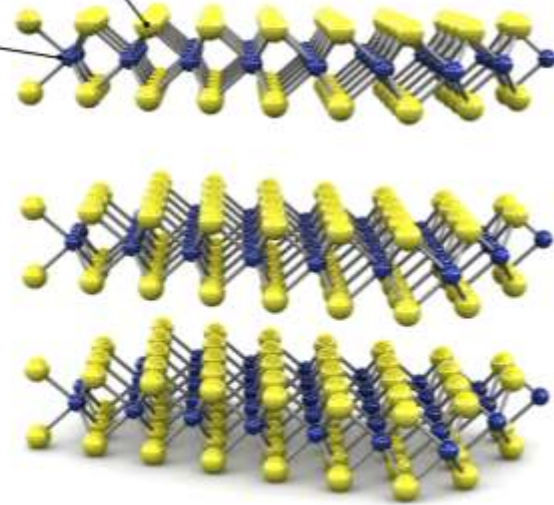


# 2D Transition Metal Dichalcogenides (TMDCs)

H																	He
Li	Be											B	C	N	O	F	Ne
Na	Mg											Al	Si	P	S	Cl	Ar
K	Ca	Sc	Ti	V	Cr	Mn	Fe	Co	Ni	Cu	Zn	Ga	Ge	As	Se	Br	Kr
Rb	Sr	Y	Zr	Nb	Mo	Tc	Ru	Rh	Pd	Ag	Cd	In	Sn	Sb	Te	I	Xe
Cs	Ba	La	Hf	Ta	W	Re	Os	Ir	Pt	Au	Hg	Tl	Pb	Bi	Po	At	Rn
Fr	Ra	An	Rf	Db	Sg	Bh	Hs	Mt	Ds	Rg							
			La	Ce	Pr	Nd	Pm	Sm	Eu	Gd	Tb	Dy	Ho	Er	Tm	Yb	Lu
			Ac	Th	Pa	U	Np	Pu	Am	Cm	Bk	Cf	Es	Fm	Md	No	Lr

Common formula:  $\text{MX}_2$

40 stable materials



Semiconductors:  $\text{MoS}_2$   $\text{MoSe}_2$   $\text{WS}_2$   $\text{WSe}_2$   
 $\text{MoTe}_2$   $\text{WTe}_2$

Semimetals:  $\text{TiS}_2$   $\text{TiSe}_2$

Metals, CDW,  
 superconductors:  $\text{NbSe}_2$   $\text{NbS}_2$   $\text{NbTe}_2$   
 $\text{TaS}_2$   $\text{TaSe}_2$   $\text{TaTe}_2$

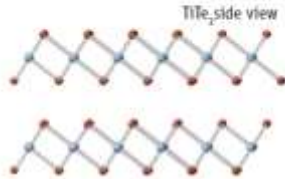
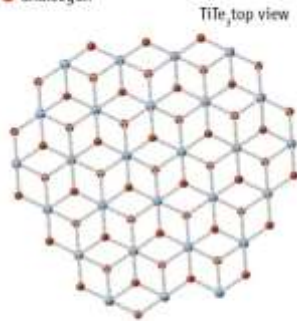
# Tip of the Iceberg

>500 potentially interesting 2D materials

## Transition metal trichalcogenides

$AMo_3X_6$ ,  $NbX_3$ ,  $TiX_3$ , and  $TaX_3$  (X = S, Se, or Te)

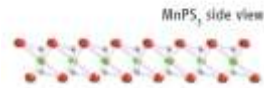
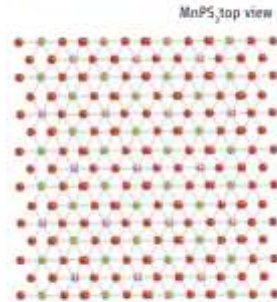
- Transition metal
- Chalcogen



## Metal phosphorous trichalcogenides

Metal phosphorous trichalcogenides (MPX<sub>3</sub>), such as MnPS<sub>3</sub>, CdPS<sub>3</sub>, NiPS<sub>3</sub>, ZnPS<sub>3</sub>, and Mn<sub>0.5</sub>Fe<sub>0.5</sub>PS<sub>3</sub>

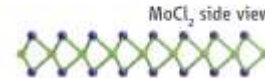
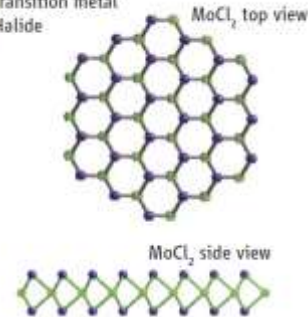
- Transition metal
- Chalcogen
- Phosphorus



## Transition metal dihalides

Transition-metal dihalides\*

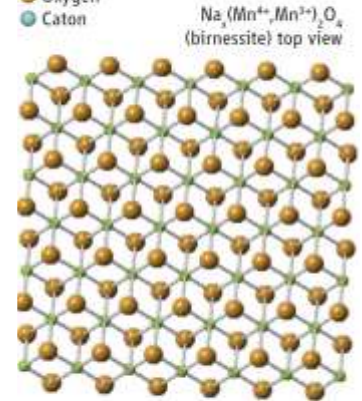
- Transition metal
- Halide



## Transition metal oxides

Transition metal oxides : Ti oxides, Ti<sub>0.71</sub>O<sub>2</sub>, Ti<sub>0.87</sub>O<sub>2</sub>, Ti<sub>3</sub>O<sub>7</sub>, Ti<sub>4</sub>O<sub>7</sub>, Ti<sub>5</sub>O<sub>11</sub>; Nb oxides, Nb<sub>3</sub>O<sub>8</sub>, Nb<sub>6</sub>O<sub>17</sub>, HNb<sub>3</sub>O<sub>8</sub>; Mn oxides, MnO<sub>2</sub>, Ti<sub>3</sub>O<sub>5</sub>, Na<sub>2</sub>(Mn<sup>4+</sup>,Mn<sup>3+</sup>)<sub>2</sub>O<sub>8</sub>

- Transition metal
- Oxygen
- Cation

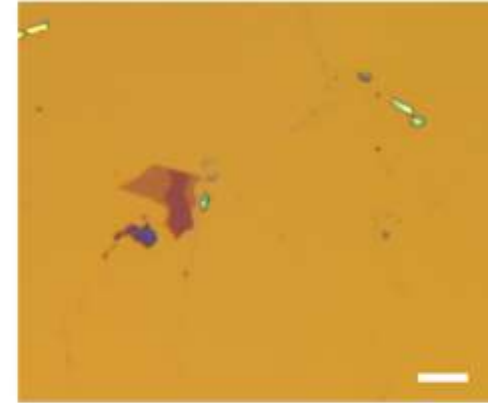
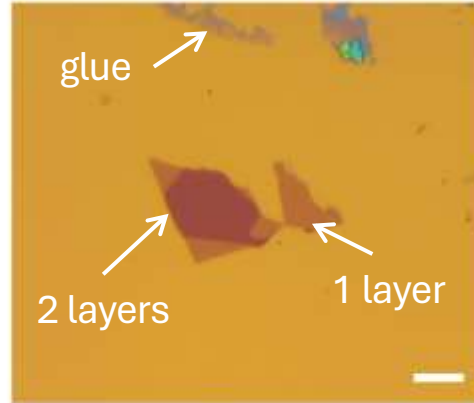
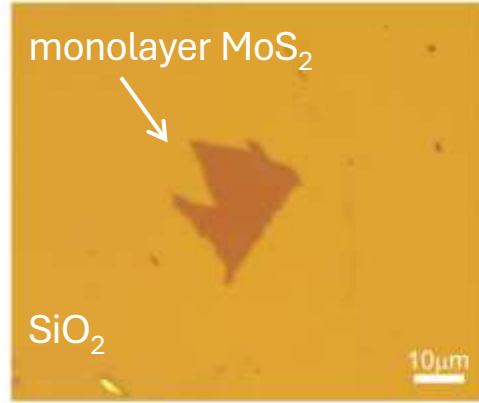


Nicolosi...Coleman; Science (2013)



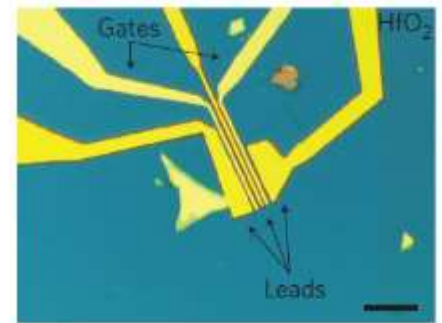
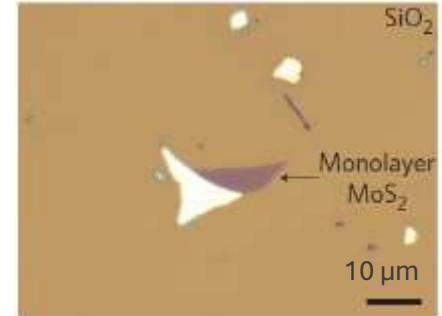
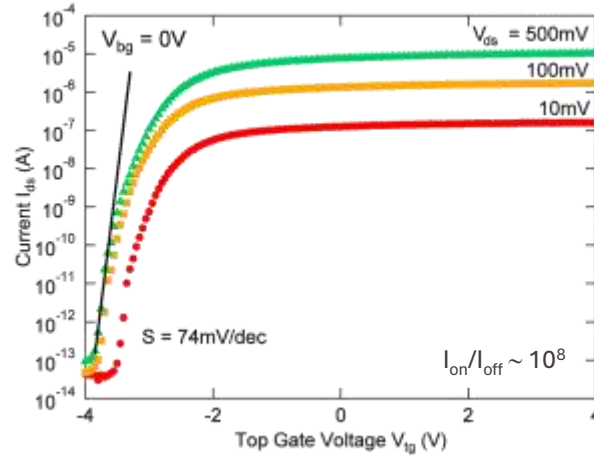
Molybdenite on quartz, Moly Hill mine, La Motte, Québec, Canada  
Source: Wikipedia

# Scotch Tape Exfoliation



Benameur...Kis, Nanotechnology (2011)

# Our First Contribution: Monolayer MoS<sub>2</sub> Transistor



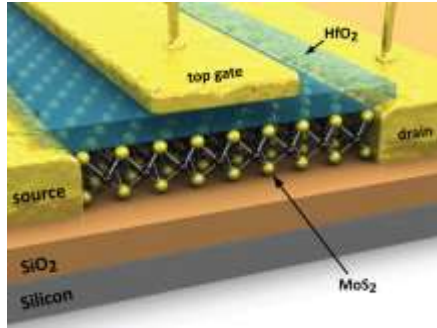
Gate length:	500 nm
Channel width:	4 μm
On/Off:	10 <sup>8</sup>
ON current:	2.5 μA/μm
OFF current:	25 fA/μm

Radisavljevic...Kis, Nature Nanotechnology (2011)

Patent US9608101B2

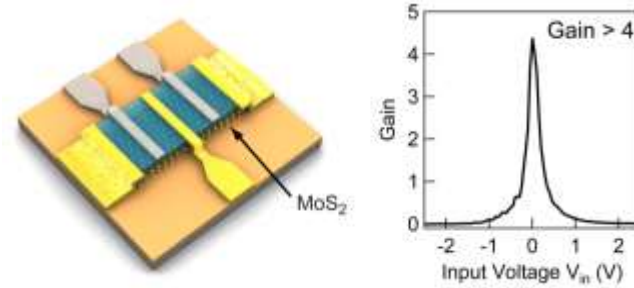
# 2D Device Breakthroughs

## MoS<sub>2</sub> Transistor



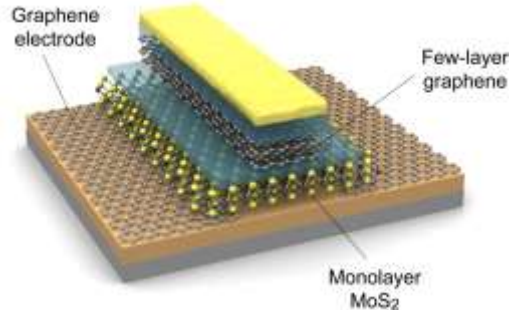
Radisavljevic...Kis; Nature Nanotech. (2011)

## MoS<sub>2</sub> Inverter



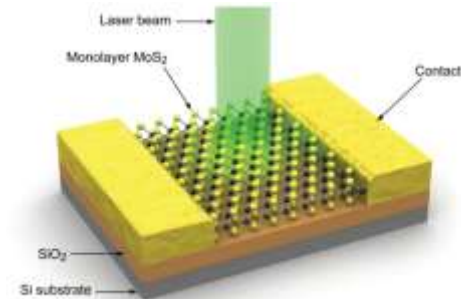
Radisavljevic...Kis; ACS Nano (2011)

## MoS<sub>2</sub> Memory Cell



Bertolazzi...Kis; ACS Nano (2013)

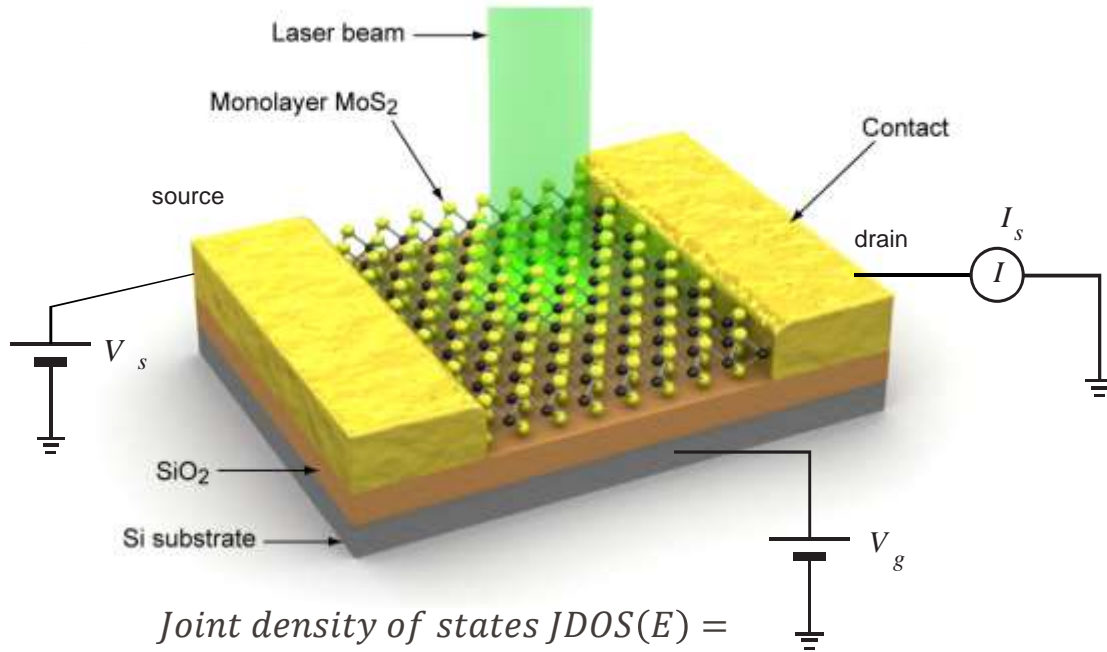
## Ultrasensitive Photodetector



Lopez-Sanchez...Kis; Nature Nanotech. (2013)



# Phototransistors/photodetectors

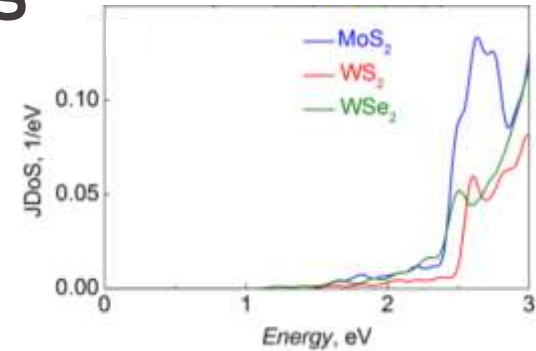


$$\text{Joint density of states } JDOS(E) = \frac{1}{4\pi^3} \int d^3k \delta(E_{V,k} - E_{C,k} - E)$$

$$\text{Photocurrent } I_{ph} = I_{light} - I_{dark}$$

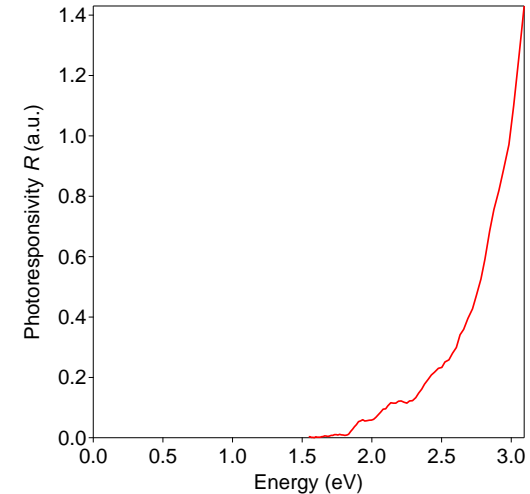
$$\text{Responsivity } R = \frac{I_{ph}}{P_{inc}}$$

## Calculations



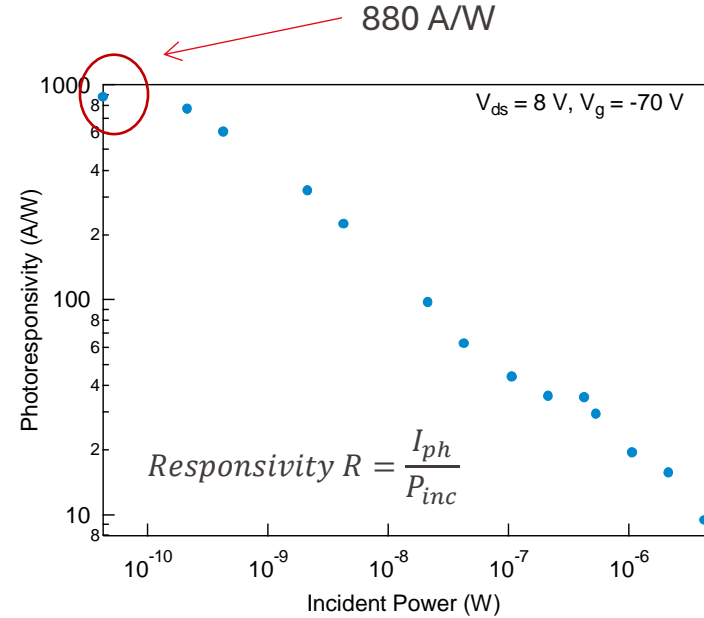
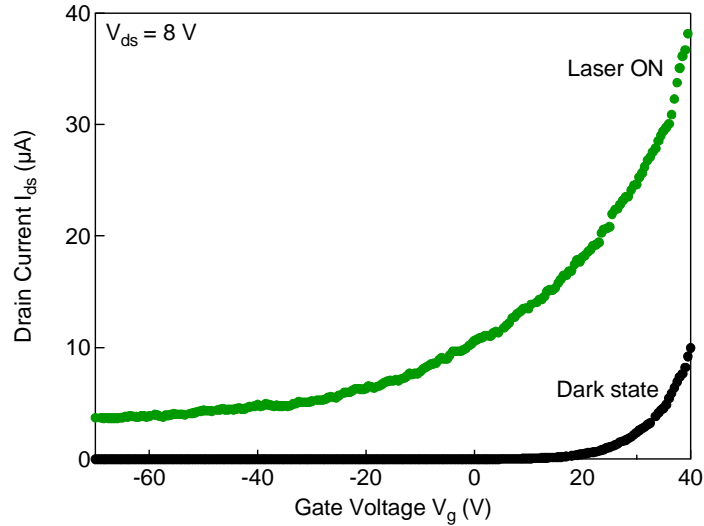
Britnell...Novoselov; Science (2013)

## Measurements



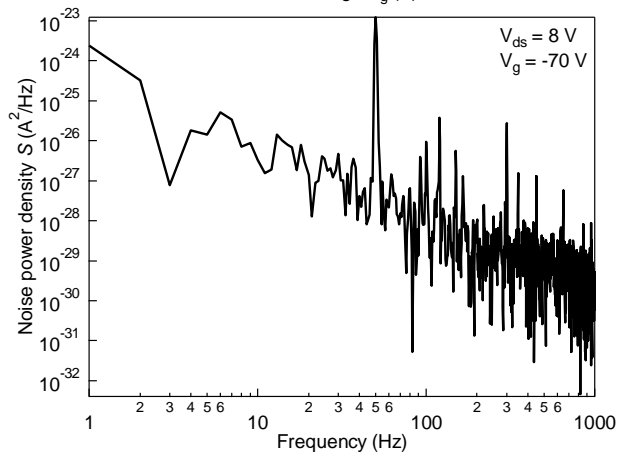
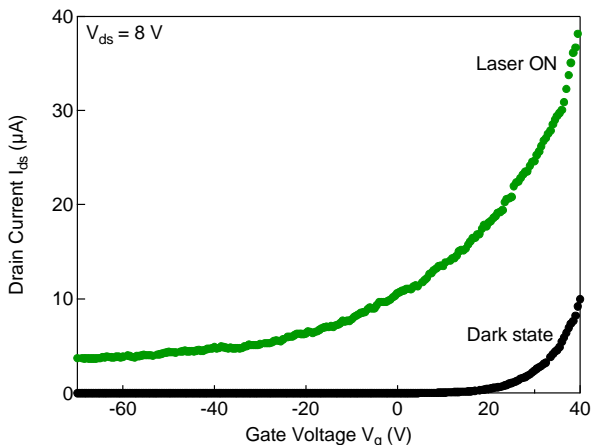
Lopez Sanchez...Kis; Nat. Nanotech. (2013)

# MoS<sub>2</sub> Photodetectors: Responsivity



Lopez-Sanchez, Nature Nanotechnology (2013)

# MoS<sub>2</sub> Photodetectors: Noise



- **Si diodes**

Photoresponsivity:

0.5 A/W

NEP:

$1 \times 10^{-14}\text{ W/Hz}^{1/2}$

- **MoS<sub>2</sub>**

Photoresponsivity:

880 A/W

NEP:

$1.8 \times 10^{-15}\text{ W/Hz}^{1/2}$

Equivalent min. photon flux  
for the MoS<sub>2</sub> photodetector:

$1 \times 10^{-17}\text{ lux}$

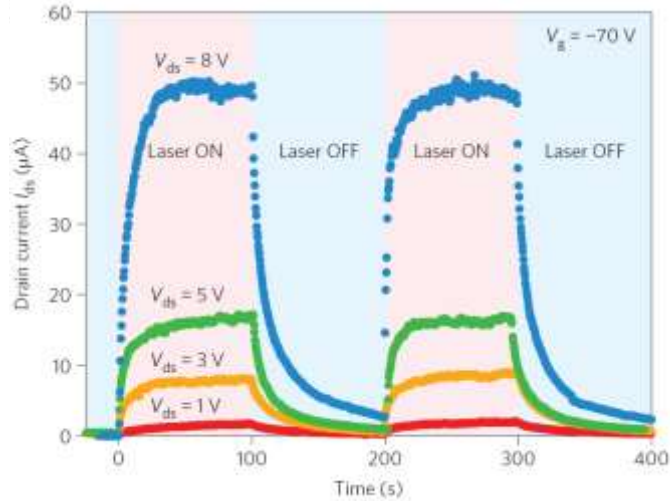
Full moon:

0.1-0.3 lux

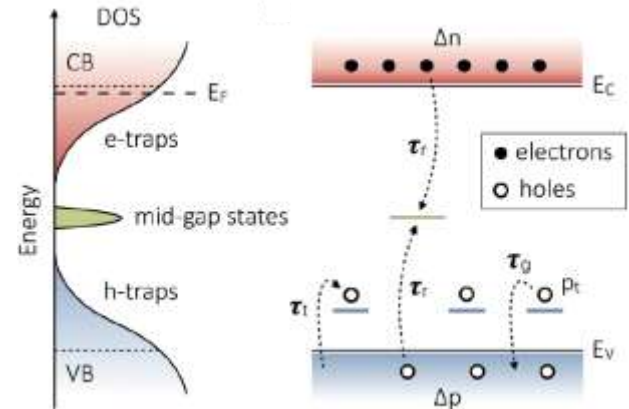
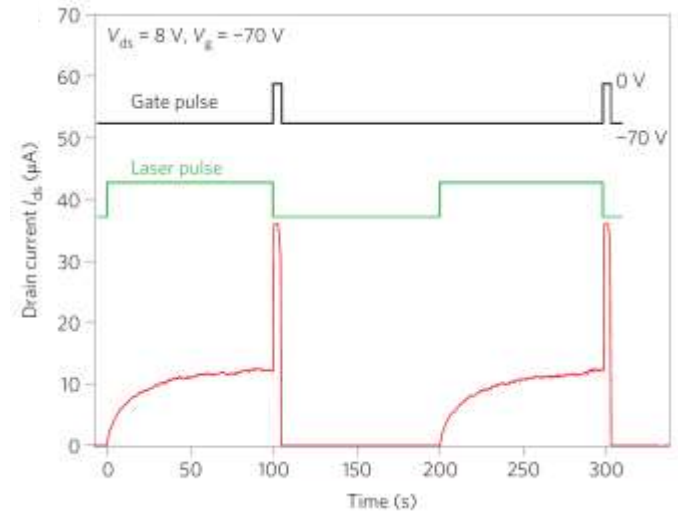
Starlight, no airglow, no moon:

0.0001 lux

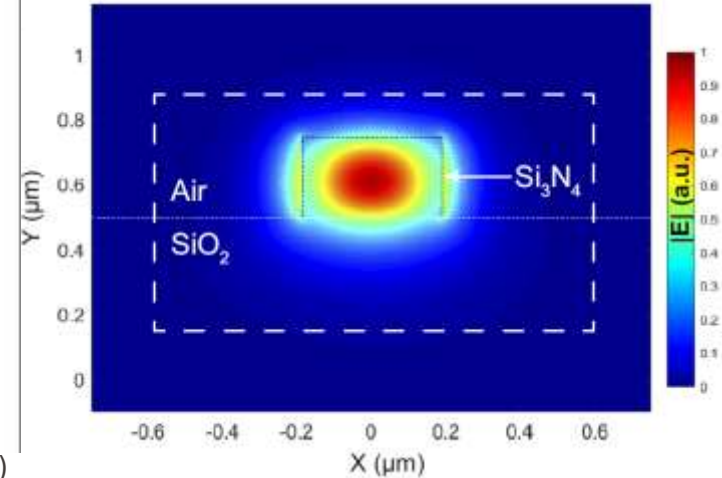
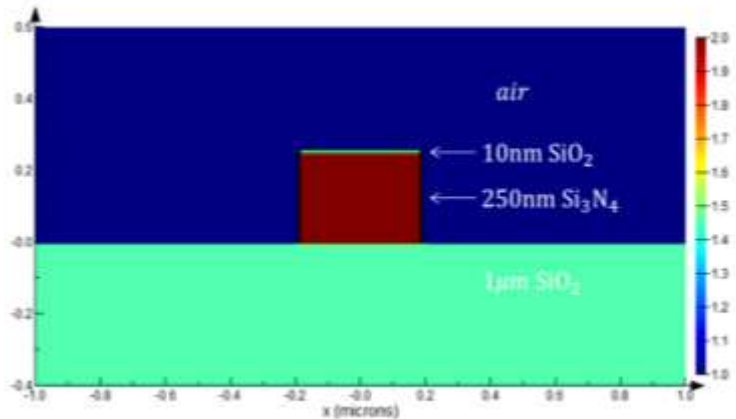
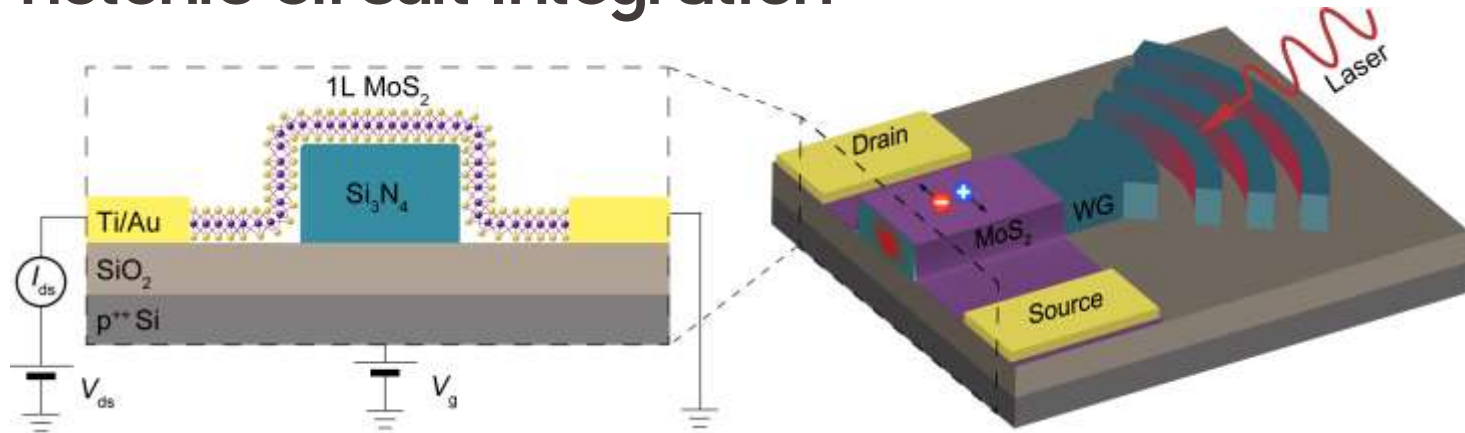
# Photocurrent Dynamics



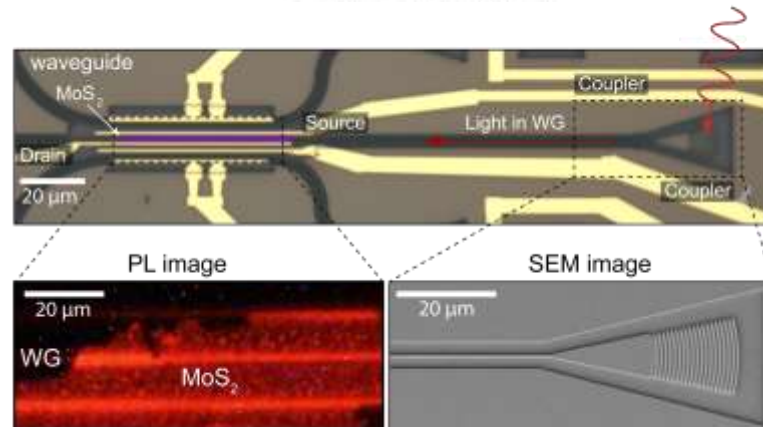
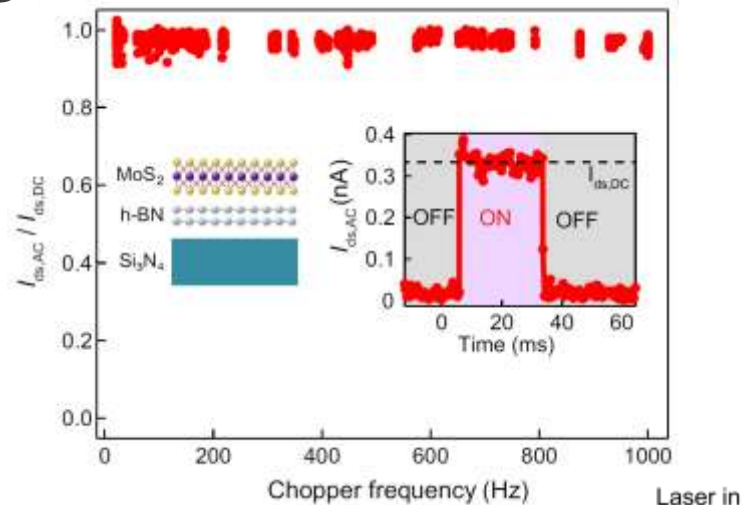
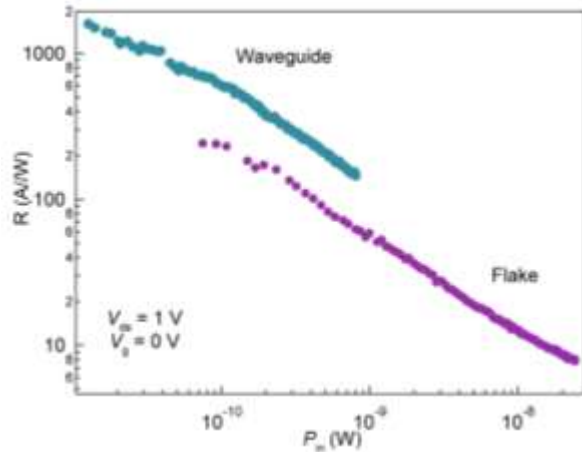
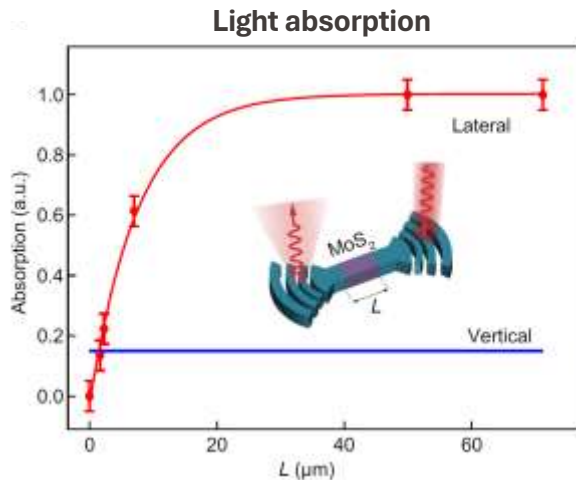
Lopez-Sanchez, Nature Nanotechnology (2013)



Furchi et al. Nano Lett. (2014)



# Integrated Photodetectors



# MoS<sub>2</sub> Photodetector Benchmarking

Technology	Material	Band Gap (eV)	Responsivity (A/W)	NEP (W/√Hz)
Silicon PIN Photodiode	Si	1.12	0.5-0.7	10 <sup>-14</sup> - 10 <sup>-15</sup>
InGaAs PIN Photodiode	In <sub>0.53</sub> Ga <sub>0.47</sub> As	0.75	0.8-1.0	10 <sup>-14</sup> - 10 <sup>-15</sup>
Germanium Photodiode	Ge	0.67	0.5-0.7	10 <sup>-13</sup> - 10 <sup>-14</sup>
Silicon APD	Si	1.12	50-130	10 <sup>-15</sup> - 10 <sup>-16</sup>
MoS <sub>2</sub>	MoS <sub>2</sub>	1.8	880	10 <sup>-15</sup>
PMT (Photomultiplier Tube)	Various	N/A	10 <sup>5</sup> - 10 <sup>7</sup> A/W	10 <sup>-17</sup> - 10 <sup>-18</sup>
Quantum Dot	PbS or PbSe	0.37 or 0.27	0.3-0.5	10 <sup>-12</sup> - 10 <sup>-13</sup>
Graphene	Graphene	0	0.1-0.5	10 <sup>-12</sup> - 10 <sup>-13</sup>
MCT (Mercury Cadmium Telluride)	Hg <sub>1-x</sub> Cd <sub>x</sub> Te	0.1-1.5	2-20	10 <sup>-11</sup> - 10 <sup>-12</sup>

Compiled using perplexity.ai

# Today: 1024 Transistors on a Chip

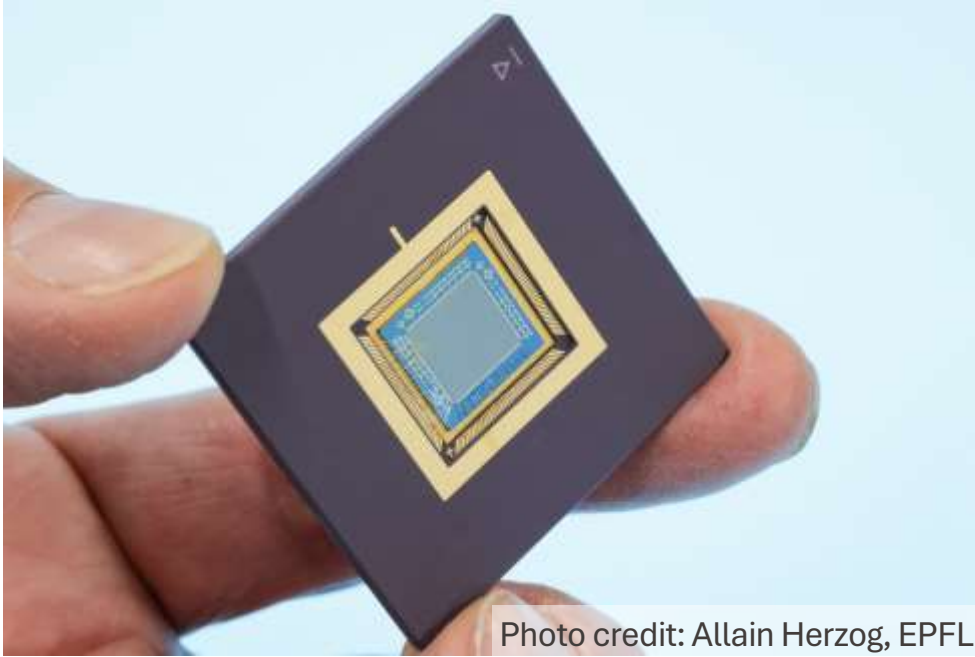
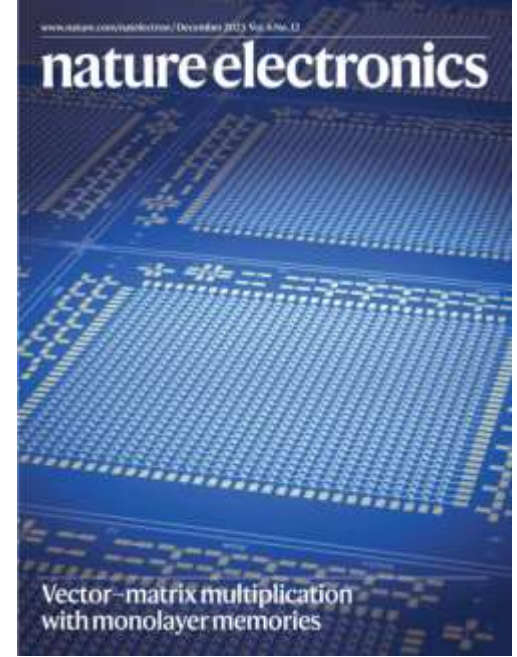


Photo credit: Allain Herzog, EPFL



Marega...Kis, Nature Electronics (2023)



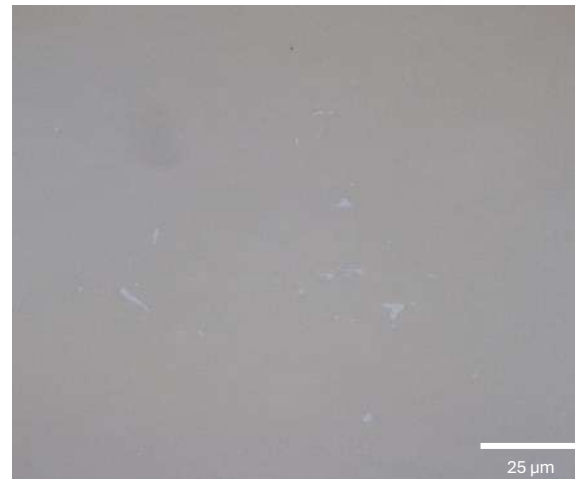
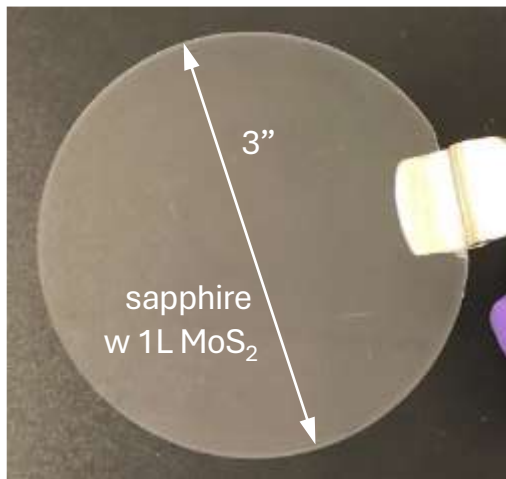
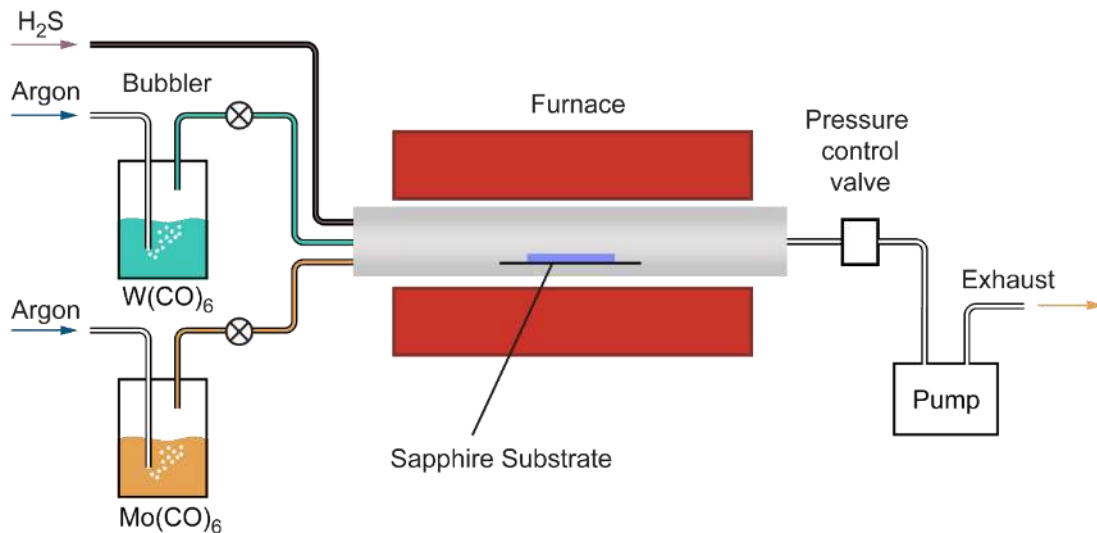
# MOCVD Growth

Metalorganic chemical  
vapour deposition

Cun, Kis, Radenovic et al. (2019)

Large single crystals  
EPFL, Kim...Kis, Nano Lett ( 2017)

$$\mu \approx 50 \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$$



# IRDS - International Roadmap for Devices and Systems

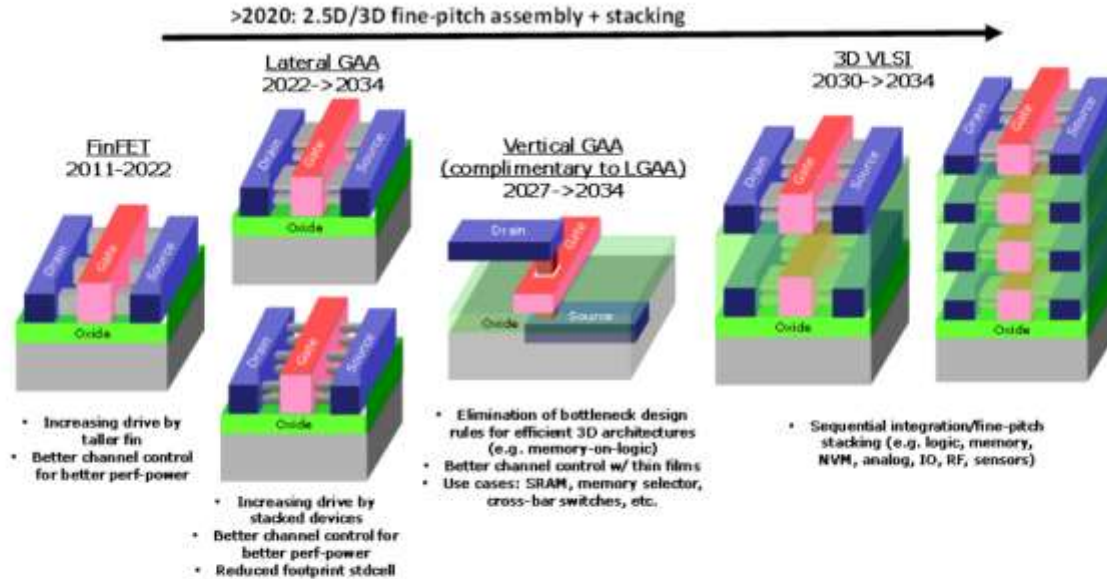


Figure ES48

Change in the MOSFET device architecture from the 2D planar through 2.5D FinFets to 3D monolithic VLSI with GAA

<https://irds.ieee.org/editions/2021/executive-summary>

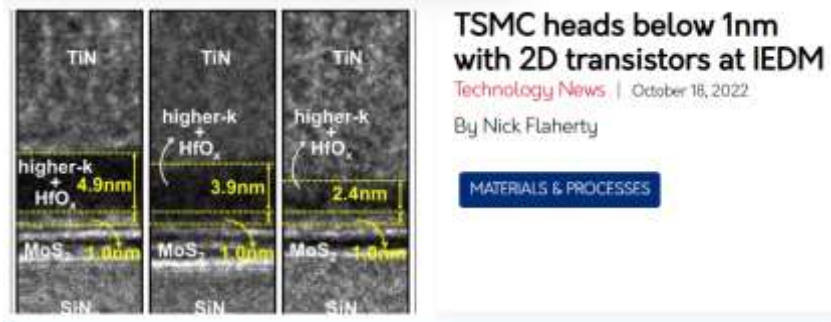
# IRDS - International Roadmap for Devices and Systems

YEAR OF PRODUCTION	2021	2022	2025	2028	2031	2034
	G51M30	G48M24	G45M20	G42M16	G40M16/T2	G38M16/T4
Logic industry "Node Range" Labeling (nm)	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	I7-I5	I5-I3	I3-I2.1	I2.1-I1.5	I1.5e-I1.0e	I1.0e-I0.7e
Logic device structure options	FinFET	finFET LGAA	LGAA	LGAA	LGAA-3D	LGAA-3D
Platform device for logic	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
Frequency scaling - node-to-node	-	0.02	0.16	0.09	-0.08	-0.01
CPU frequency at constant power density (GHz)	3.13	2.83	3.53	2.50	1.48	0.86
Power at iso frequency - node-to-node	-	-0.16	-0.27	-0.05	-0.06	-0.08
Power density - relative	1.00	1.12	1.04	1.59	2.51	4.27
<b>LOGIC TECHNOLOGY ANCHORS</b>						
Patterning technology inflection for Mx interconnect	193i, EUV DP	193i, EUV DP	193i, EUV DP	193i, High-NA EUV	193i, High-NA EUV	193i, High-NA EUV
Beyond-CMOS as complimentary to platform CMOS	-	-	-	2D Device, FeFET	2D Device, FeFET	2D Device, FeFET
Channel material technology inflection	SiGe25%	SiGe50%	SiGe50%	Ge, 2D Mat	Ge, 2D Mat	Ge, 2D Mat
Process technology inflection	Conformal Doping, Contact	Channel, RMG	Lateral/Atomic Etch	Non-Cu Mx	3DVLSI	3DVLSI
Stacking generation inflection	2D	3D-stacking: W2W, D2W Mem-on-Logic	3D-stacking: W2W, D2W Mem-on-Logic	3D-stacking, Fine-pitch stacking, P-over-N, Mem-on-Logic	3D-stacking, 3DVLSI: Mem-on-Logic with Interconnect	3D-stacking, 3DVLSI: Logic-on-Logic

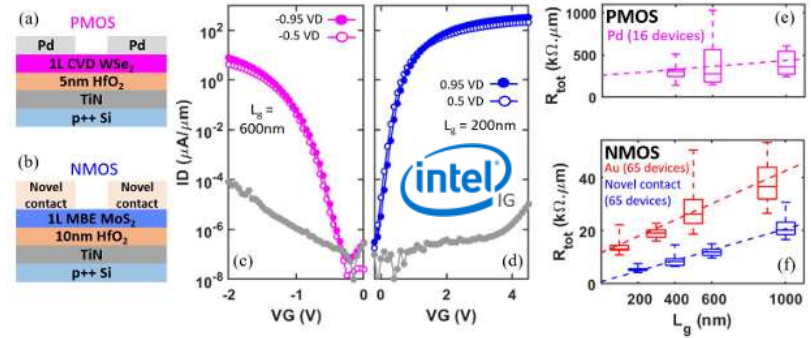
Figure ES9

*Devices will continue to aggressively scale in the next 5 years*

<https://irds.ieee.org/editions/2021/executive-summary>



<https://www.eenewseurope.com/en/tsmc-heads-below-1nm-with-2d-transistors-at-iedm/>



[INTEL, IEEE TED (2021), doi:10.1109/TED.2021.3118659]



## First Demonstration of GAA Monolayer-MoS<sub>2</sub> Nanosheet nFET with 410 $\mu\text{A}/\mu\text{m}$ $I_{\text{D}}$ at 1V $V_{\text{D}}$ at 40nm gate length

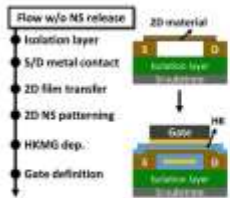


Fig. 19. Process flow and schematic of single 2D NS device without sheet release.

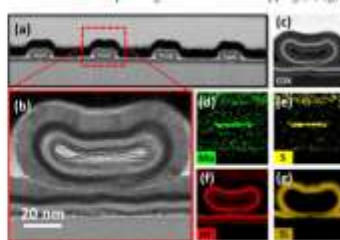


Fig. 20. TEM cross section of (a) and (b) monolayer MoS<sub>2</sub> nanosheet device with gate stack fully wrapped around the channel. Corresponding EDX elemental mapping (c)-(d).

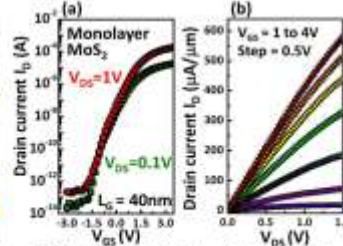
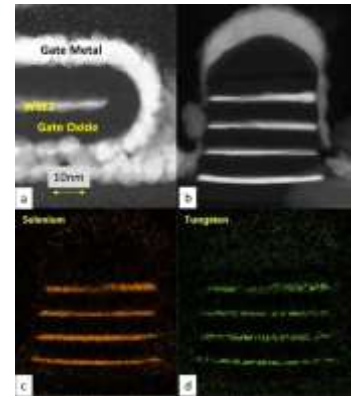


Fig. 21. (a)  $I_{\text{D}}-V_{\text{GS}}$  and (b)  $I_{\text{D}}-V_{\text{GS}}$  device characteristics of monolayer MoS<sub>2</sub> NSFET with  $L_{\text{g}}=40\text{nm}$ .

## Process integration and future outlook of 2D transistors

Kevin F. O'Brien, Carl H. Naylar, Chelsea Greene, Kirby Massey, Ashish Venka Penumatcha, Anshu Vyasiah, Ying Zhang, Anshu Kulkarni, Sudant Lim, Carly Bagan, Walter Markiewicz, Mahesh Sankar Kavali, Sachin Srinivasan, Pradyumn Bangarath, Souvik Dutta, Tamas Tamas, Sanku Chandraharan, Paul Fischer, Eryoseh H. Pinn, Mehdi Radouaninejad, Matt Metz & Ugyar Arci

nature communications



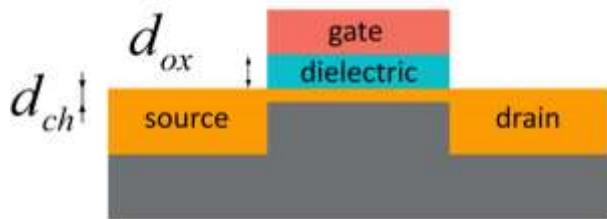
[INTEL, Nature Comm. (2023), DOI: 10.1038/s41467-023-41779-5]

[TSMC, IEDM (2022), doi:10.1109/IEDM45625.2022.10019563]

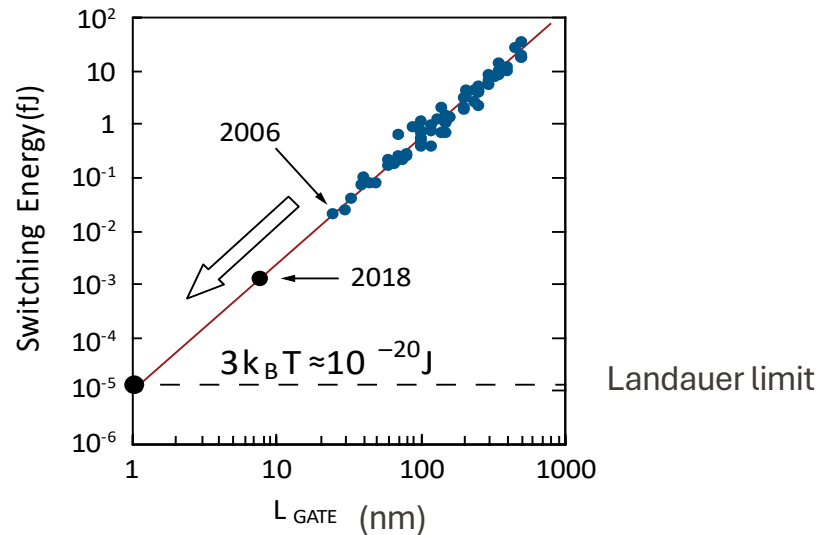
# IT Energy Problem



[http://www.phys.ncku.edu.tw/~htsu/humor/fry\\_egg.html](http://www.phys.ncku.edu.tw/~htsu/humor/fry_egg.html)



## Single device:



Cavin et al. J Nanopart Res (2006)

## System level:

Intel Core i7 8700K processor (2017)

**$10^9 \times$  worse!** (2.5 GFLOPS/W)

Frontier supercomputer (ORNL, 2022)

**$4 \cdot 10^7 \times$  worse** (62.68 GFLOPS/W)

A100 40 GB (NVIDIA, 2023)

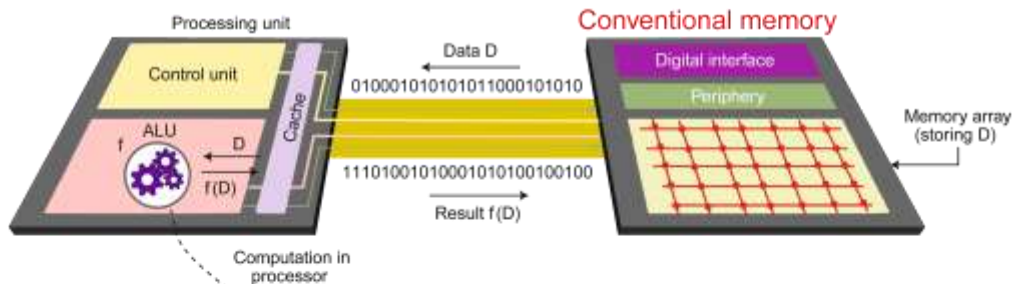
**$3.7 \cdot 10^7 \times$  worse** (78 GFLOPS/W)



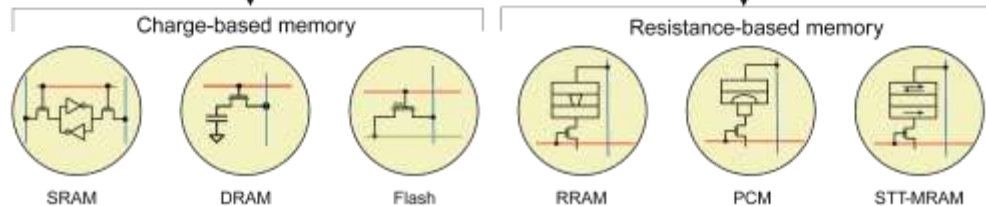
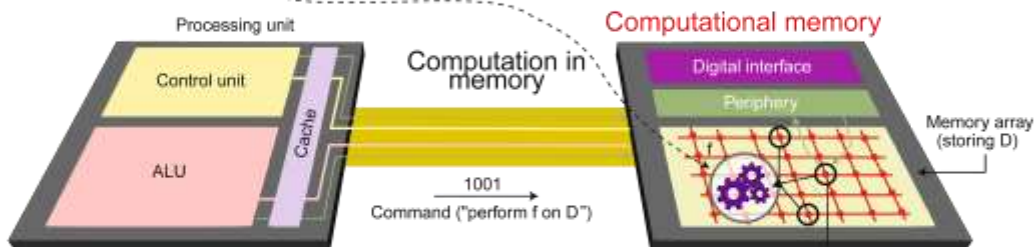
John von Neumann

# Logic in Memory

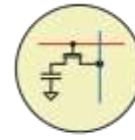
Von Neumann



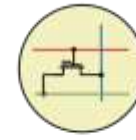
Logic in memory



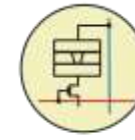
Sebastian...Eleftheriou, Nat. Nanotech. (2020)



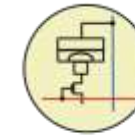
DRAM



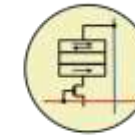
Flash



RRAM



PCM



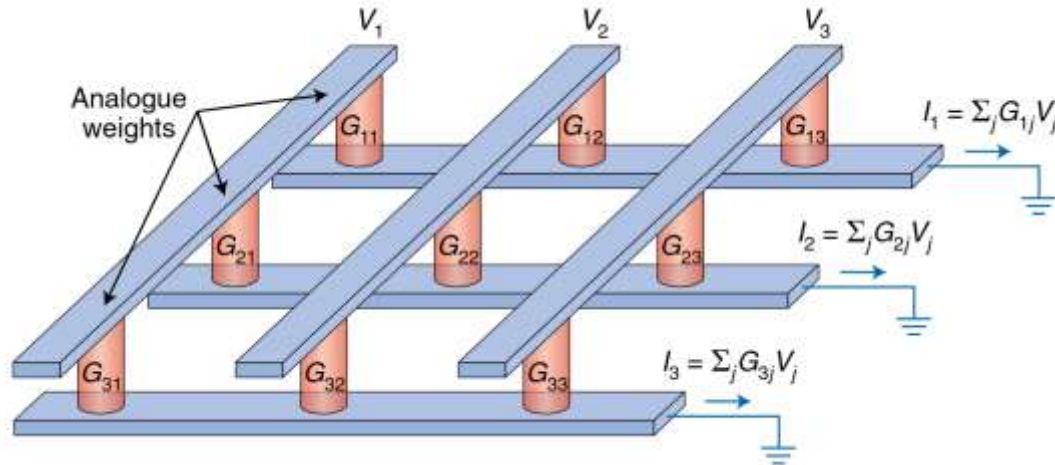
STT-MRAM

Sebastian...Eleftheriou, Nat. Nanotech. (2020)

Performance metrics	DRAM	Flash	PCM	STT-MRAM	RRAM	HDD
Feature size (nm)	36	22	45	95	9	NA
Cell Area	$6F^2$	$4F^2$	$4F^2$	$4F^2$	$4F^2$	$\sim 256^*$
Write/Erase Time	< 10ns	1/0.1ms	100ns	<10ms	<1ns	5ms
Retention	64ms	>10y	>10y	>10y	>10y	>10y
Endurance	>1E16	1E4	1E9	>1E12	1E12	>1E16
Nonvolatility	N	Y	Y	Y	Y	Y
Multi-level capability	N	Y	Y	N	Y	-
Write Energy (J/bit)	4E-15	> 2E-16	1E-12	2.5E-12	1E-13	-
Standby Power (W/Gb)	1E-1	1E-3	1E-3	1E-3	1E-3	110

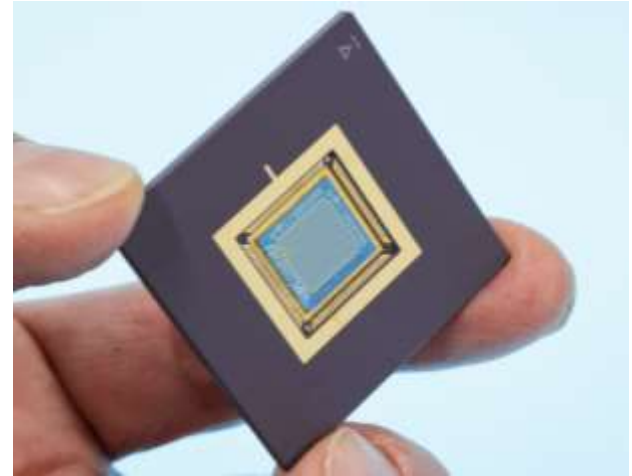
Credit: G. M. Marega

# Vector Matrix Multiplication



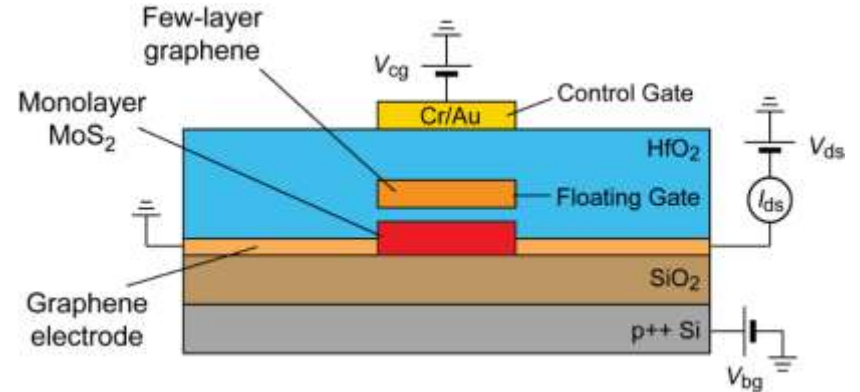
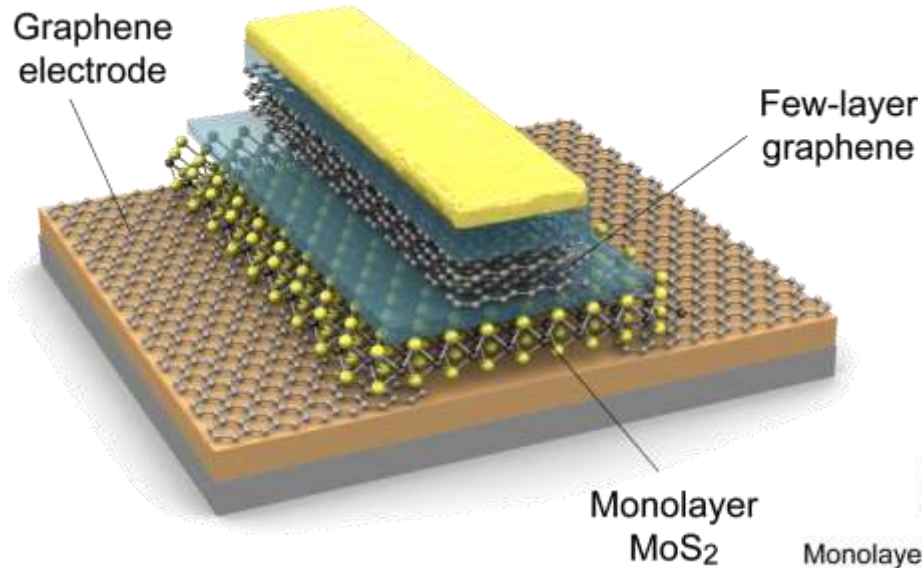
$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} & G_{13} \\ G_{21} & G_{22} & G_{23} \\ G_{31} & G_{32} & G_{33} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

Ielmini and Wong, Nat. Electron. (2018)



Marega...Kis, Nature Electronics, 2023.



Flash Memory with  $\text{MoS}_2$ 

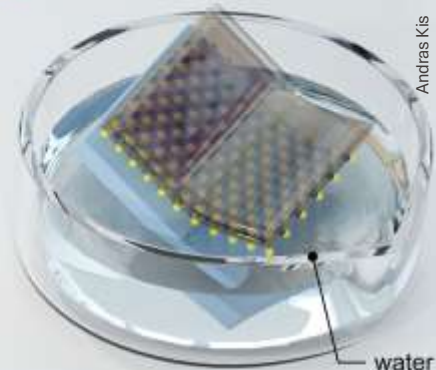
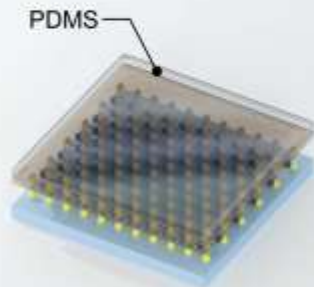
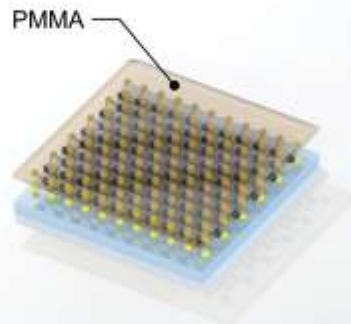
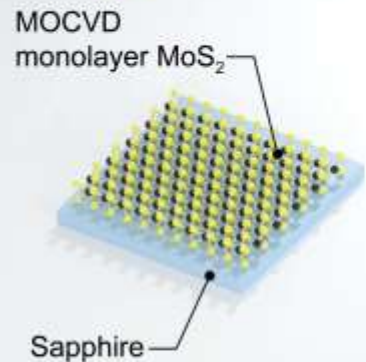
Bertolazzi...Kis; ACS Nano (2013)

1 Growth

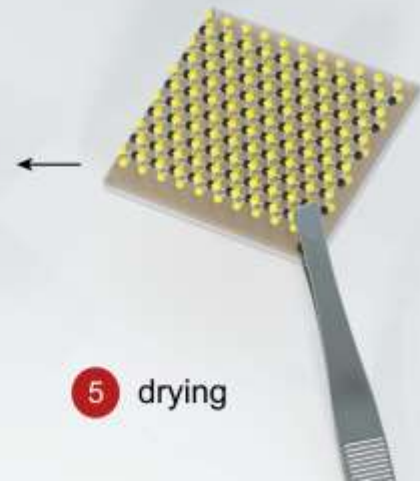
2 sacrificial polymer

3 stamp application

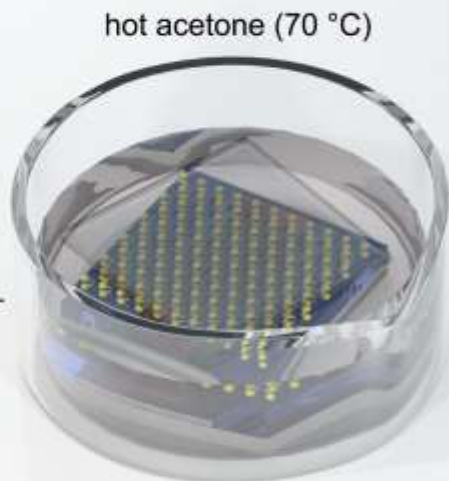
4 water intercalation, peel-off



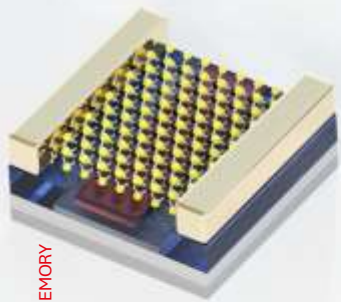
Andras Kis



5 drying

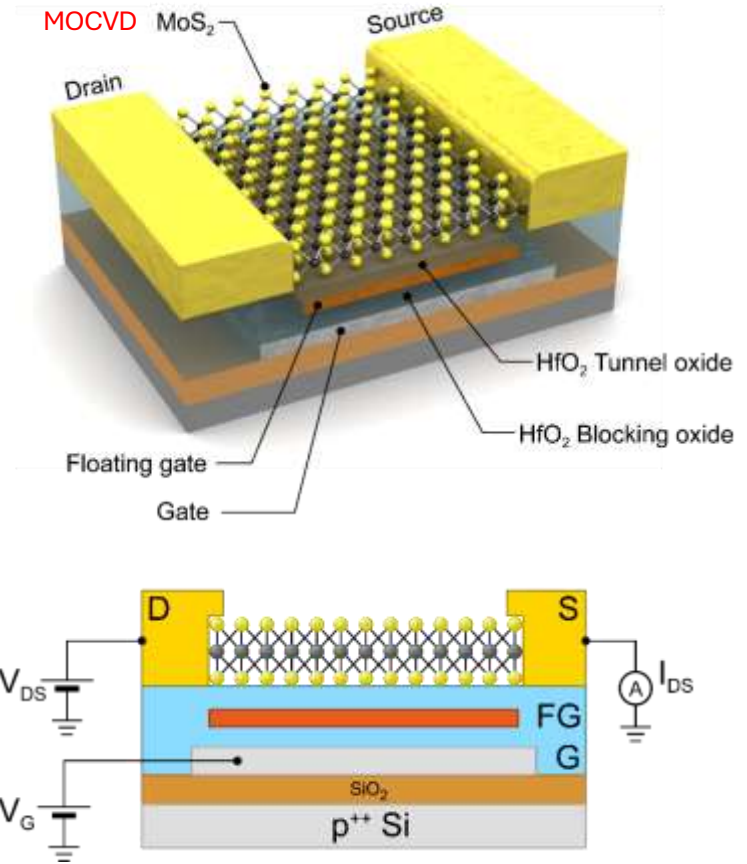
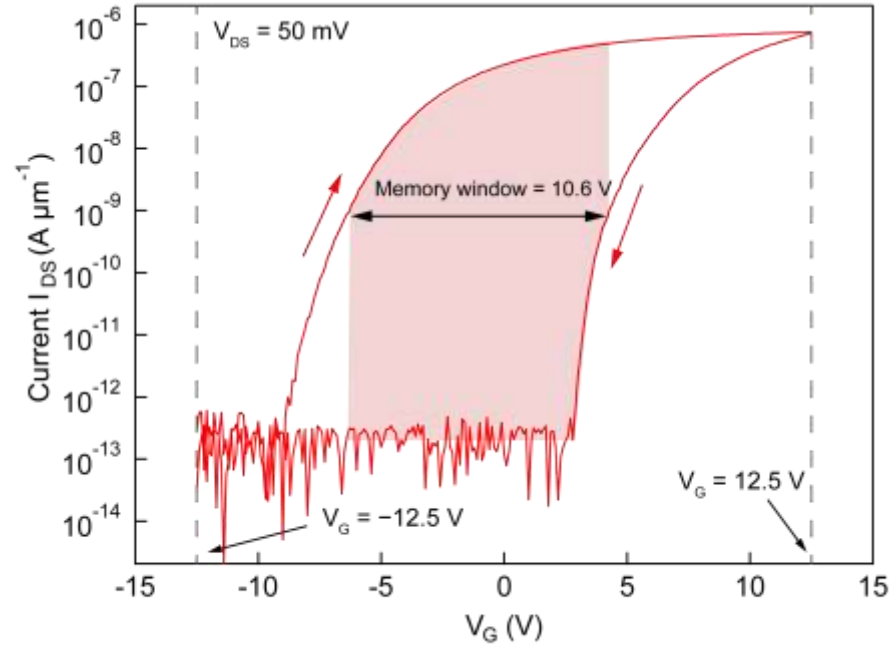


6 transfer



7 contact fabrication

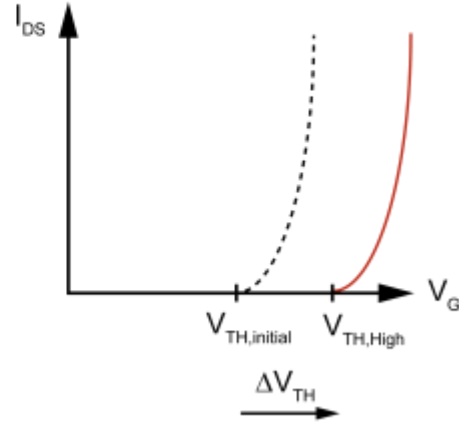
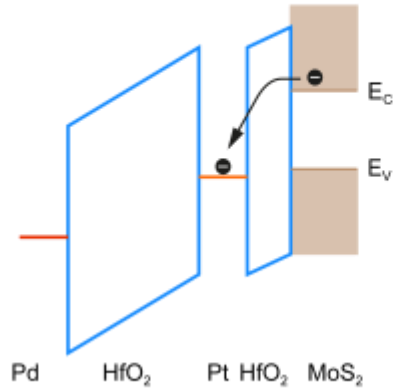
© IN MEMORY



Marega...Kis; Nature (2020)

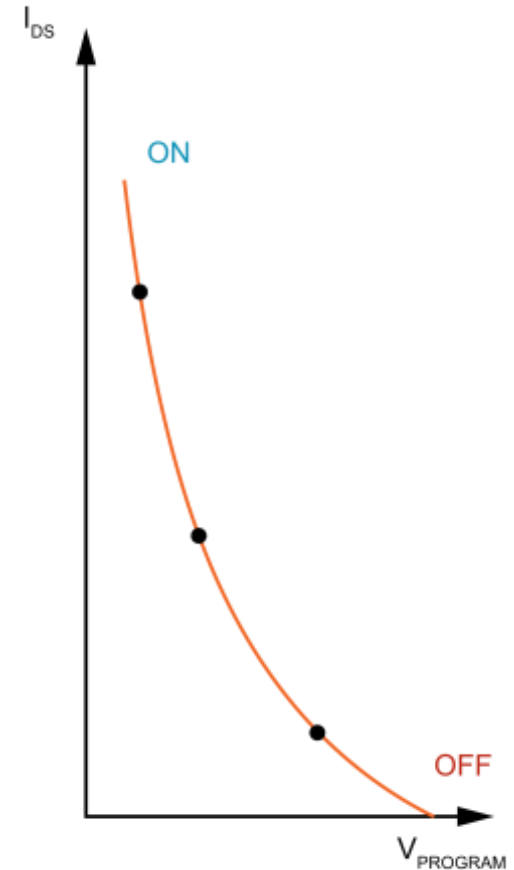
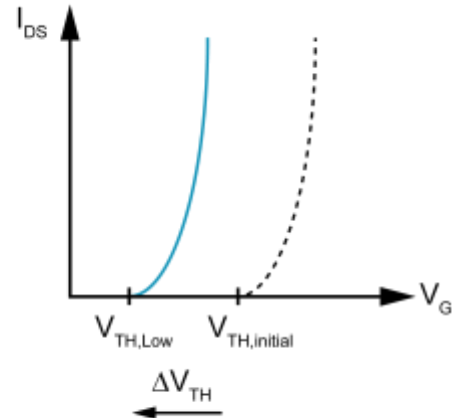
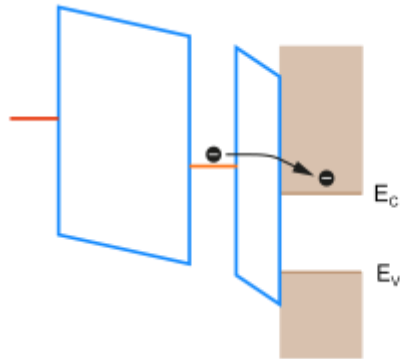
Program

$V_G > 0$

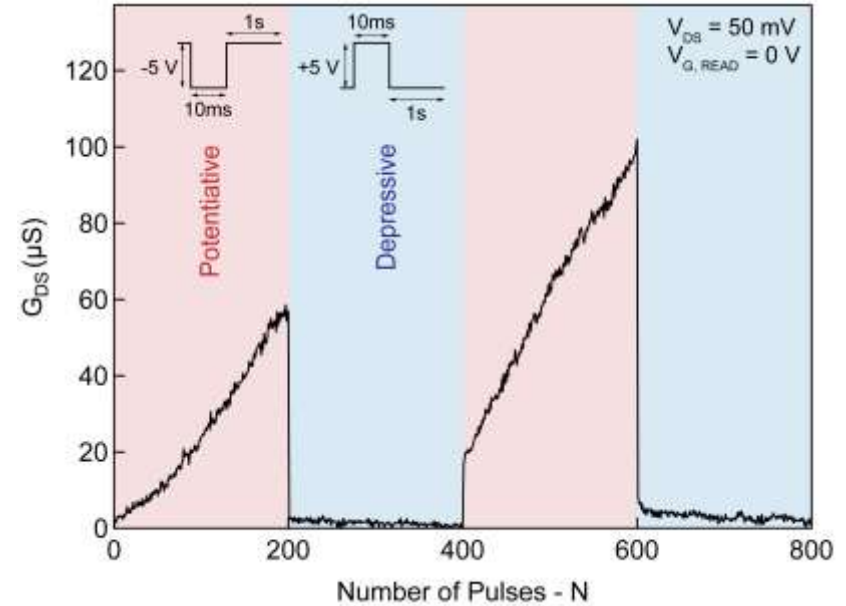
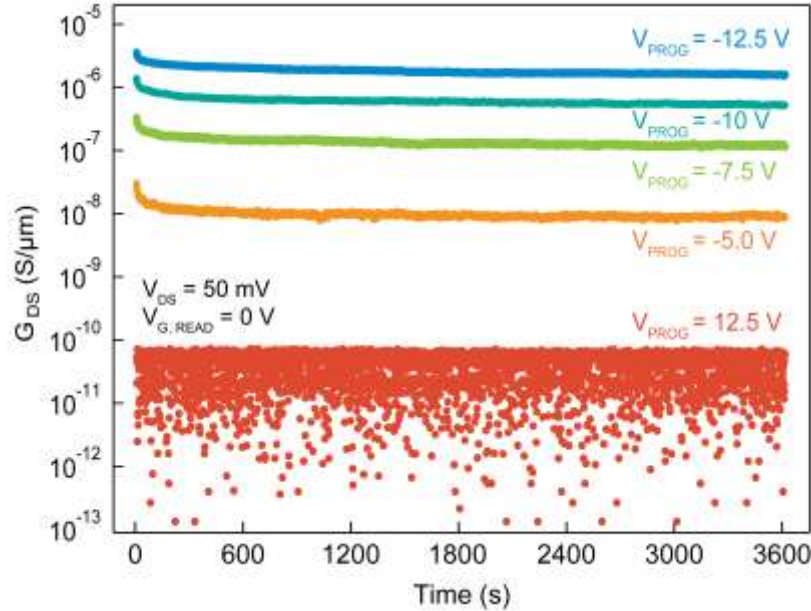


Erase

$V_G < 0$

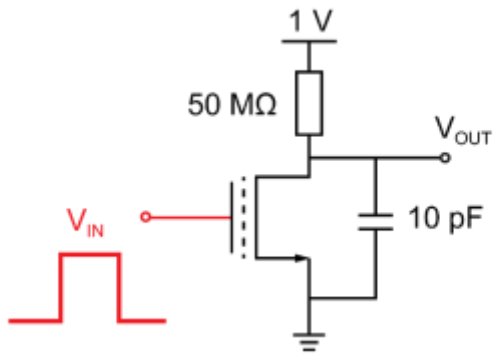


Intermediate states



2-state retention >10 years  
Endurance: 60,000 program/erase cycles

# Programmable Inverter

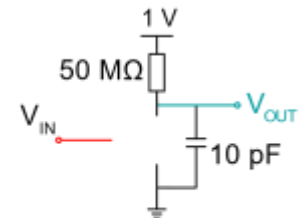


Q	IN	X <sup>(Q)</sup>
1	0	0
2	0	1
3	0	1

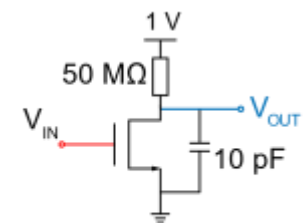
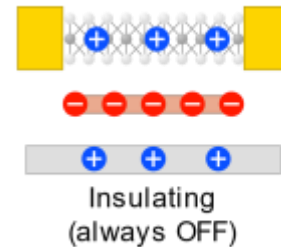
Logic input and memory states

X <sup>(Q)</sup>	OUT
0	1
1	0

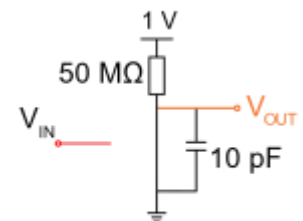
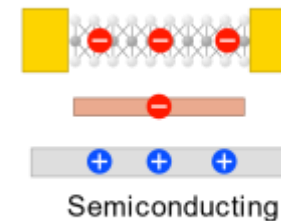
Memory states and logic output



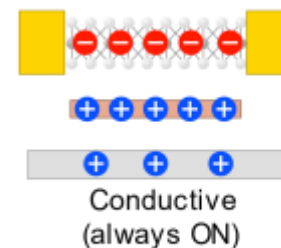
Q = 1 : memory state 0



Q = 2 : memory state 0 OR 1

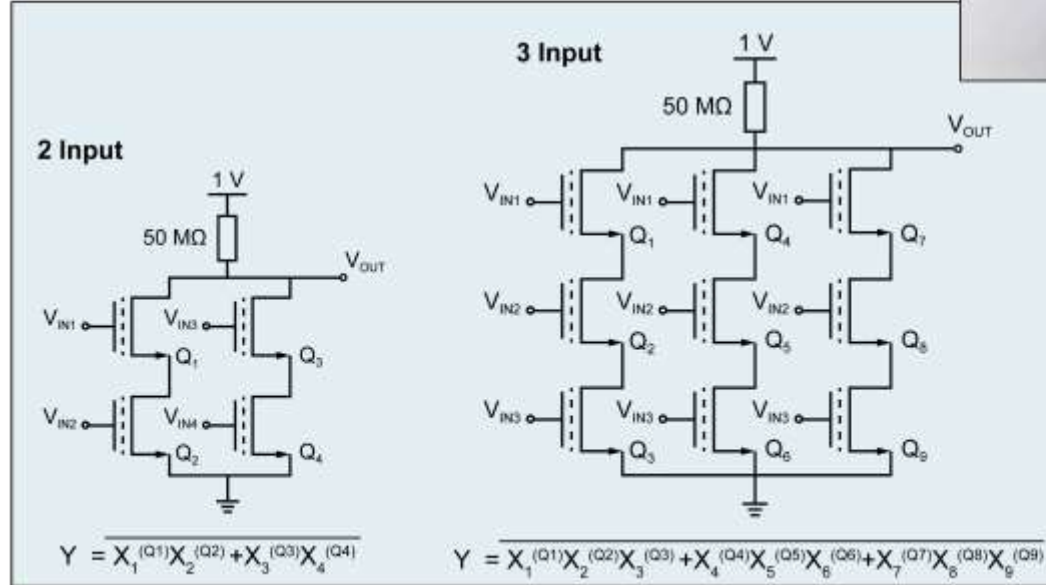
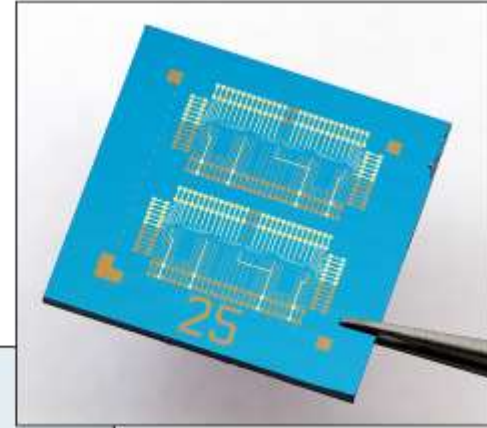


Q = 3 : memory state 1



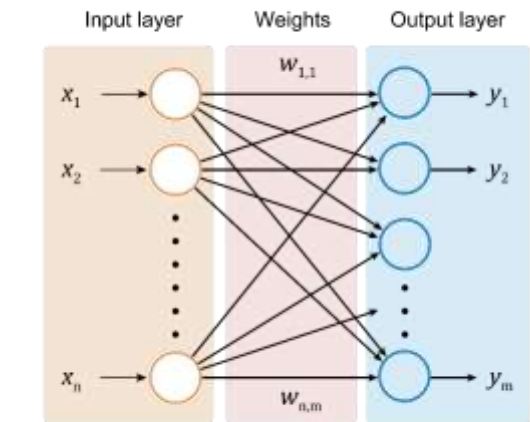
# Universal Logic Gate

12 mm × 12 mm die  
80 memory devices

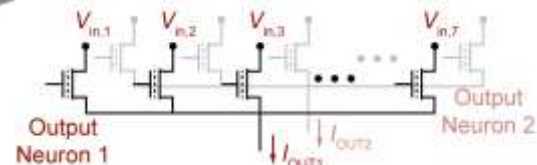
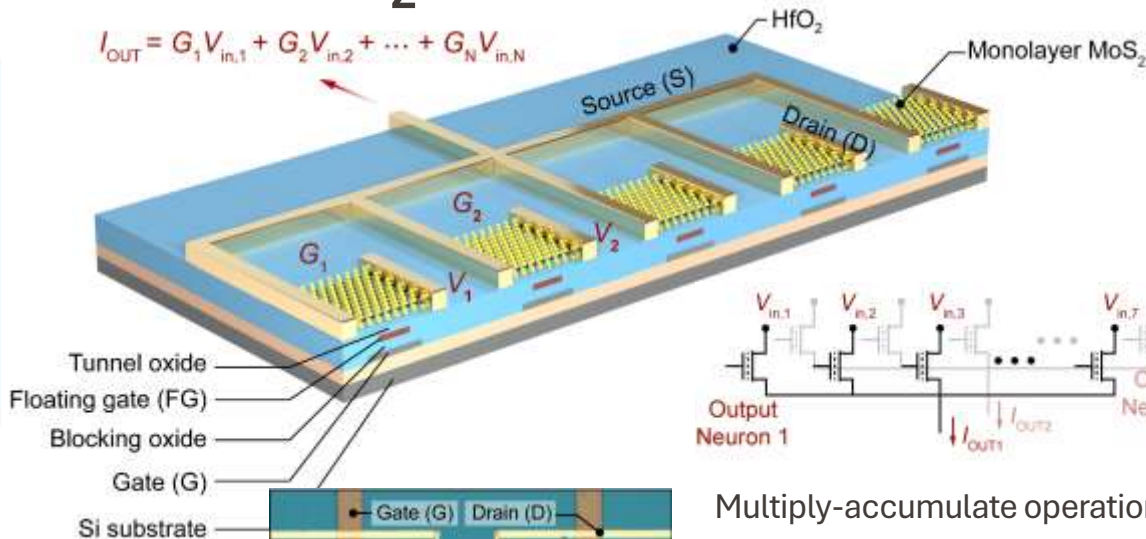


Marega...Kis; Nature (2020)

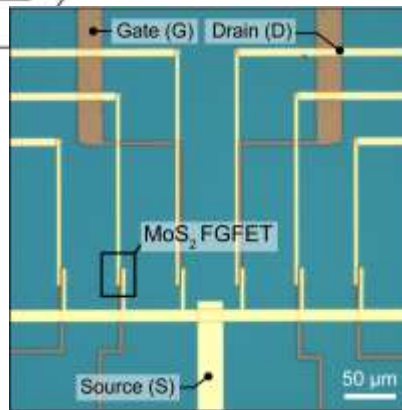
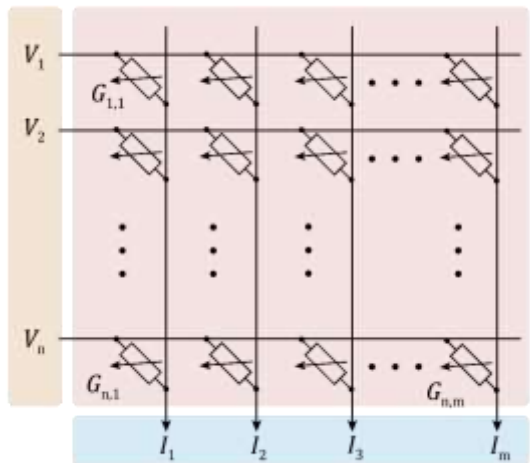
# Neural Networks with MoS<sub>2</sub>



$$I_{OUT} = G_1 V_{in,1} + G_2 V_{in,2} + \dots + G_N V_{in,N}$$



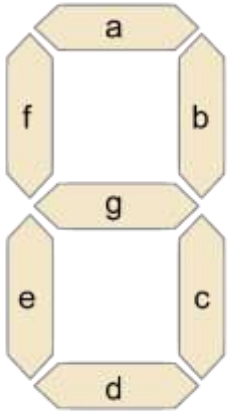
Multiply-accumulate operations



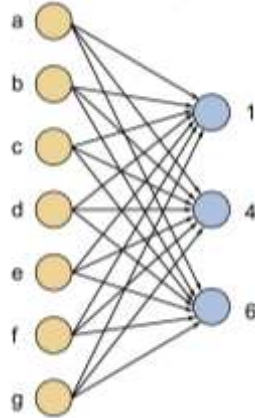
Marega...Kis; ACS Nano (2022)



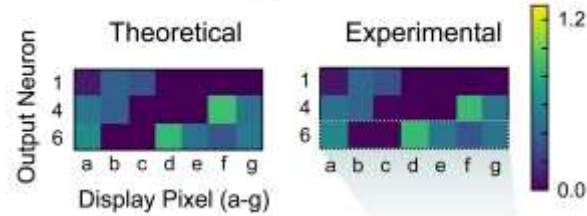
7-segment display



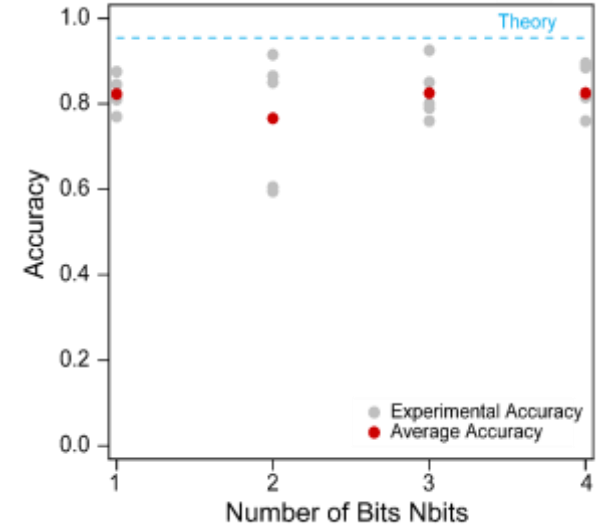
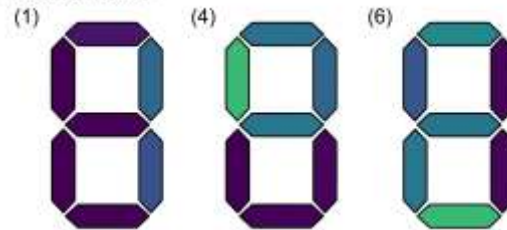
Perceptron layer



Weight Matrix



Feature Maps:

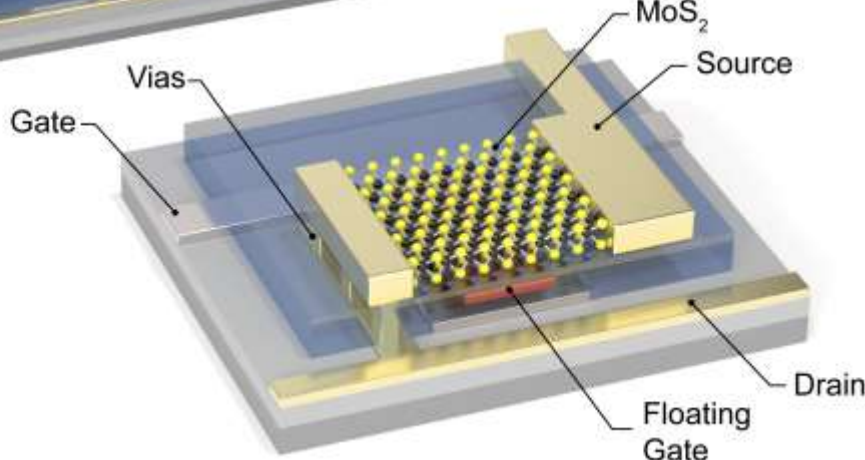
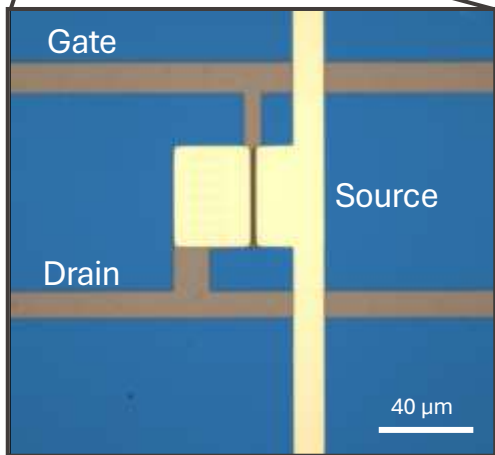
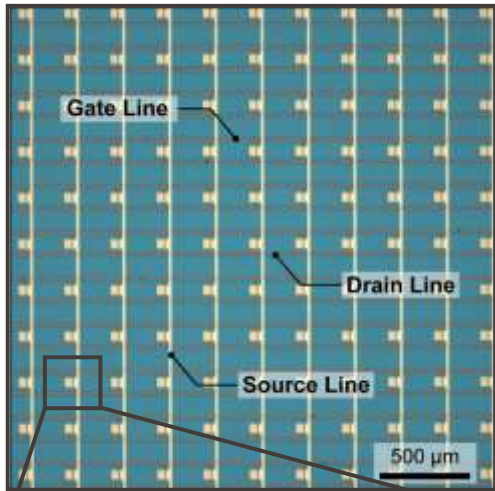
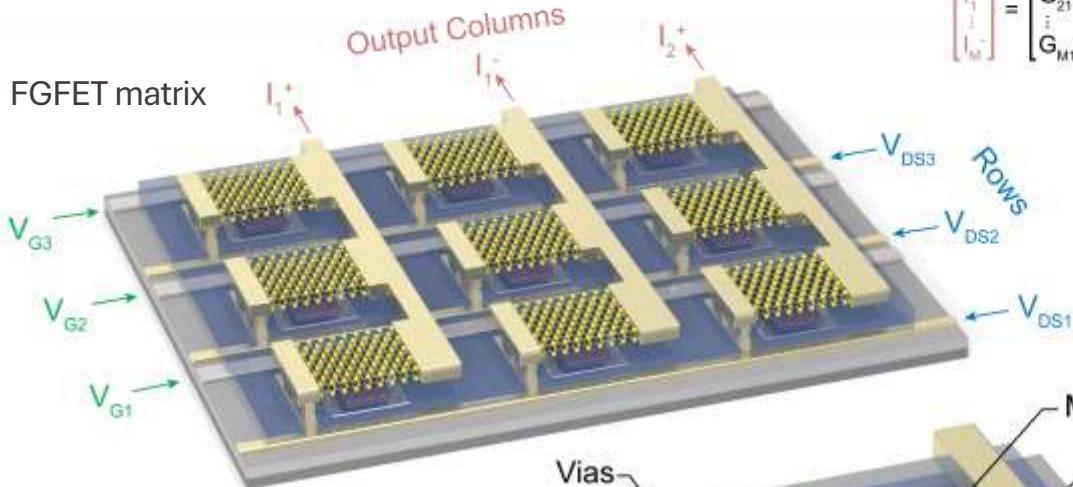


**Simulations: 38× energy advantage over CMOS - Giuseppe Iannaccone (U. of Pisa)**

# Large-scale Integration

Vector-Matrix Multiplication

$$\begin{bmatrix} I_1^+ \\ \vdots \\ I_M^+ \end{bmatrix} = \begin{bmatrix} G_{11} & G_{12} & \dots & G_{1N} \\ G_{21} & G_{22} & \dots & G_{2N} \\ \vdots & \vdots & \ddots & \vdots \\ G_{M1} & G_{M2} & \dots & G_{MN} \end{bmatrix} \cdot \begin{bmatrix} V_{DS1} \\ V_{DS2} \\ \vdots \\ V_{DS(N)} \end{bmatrix}$$



32×32 FGFET array  
1024 devices

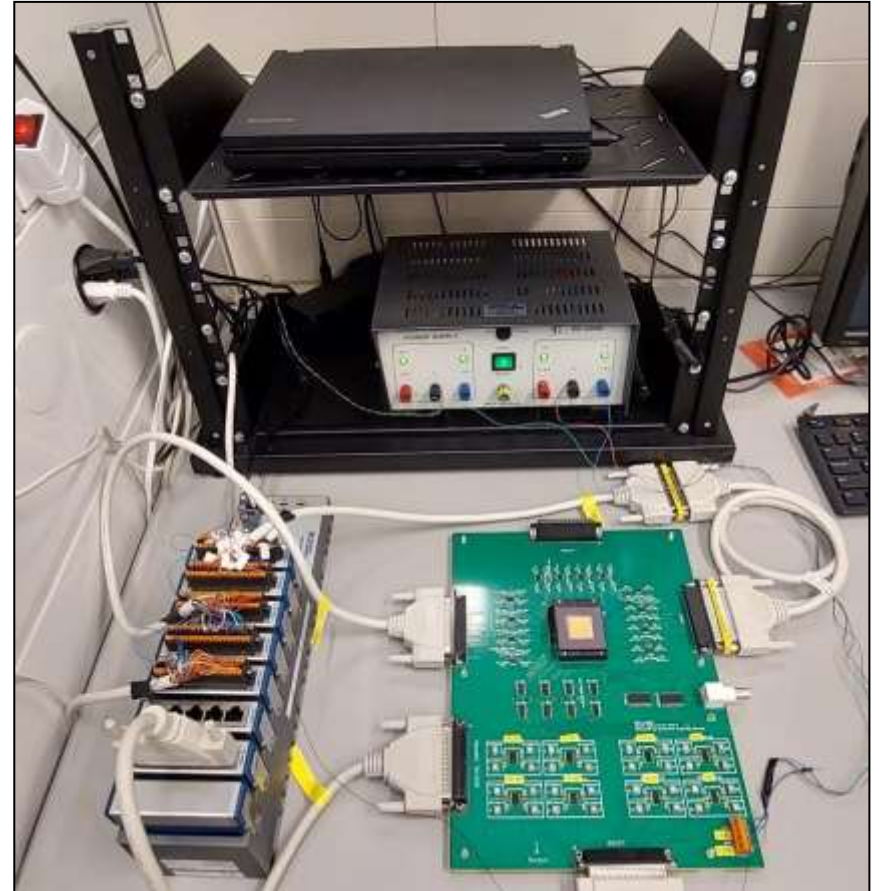
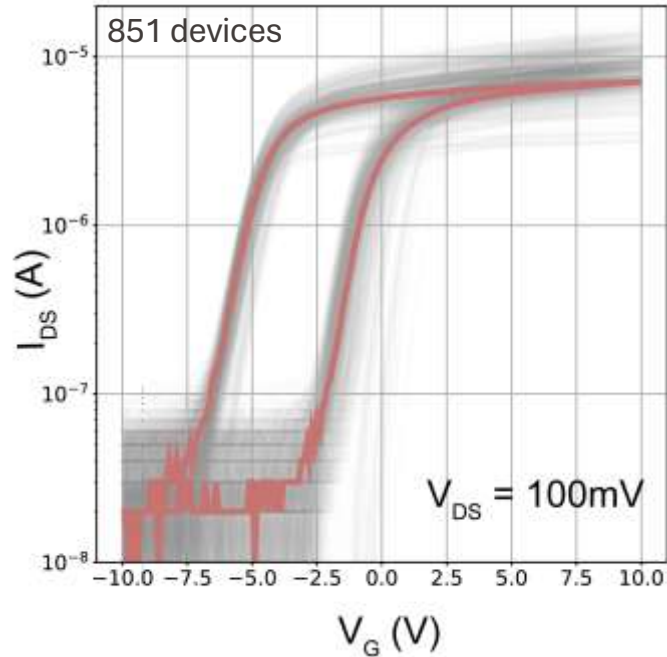
■ IN-MEMORY COMPUTING

Marega...Kis; Nat. El. (2023)

Floating-gate Field-effect Transistor

# Large-scale Integration

32×32 FGFET array  
1024 devices  
83% yield

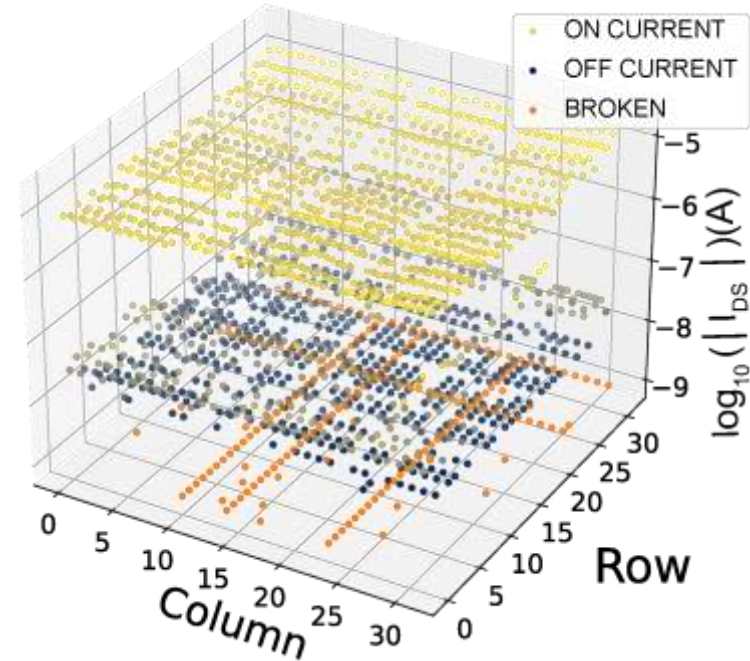
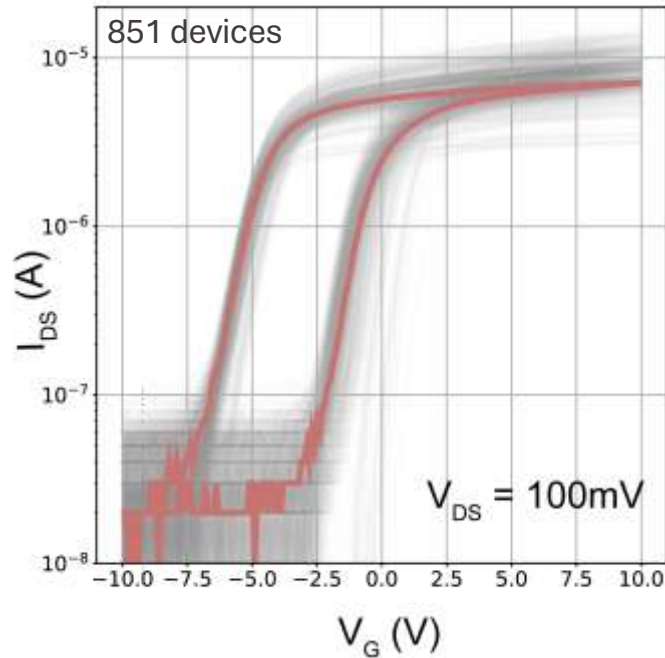


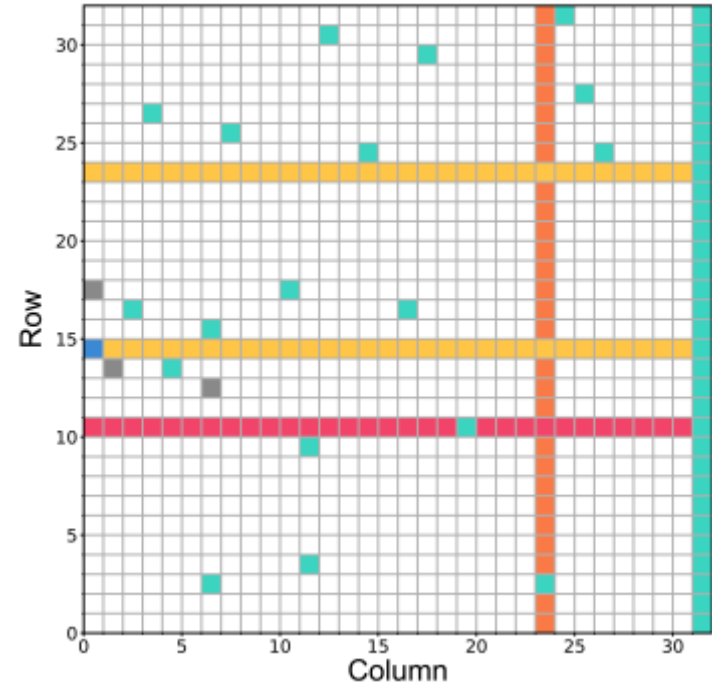
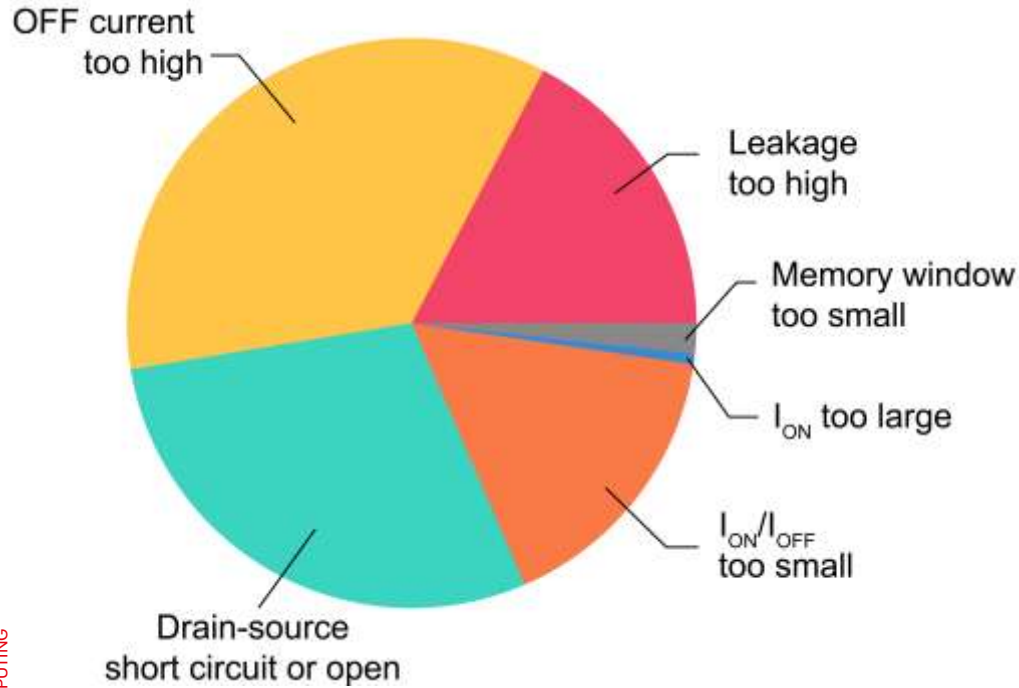
# Large-scale Integration

32×32 FGFET array

1024 devices

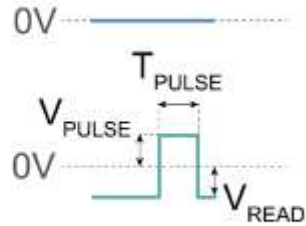
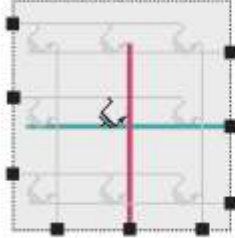
83% yield



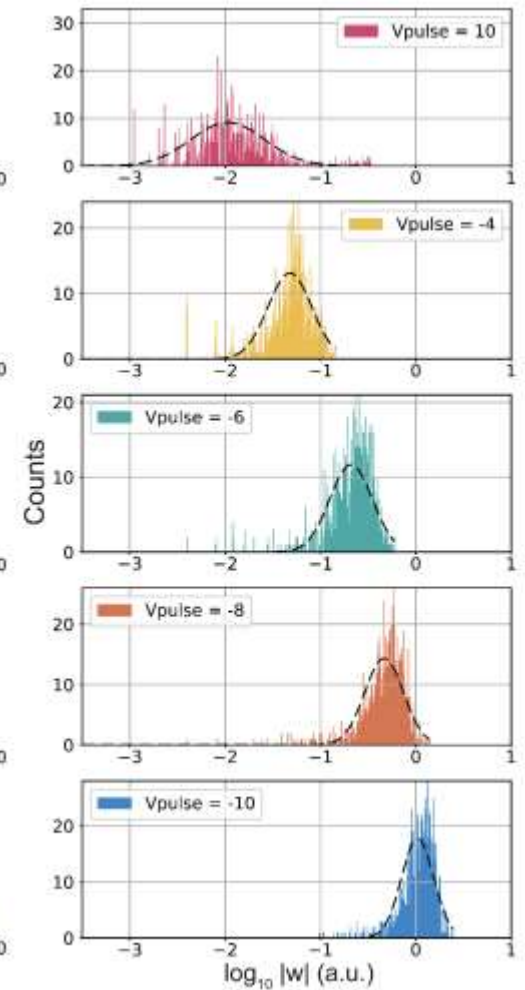
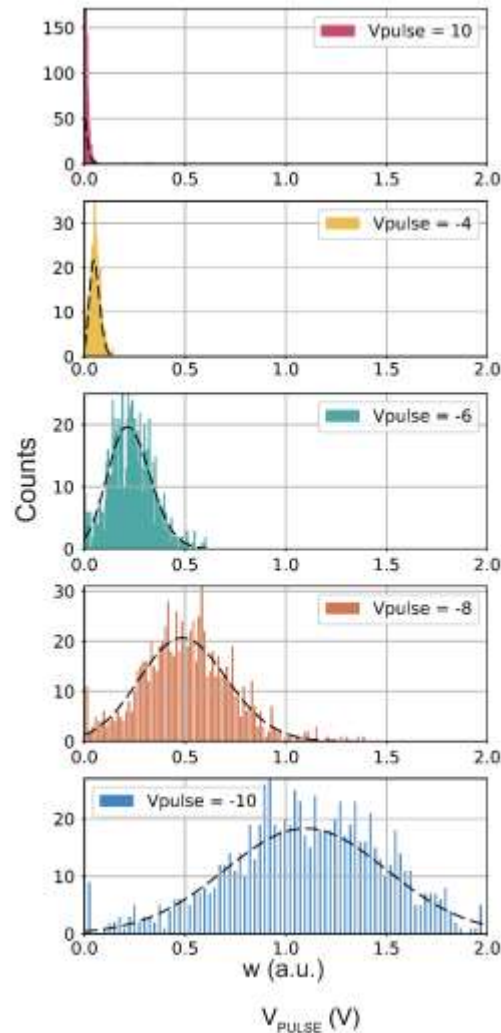
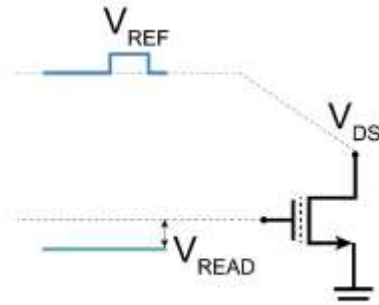
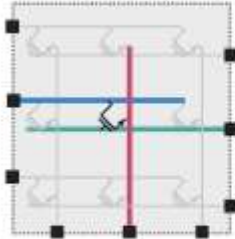


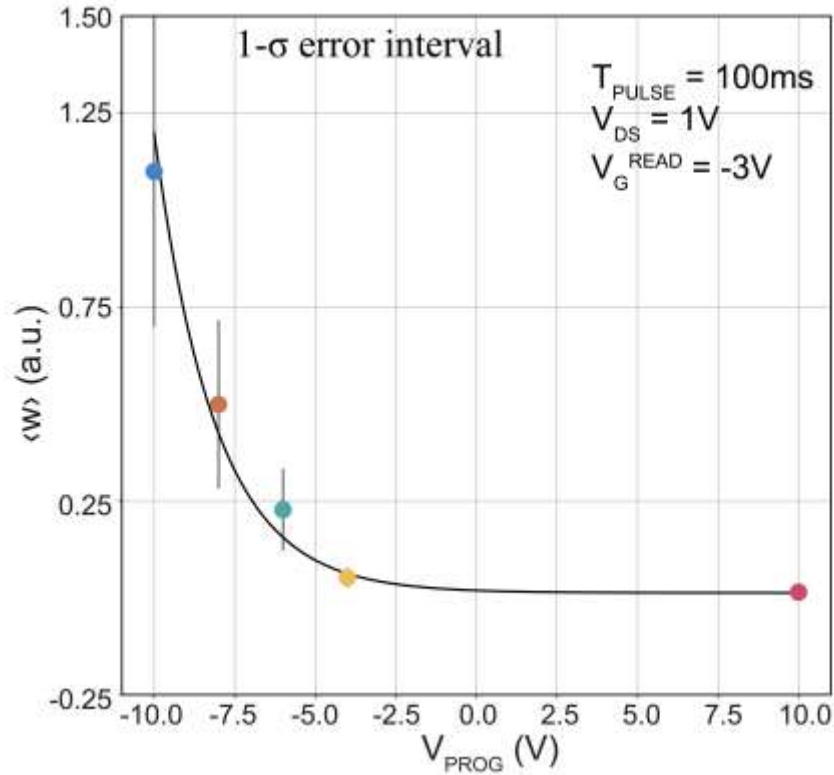
# Open-loop Programming

Programming



Readout



 $V_{\text{PULSE}}$  (V)

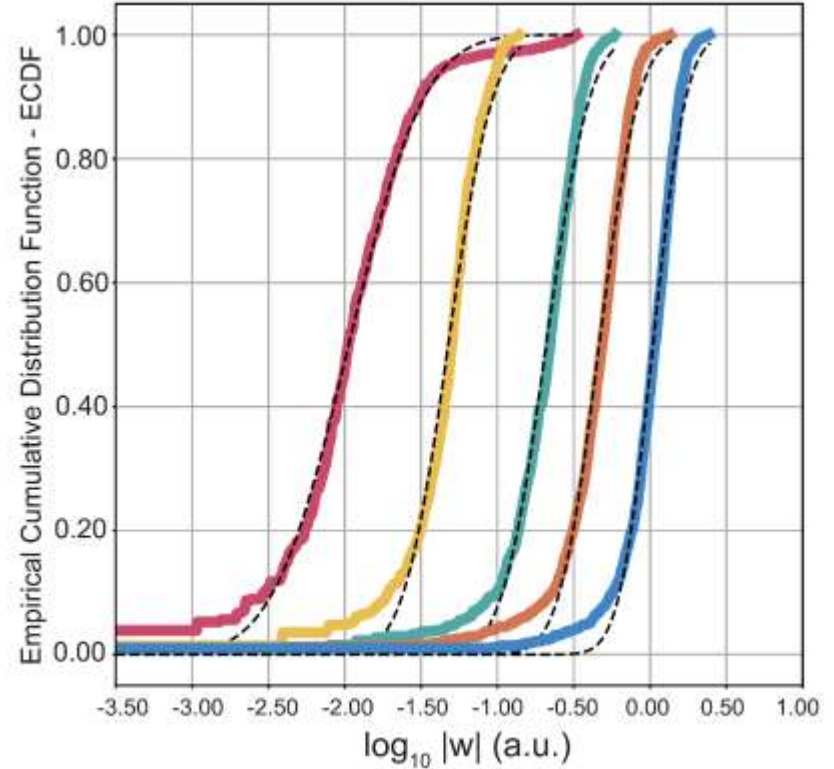
10V

-4V

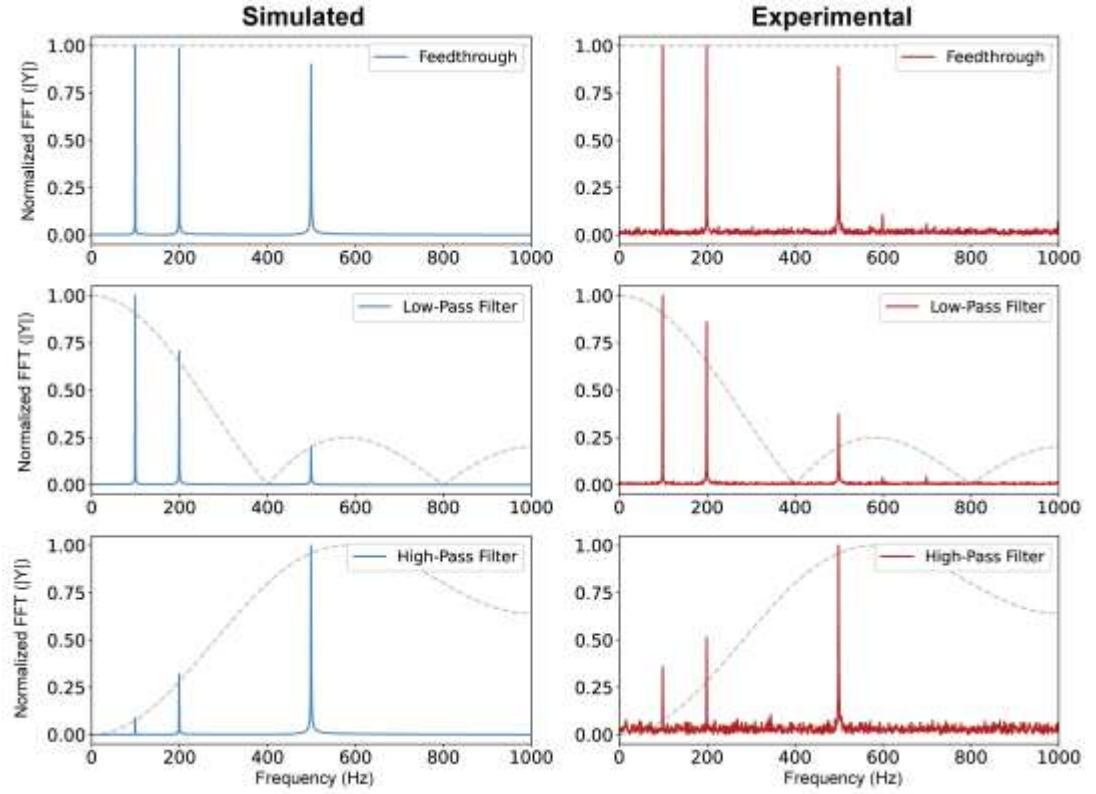
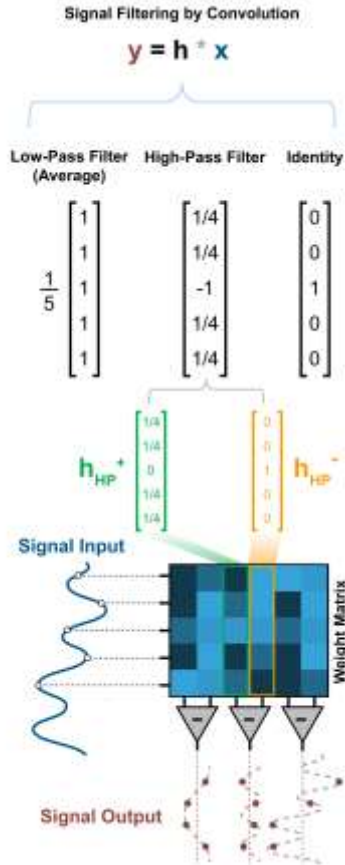
-6V

-8V

-10V



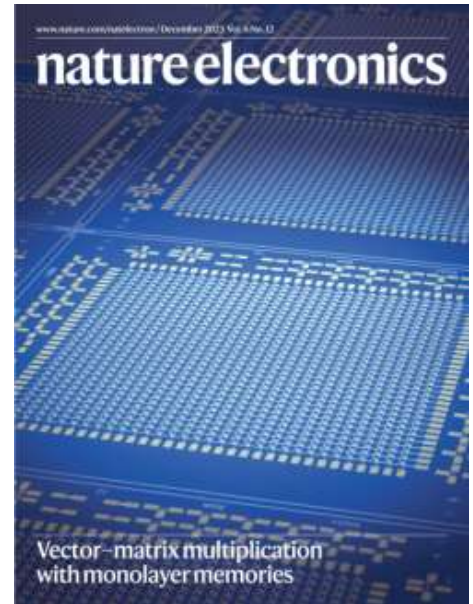
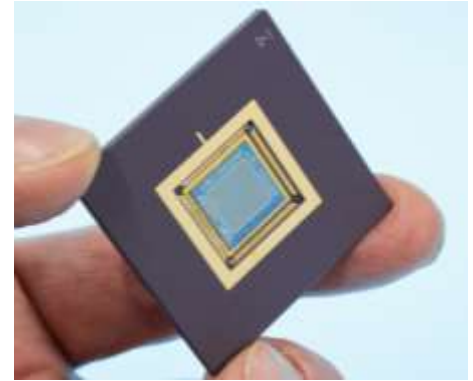
# In-Memory Signal Processing





# Summary

- MoS<sub>2</sub> photodetectors
  - Lopez-Sanchez...Kis, Nature Nanotechnology (2013)  
doi: 10.1038/nnano.2013.100
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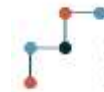
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