ÖAW AUSTRIAN ACADEMY OF SCIENCES

HEPHY INSTITUTE OF HIGH ENERGY PHYSICS

The RD50-MPWx HV-CMOS Series elevated by the Caribou system

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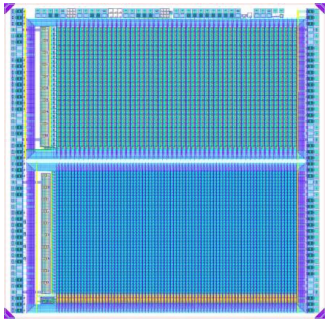
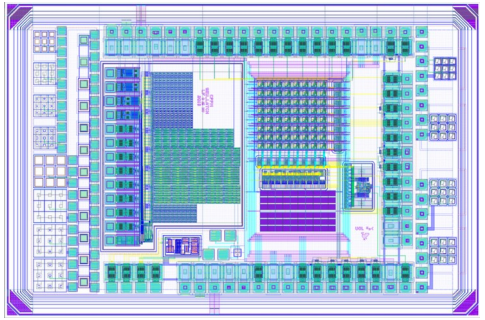
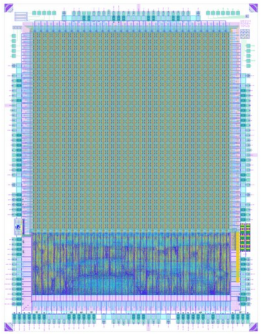
RD50 HV-CMOS Series



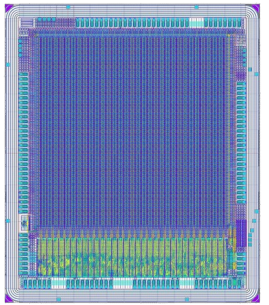
RD50-MPW1
(5mm x 5mm)



RD50-MPW2
(3.2mm x 2.1mm)



RD50-MPW3
(5.1mm x 6.6mm)



RD50-MPW4
(5.4mm x 6.3mm)

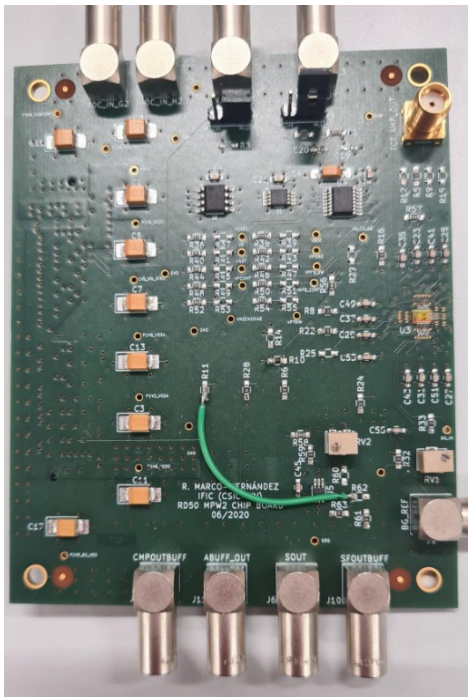
2017 2018 2019 2020 2021 2022 2023 2024

Submission and delivery date

- HV-CMOS sensors fabricated in *LFoundry* 150nm process
- All sensors use Caribou as DAQ system

RD50-MPW2

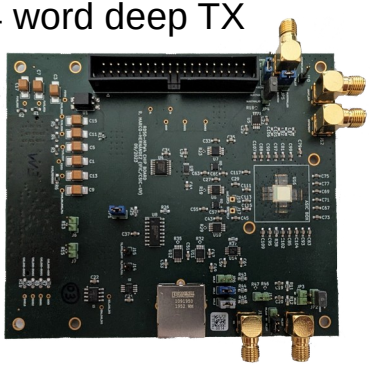
- RD50-MPW1 suffered from high leakage current
- Designed to evaluate guard rings and in-pixel electronics
- 6x6 pixel matrix with 2 pixel flavors
- Analog only
- ADC on chip carrier board digitizing signals
  - Directly operated by FPGA on Xilinx Zynq ZC706
- Peary device used *just* to operate FPGA via AXI
- Configuration also done by FPGA
- Carboard DACs used for supply voltages



RD50-MPW3 / -MPW4

Both sensors feature:

- 64x64 pixel matrix arranged in 32 FEI-3 style double columns
- Active area of 4x4mm²
- Pixel-size of 62x62µm²
- 8 bit timestamp information (based on 25ns) for each hit
- 4 bit in-pixel trimming
- 640MHz readout
- Digital periphery with 128 / 64 word deep TX FIFOs
- Configuration via I²C

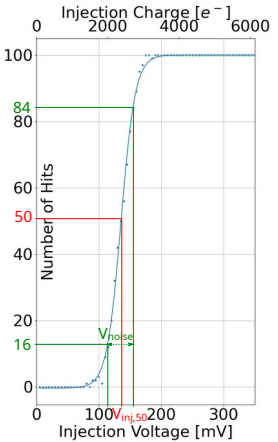


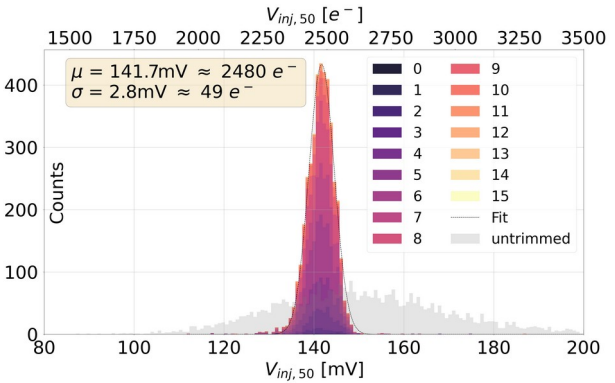
Modifications / Improvements MPW3 → MPW4

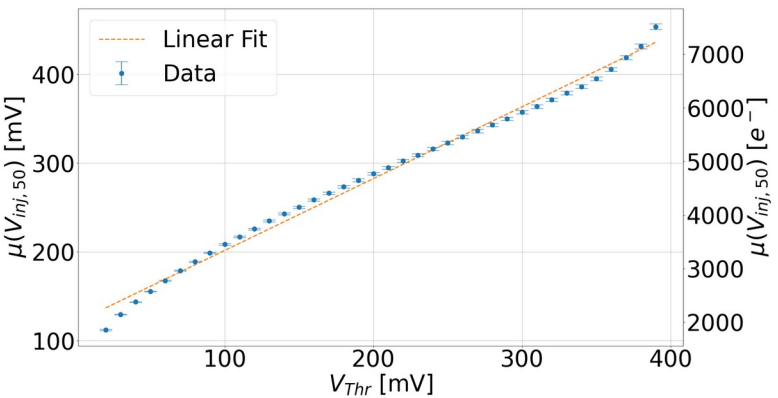
- Noise significantly reduced by
  - separating power domains of in-pixel and peripheral digital readout
  - improved routing of power lines
- Optimized guard rings
  - higher breakdown voltage → improved radiation hardness
- Backside processing
  - higher breakdown voltage→ improved radiation hardness
- Length of EOC readout signals adjustable

MPW3/4 Peary implementation

- Custom I²C interface implemented
  - Internal conversion from I²C → Wishbone
  - Non *standard* I²C implementation (SMBus 7 bit address range not sufficient)
  - Used for configuration of chip
- Data transfer from FPGA → Peary via AXI
- Laboratory measurements implemented in device
  - S-curve injection measurements
  - Hitmap
  - TrimDAC evaluation
- Preprocessed form of raw data stored to text files in Poky Linux
- Data analysis done via external Python tools

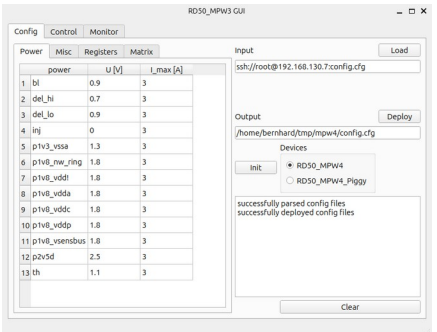


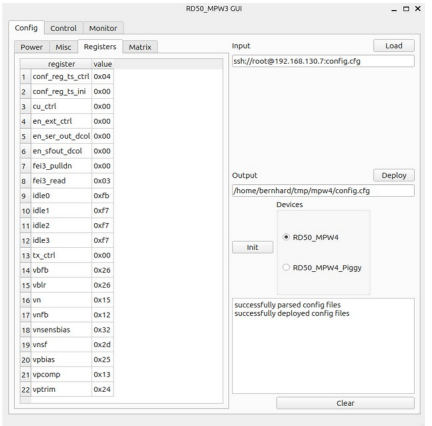


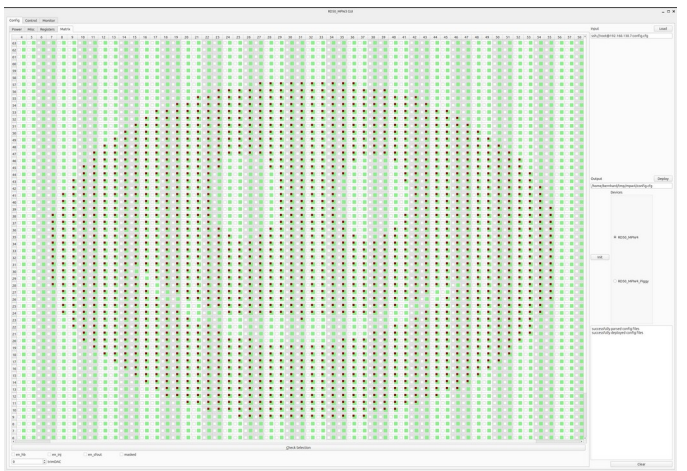


Generic GUI

- 23 global registers and 16 registers for each double column
- Every single pixel has 8 bit config options
- Implemented GUI for user friendly generation of Peary-style config-files
- GUI could be used by other pixel detectors
  - Fully configurable by JSON config file
- Features EUDAQ2 monitor (hitmap)

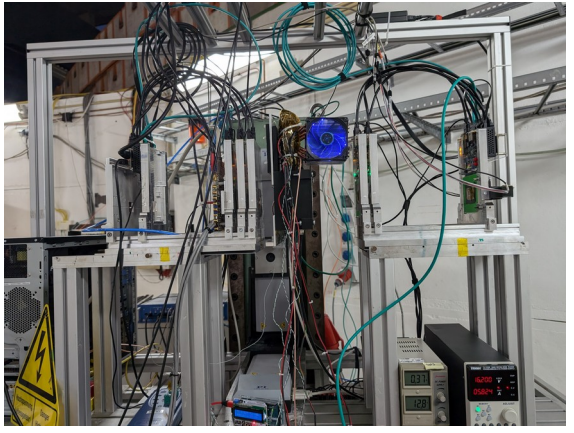


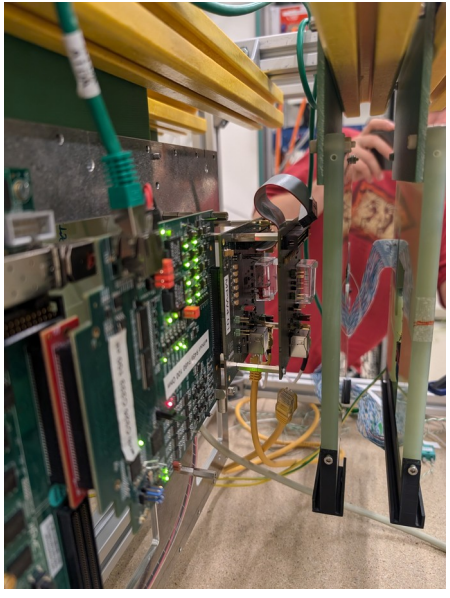




MPW3/4 testbeam DAQ

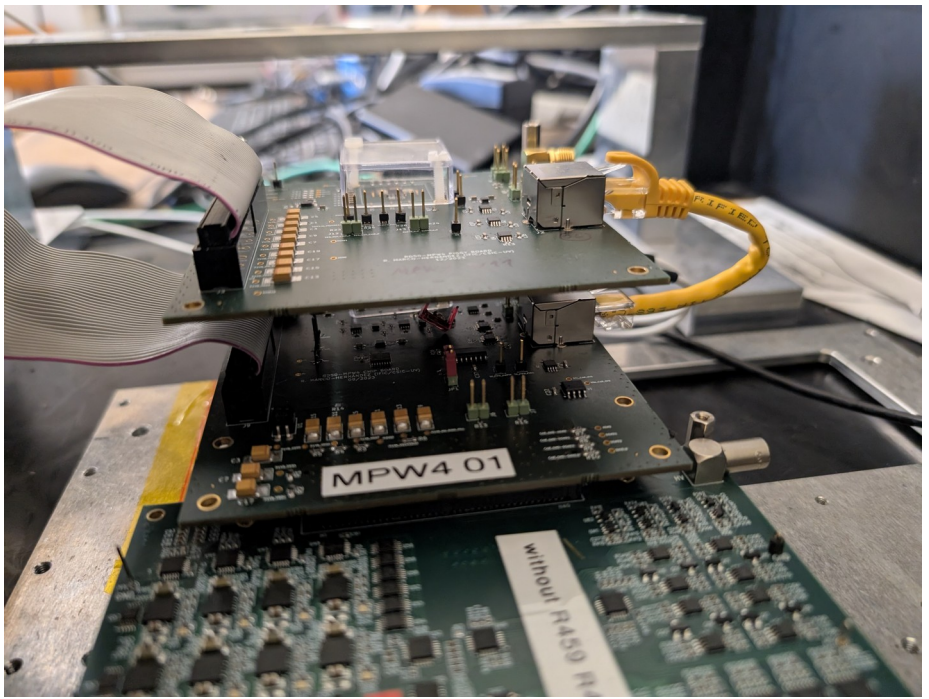
- Utilizing EUDAQ2's Caribou producer
- Data taking:
  - Our *standard* data path via AXI FIFOs too slow for testbeam usage
  - Implemented fast data path: FPGA dispatches UDP packages
  - Custom EUDAQ2 data collector developed
    - Multi threaded approach
    - Data rate of up to 1 Gbit/s possible (not needed at our usual testbeam sites)
- Entire setup mounted on aluminium frame and placed into beam telescope
  - No *proper / flexible* FMC cables available
  - Suggestions for improvements very welcome!





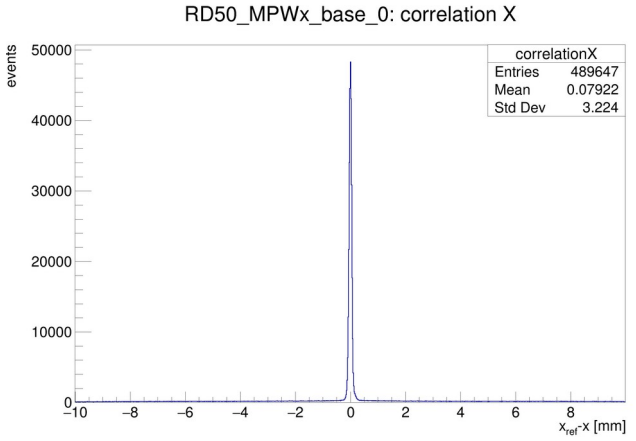
Doubling the number of DUTs in one Caribou system
The Piggy Board

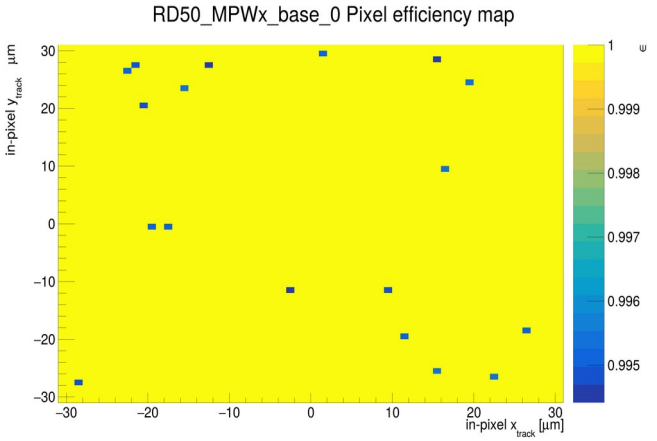
- Initial idea:
  - Readout and operate two RD50-MPW3/4s with just one Caribou system
  - Easy to install / remove DUTs for testbeam scenarios
- Implementation:
  - Developed second chip carrier board
  - Reduced number of electronic components
  - Connected to *main* chip board via a ribbon cable (bias voltages, slow signals) and an Ethernet cable (data and clock lines)
- Both DUTs readout by the same FW / FPGA via separate serial data lines

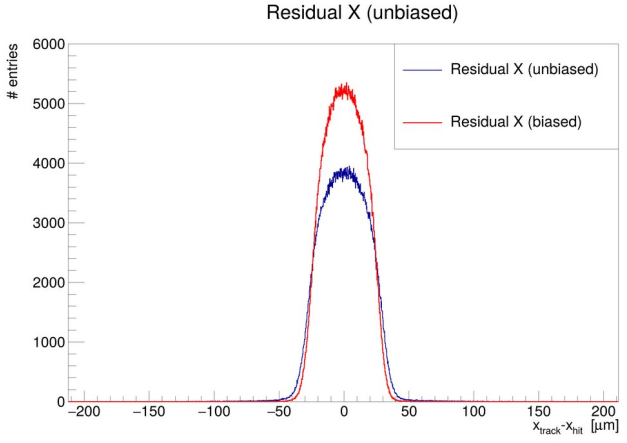


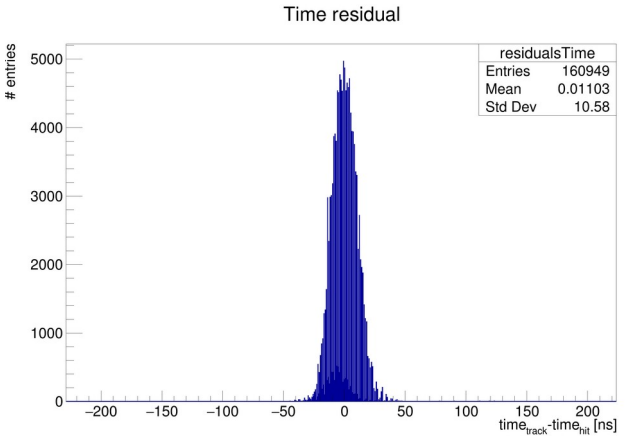
Testbeam performance of the RD50-MPW4

- Triggerless readout of RD50-MPW3/4
  - Timestamps utilized for synchronization
- Matching events of DUT with telescope done by employing the AIDA 2020 TLU
- Narrow correlation peak with very little background
- Efficiency > 99.9% evaluated
- Spatial resolution of ~15.8µm
- Time resolution of ~10ns

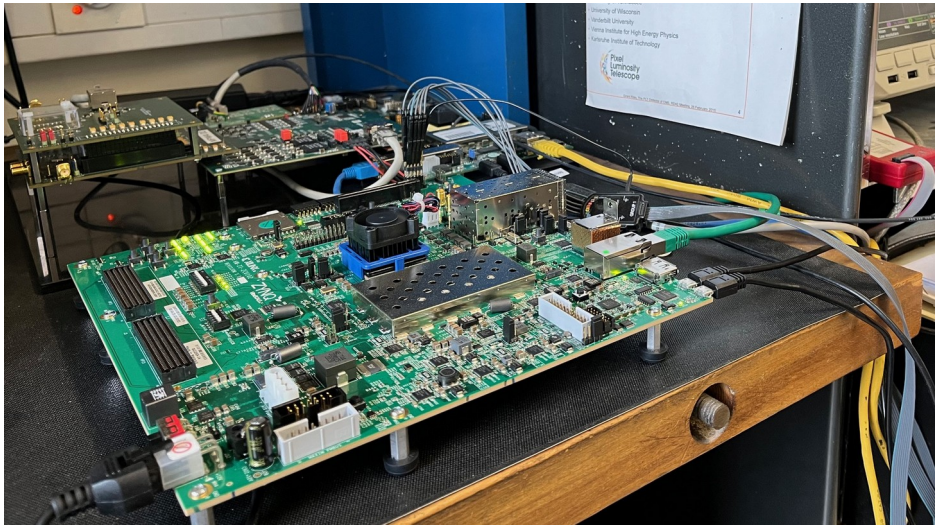




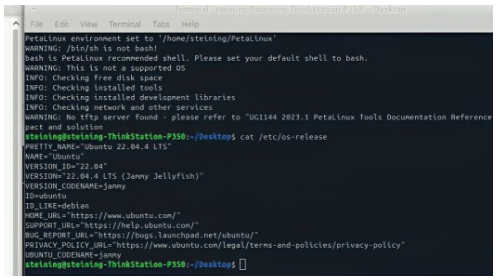


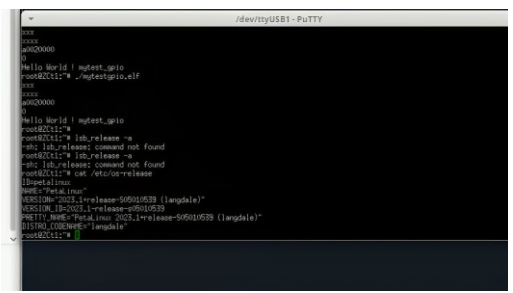


Developments towards Caribou 2.0



- In order to get fit for Caribou 2.0 started to port FW to Xilinx ZCU102
- So far managed to boot Peta Linux
- Currently trying to get DMA running
- Work in progress





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Thank you for your attention!
Questions?

This work has been partly performed in the framework of the CERN-RD50 collaboration.

The measurements leading to these results have been performed at the Test Beam Facility at DESY Hamburg (Germany), a member of the Helmholtz Association (HGF).

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