How does the NA61 Trigger work?

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National Centre for Nuclear Researech

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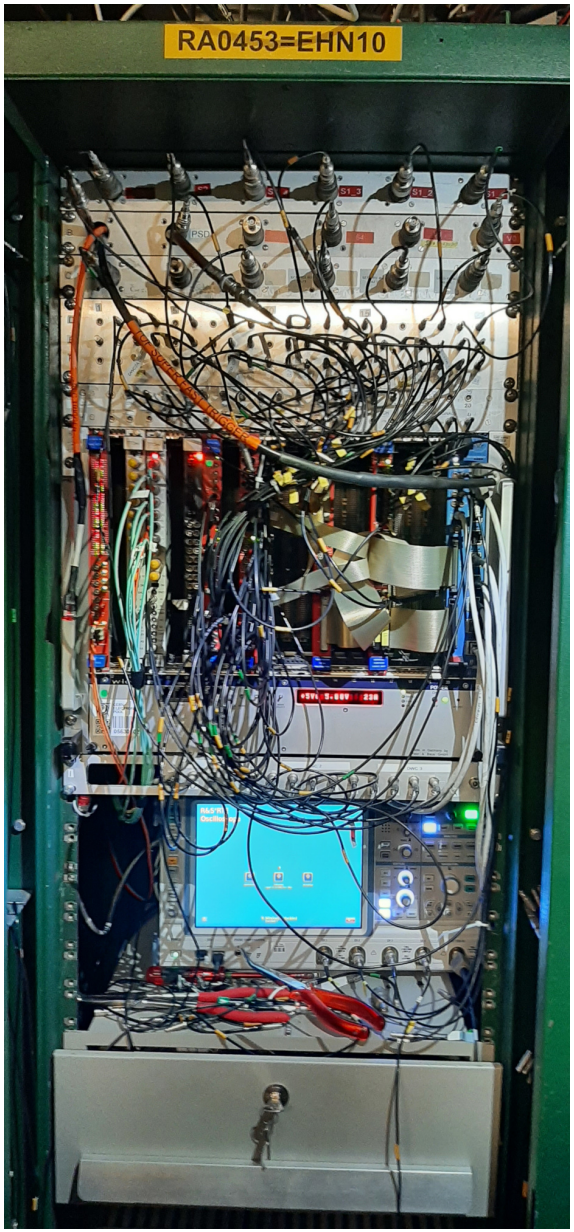
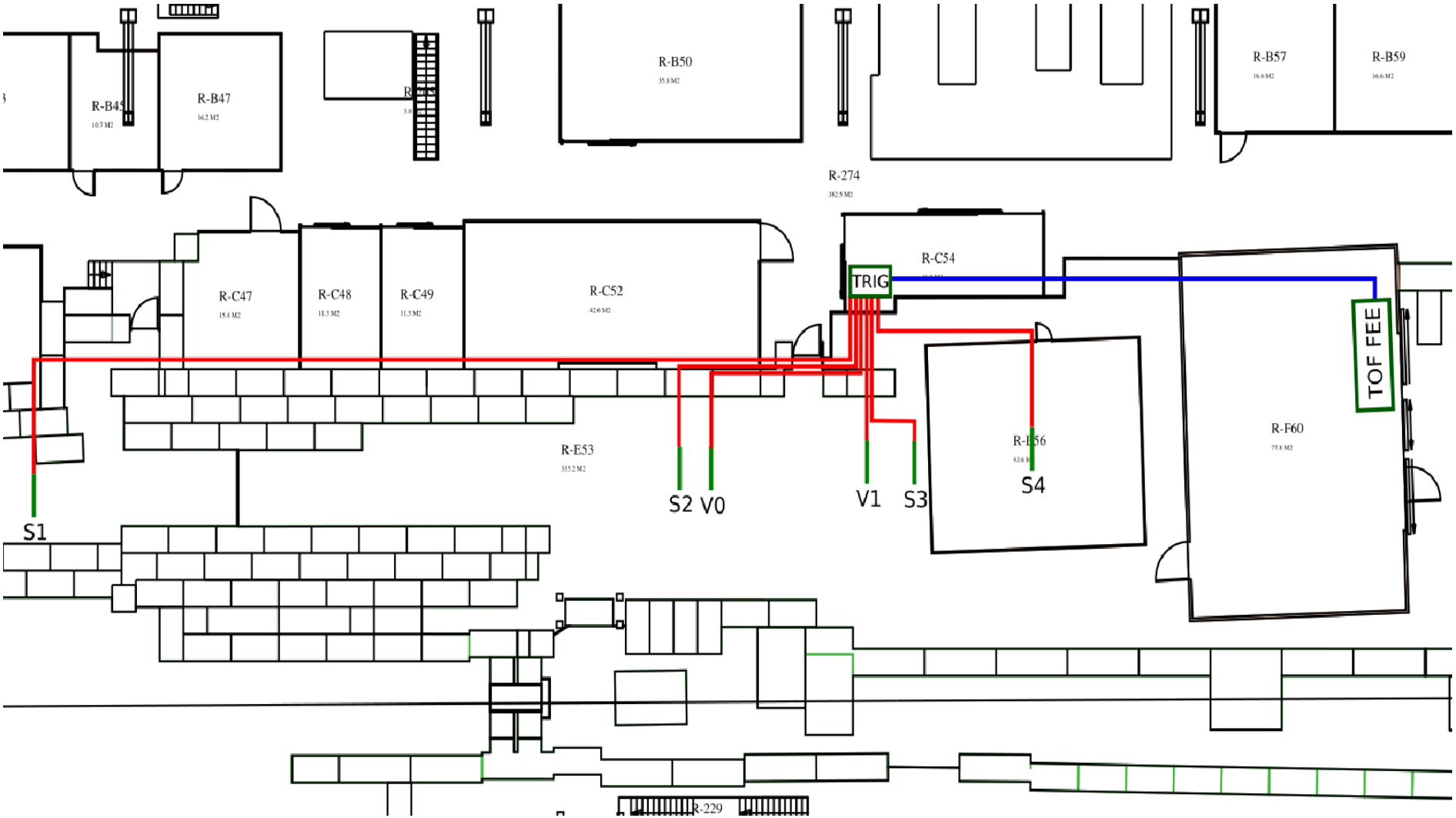
The Trigger

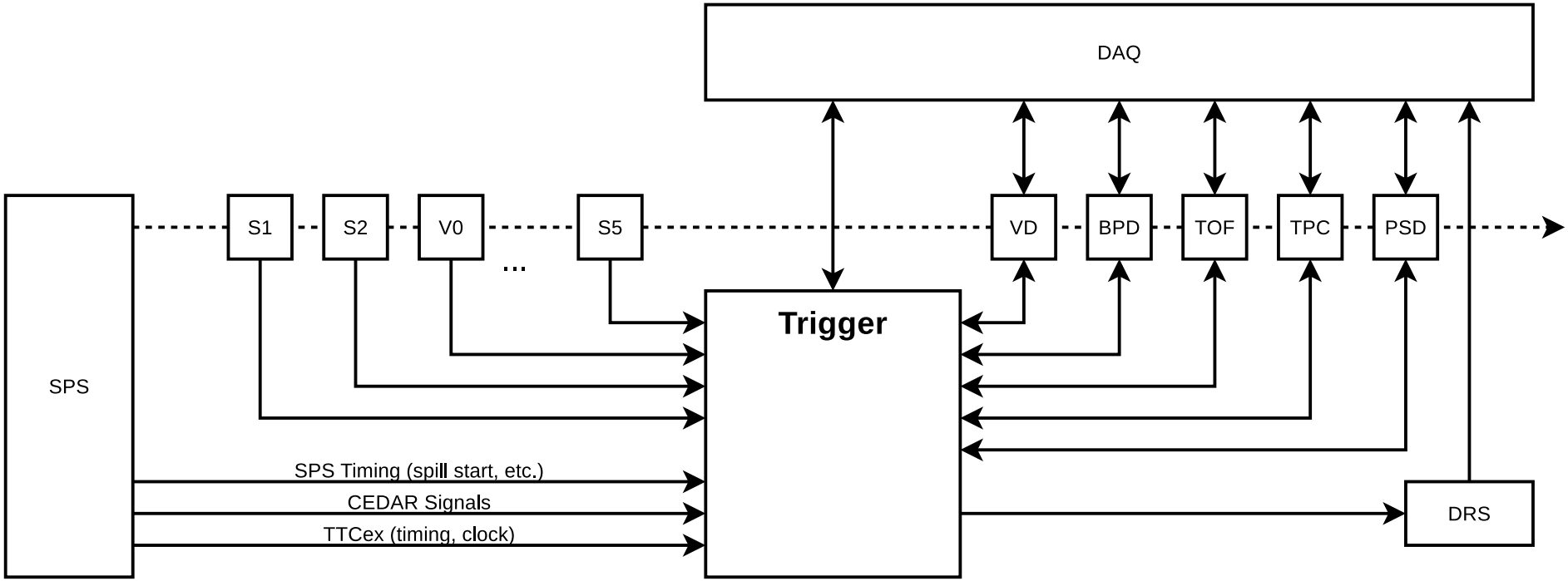
- Main function: detect requested type of events and start data acquisition
- One of the core subsystems
- Without working trigger no data can be taken



Trigger and beam counters location



Trigger logical diagram and main tasks



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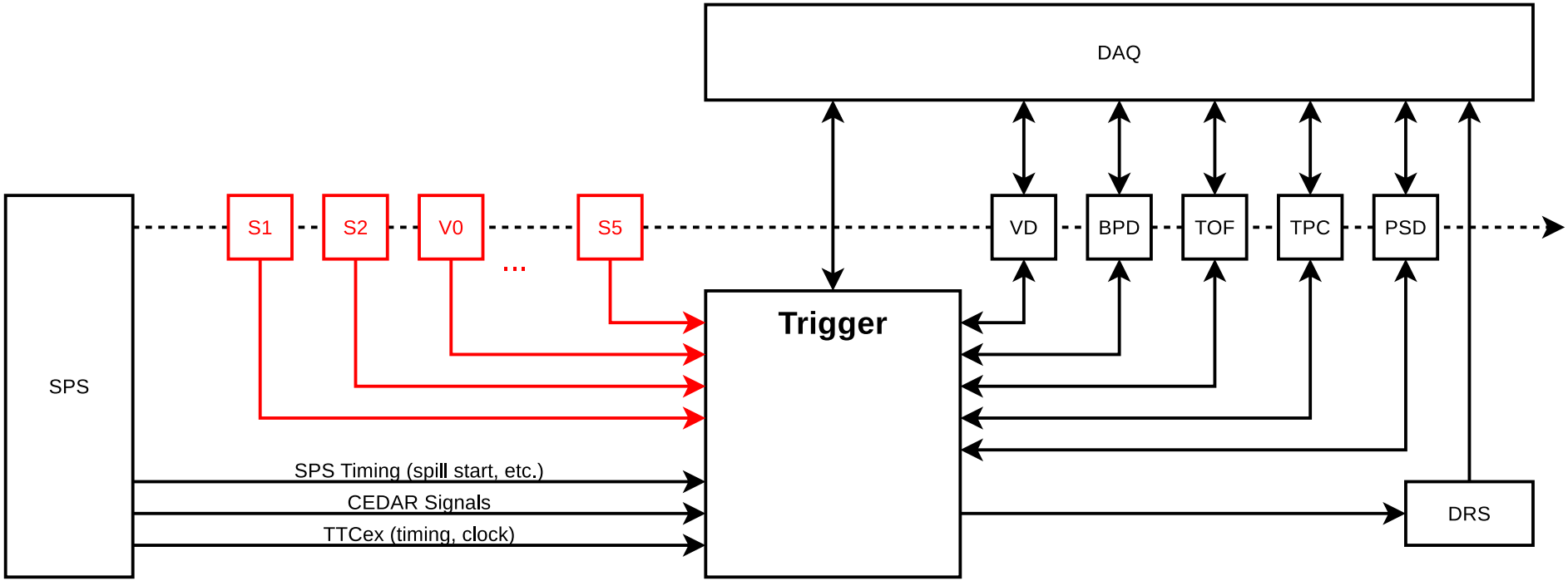

- Reads signals from beam counters

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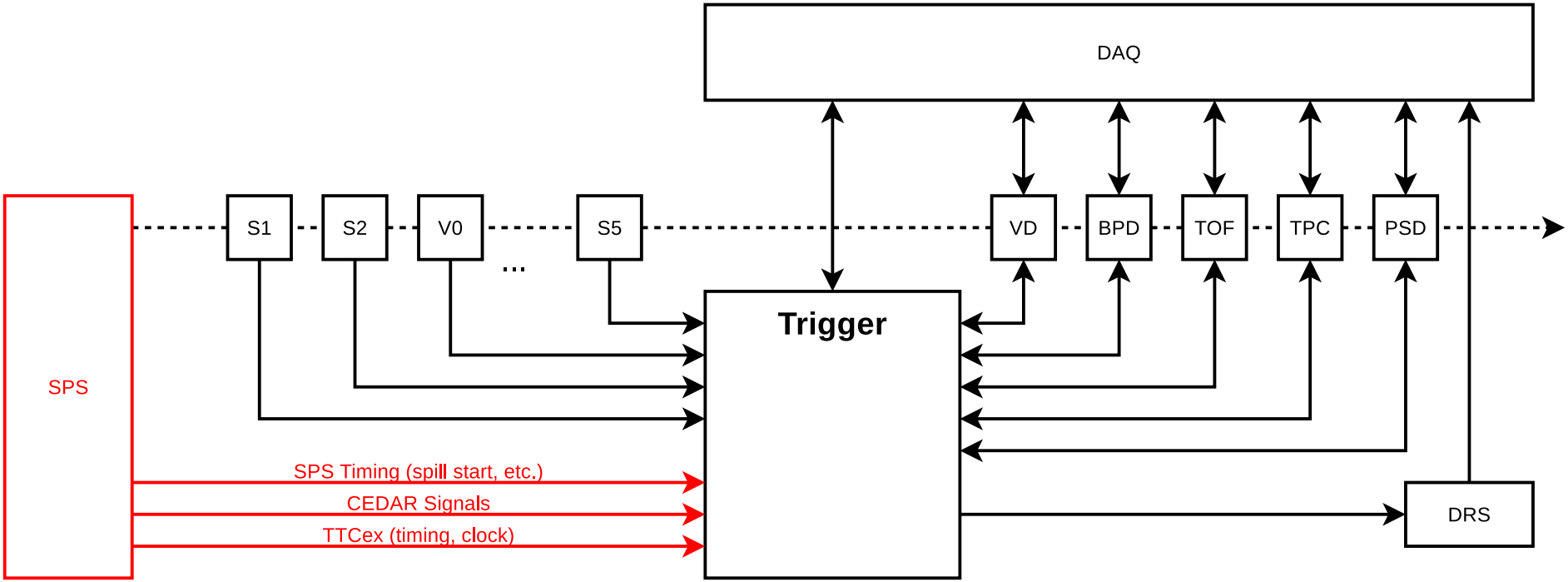

- Reads signals from beam counters
- Reads external signals from SPS

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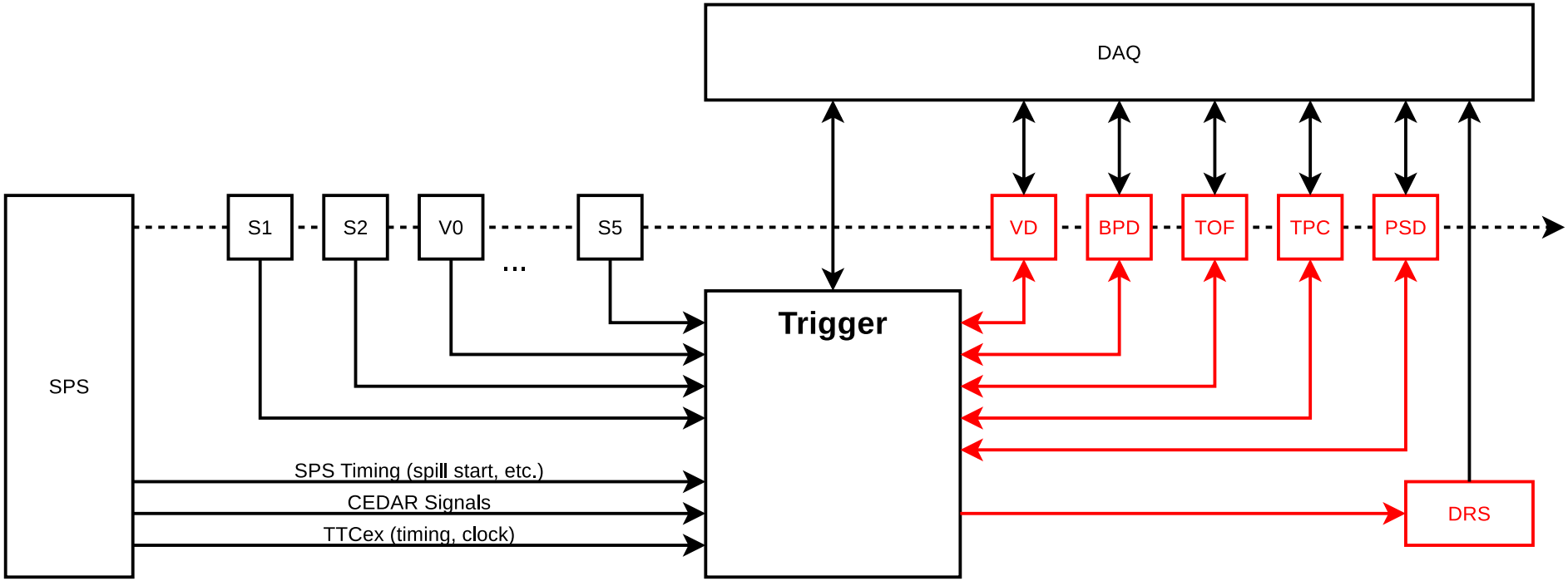

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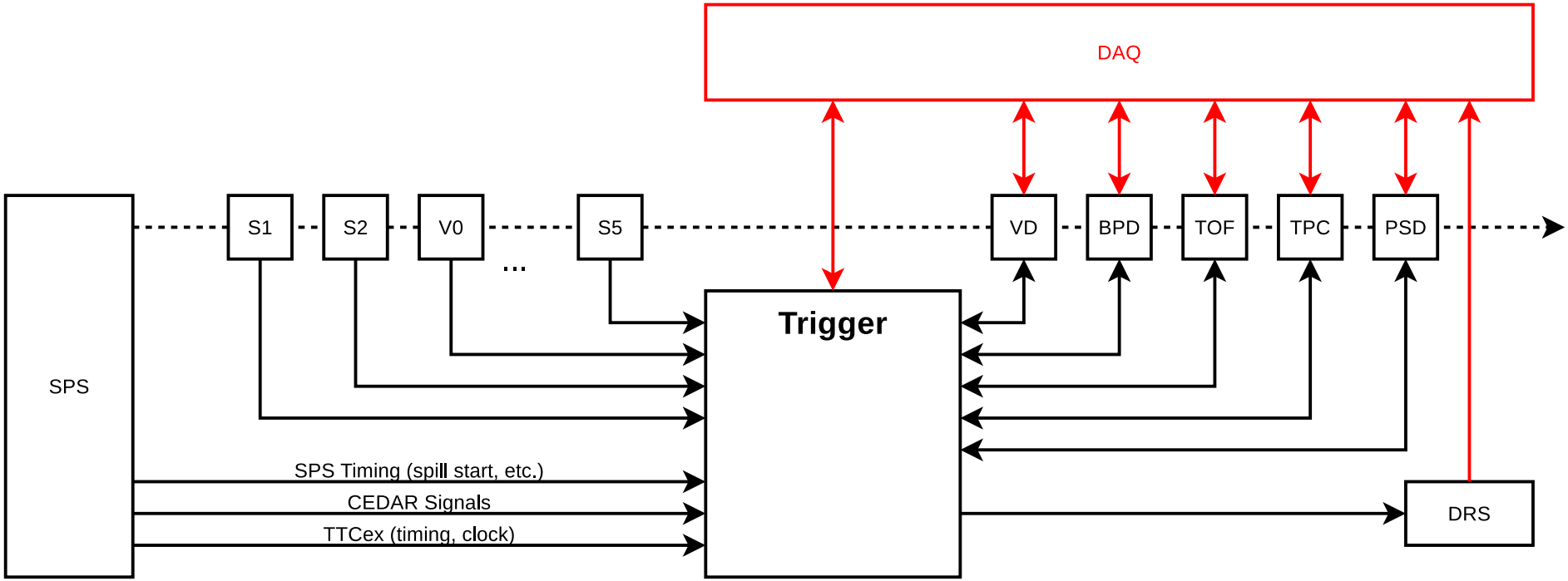
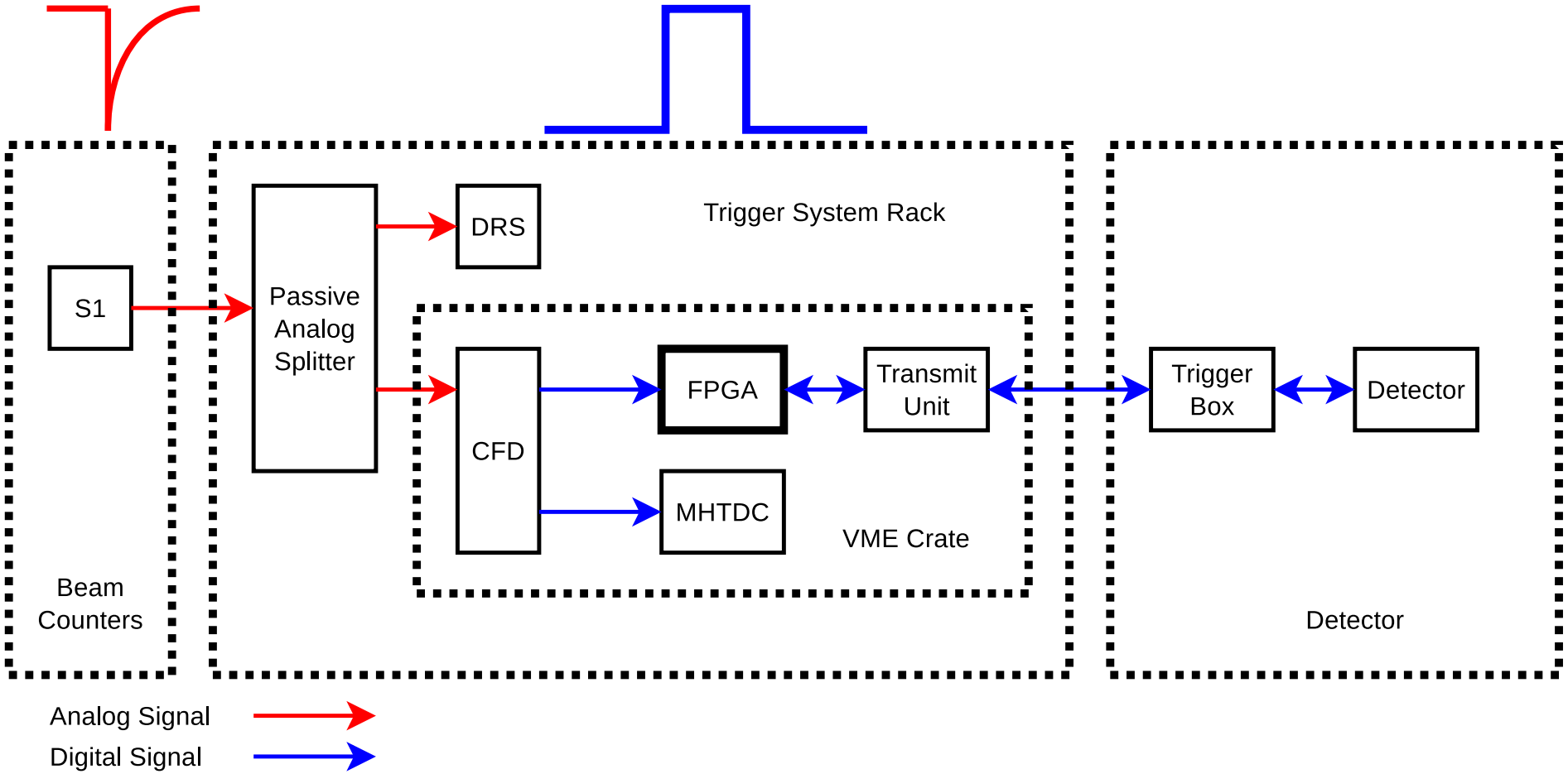
- Reads external signals from SPS
- Controls data acquisition in all detectors

Trigger logical diagram and main tasks



- Reads signals from beam counters
- Reads external signals from SPS
- Controls data acquisition in all detectors
- Initiated by trigger, DAQ reads data from detectors

Trigger system internal structure



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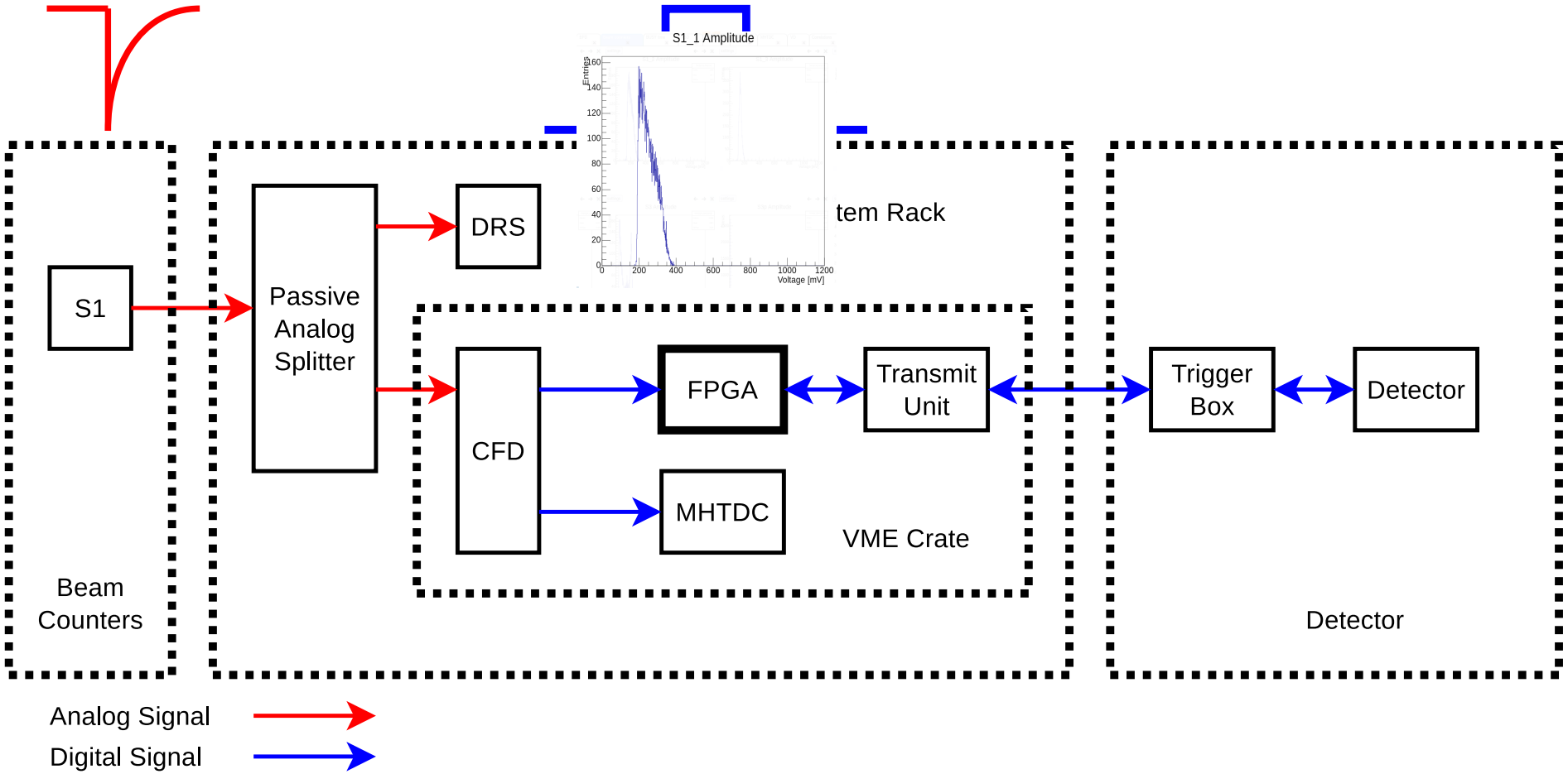
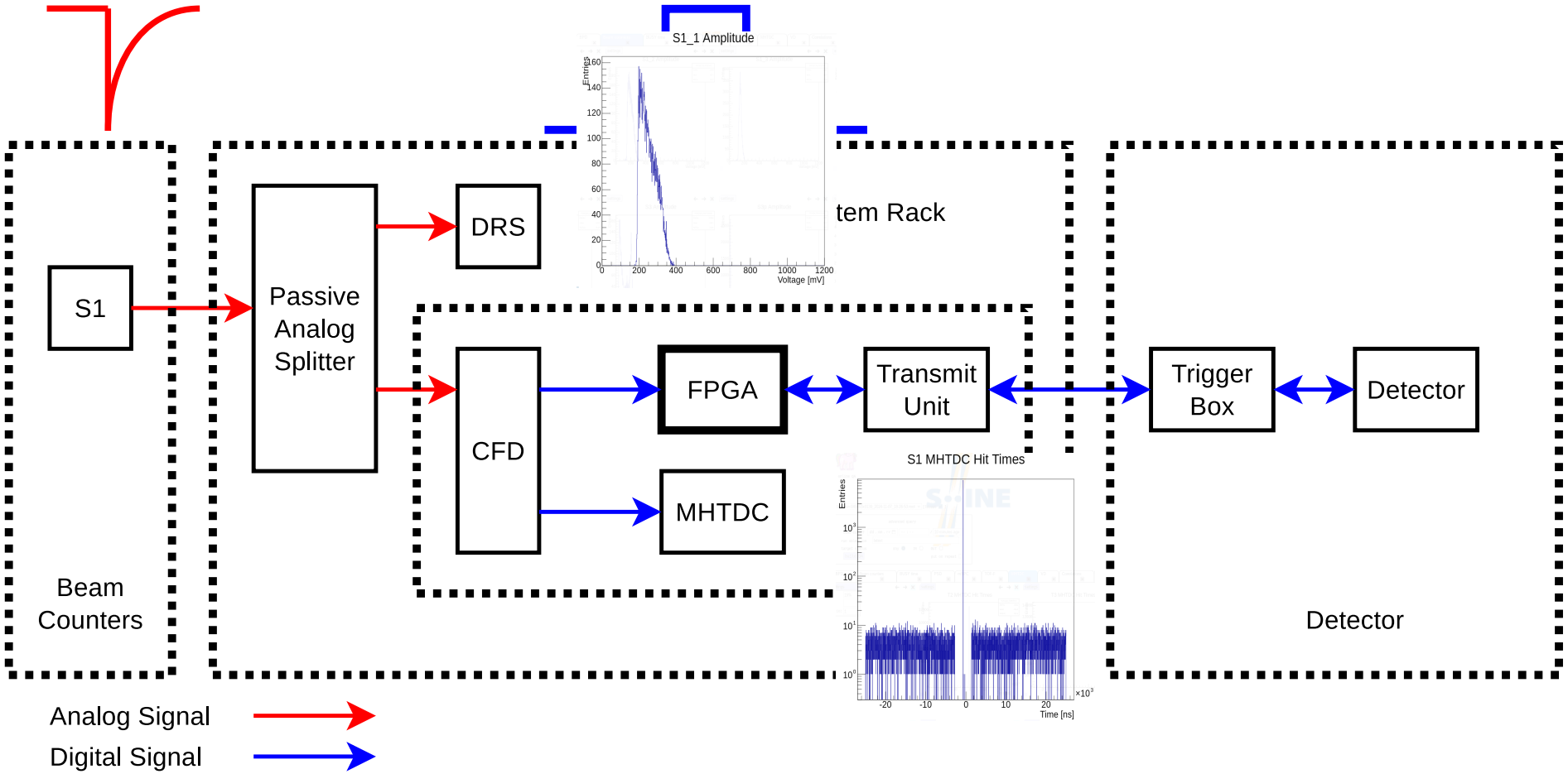


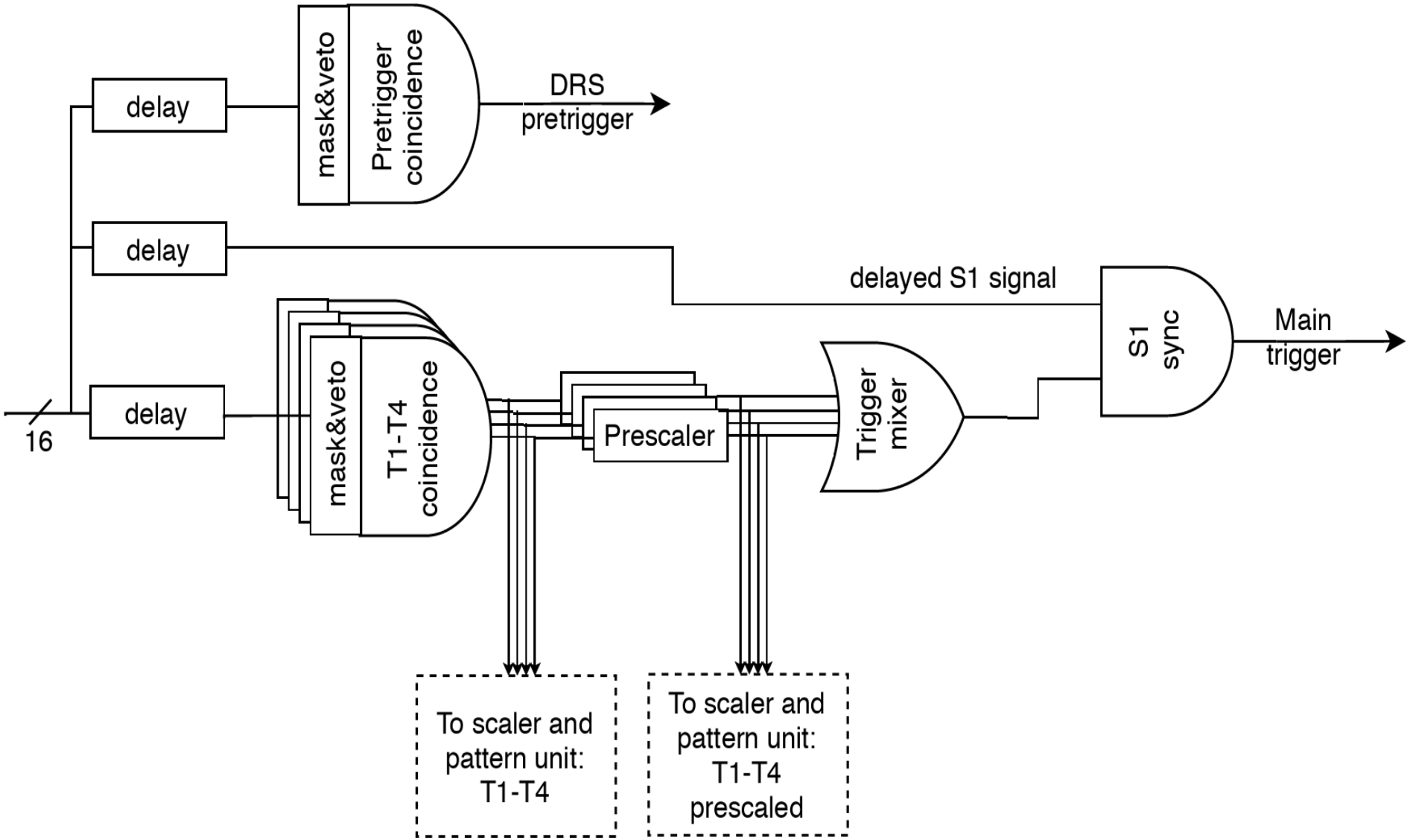
- DRS Provides the amplitude information on trigger signals

Trigger system internal structure

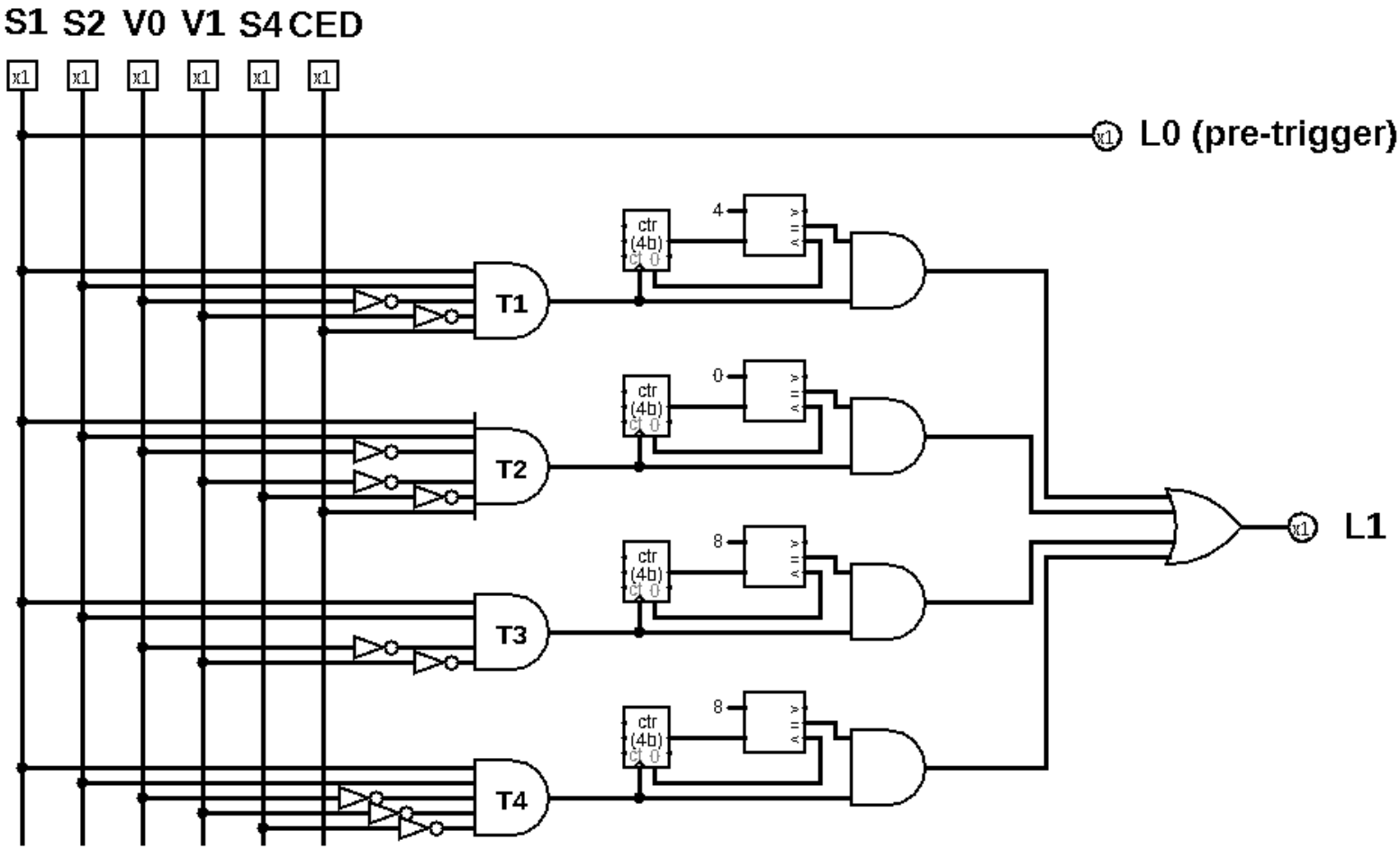


- DRS Provides the amplitude information on trigger signals
- Multi-hit TDC provides time distribution within time window around the trigger

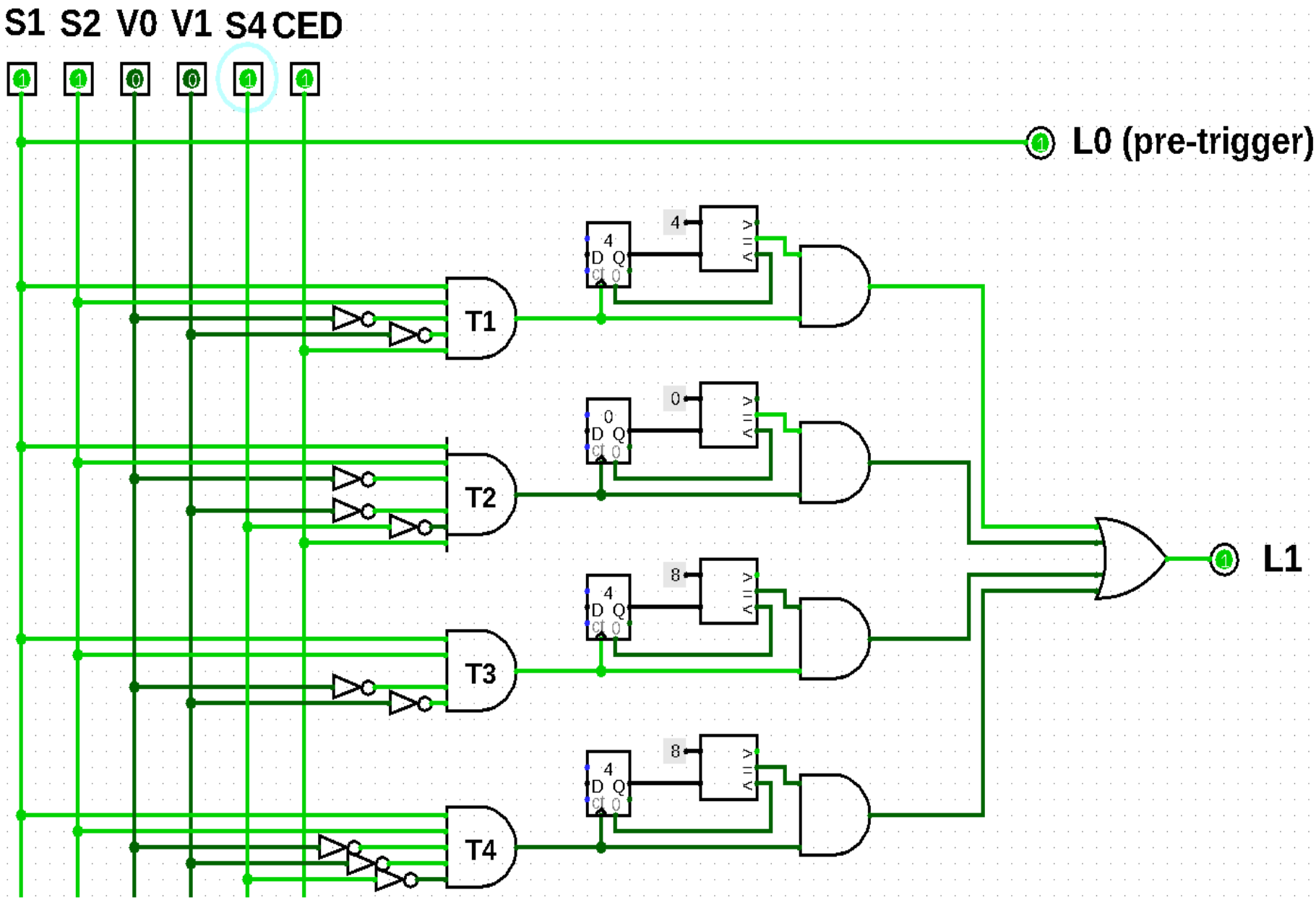
Trigger FPGA logic



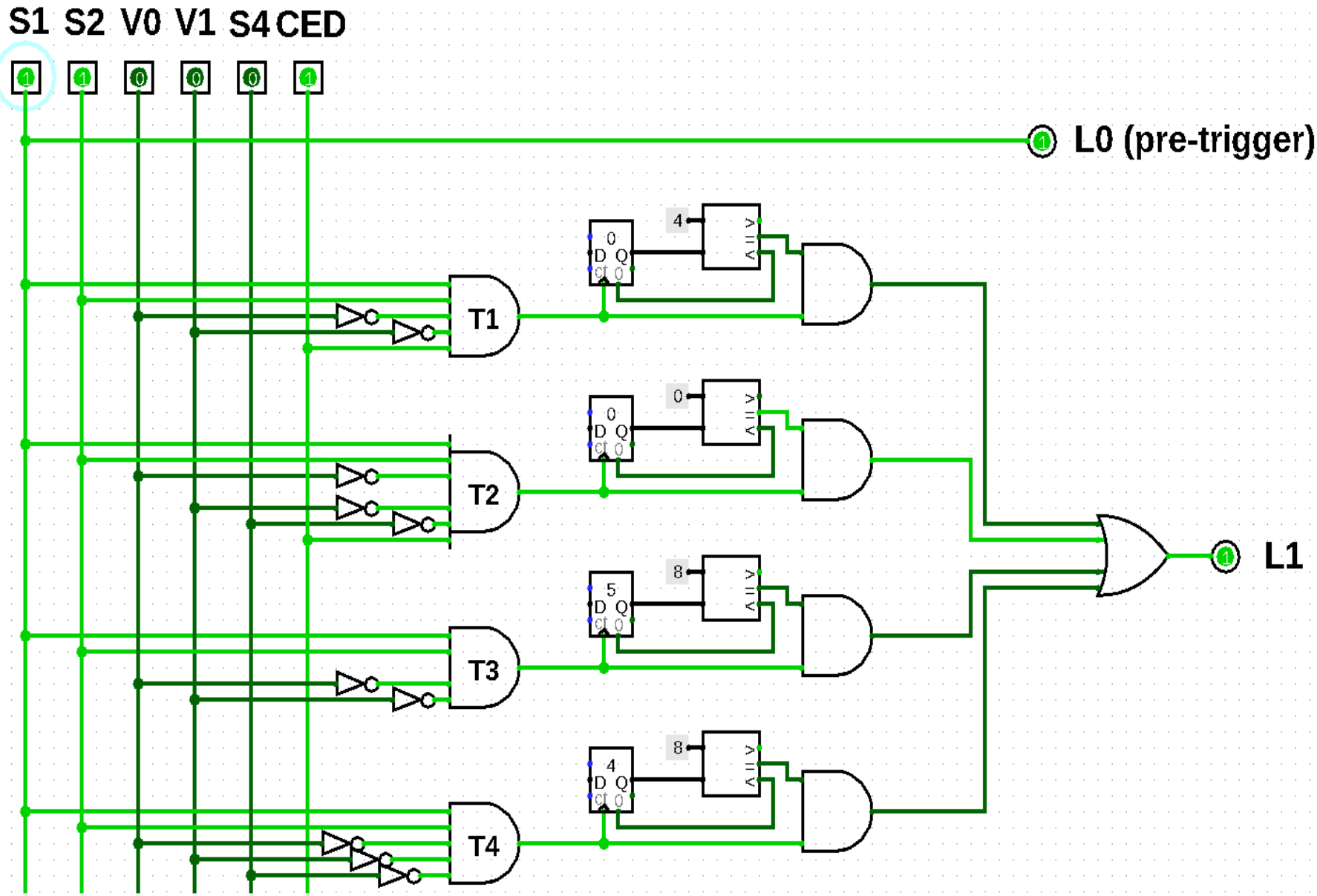
Trigger FPGA logic - different view



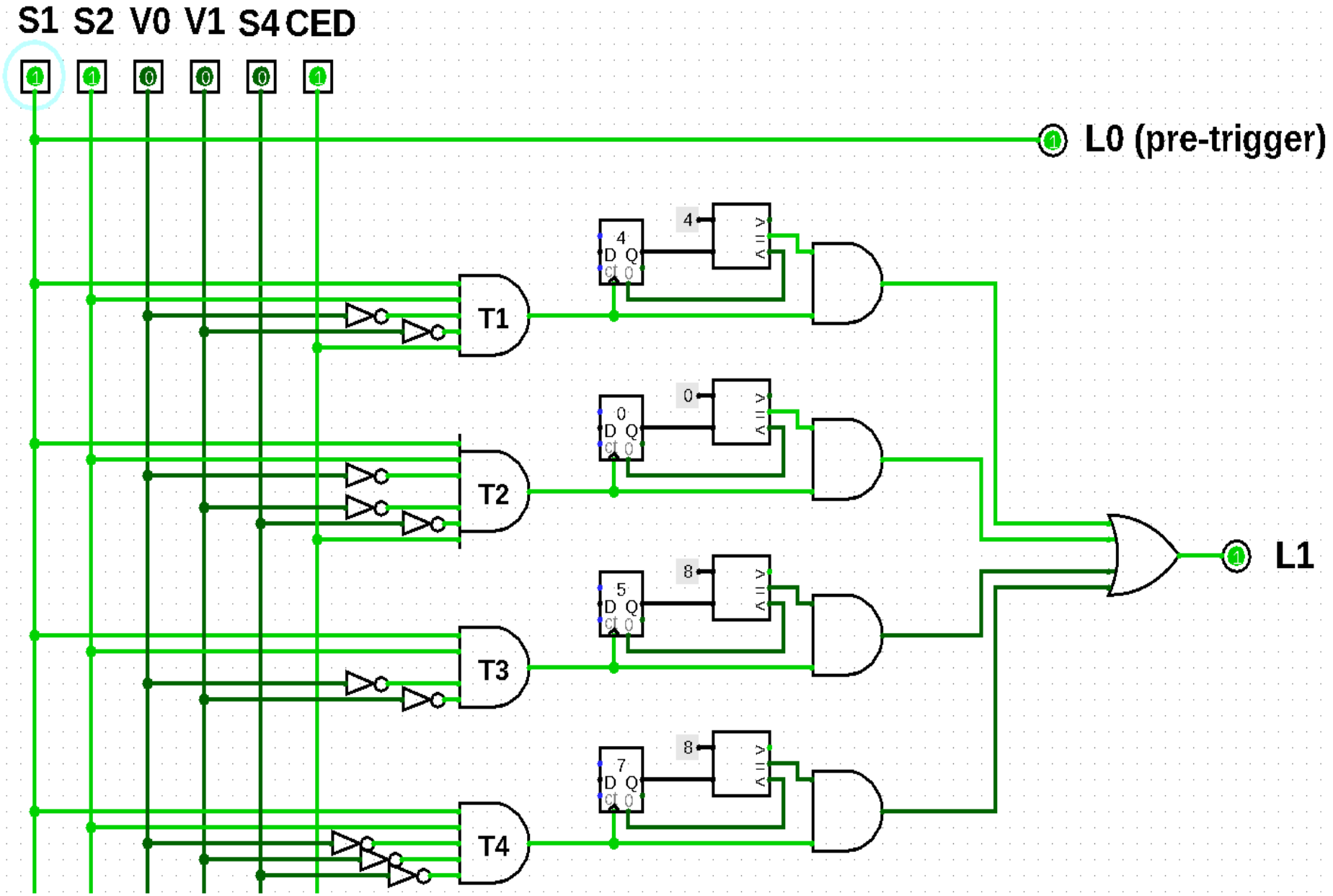
Trigger FPGA logic - T1 condition



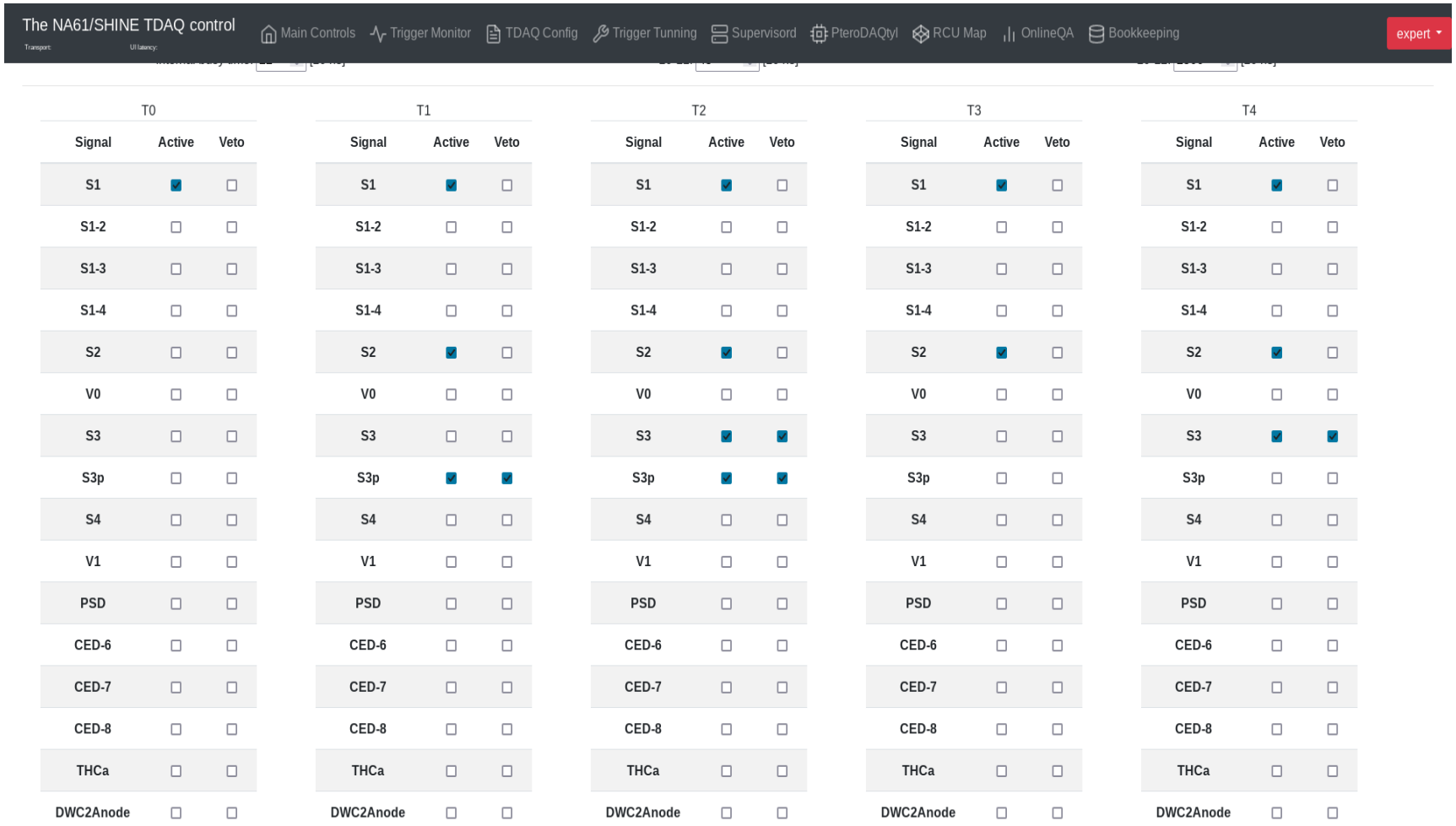
Trigger FPGA logic - T2 condition



Trigger FPGA logic - T1 and T2 condition



Trigger definitions in the GUI



T0		
Signal	Active	Veto
S1	☑	☐
S1-2	☐	☐
S1-3	☐	☐
S1-4	☐	☐
S2	☐	☐
V0	☐	☐
S3	☐	☐
S3p	☐	☐
S4	☐	☐
V1	☐	☐
PSD	☐	☐
CED-6	☐	☐
CED-7	☐	☐
CED-8	☐	☐
THCa	☐	☐
DWC2Anode	☐	☐

T1		
Signal	Active	Veto
S1	☑	☐
S1-2	☐	☐
S1-3	☐	☐
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S2	☑	☐
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S3p	☑	☑
S4	☐	☐
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T2		
Signal	Active	Veto
S1	☑	☐
S1-2	☐	☐
S1-3	☐	☐
S1-4	☐	☐
S2	☑	☐
V0	☐	☐
S3	☑	☑
S3p	☑	☑
S4	☐	☐
V1	☐	☐
PSD	☐	☐
CED-6	☐	☐
CED-7	☐	☐
CED-8	☐	☐
THCa	☐	☐
DWC2Anode	☐	☐

T3		
Signal	Active	Veto
S1	☑	☐
S1-2	☐	☐
S1-3	☐	☐
S1-4	☐	☐
S2	☑	☐
V0	☐	☐
S3	☐	☐
S3p	☐	☐
S4	☐	☐
V1	☐	☐
PSD	☐	☐
CED-6	☐	☐
CED-7	☐	☐
CED-8	☐	☐
THCa	☐	☐
DWC2Anode	☐	☐

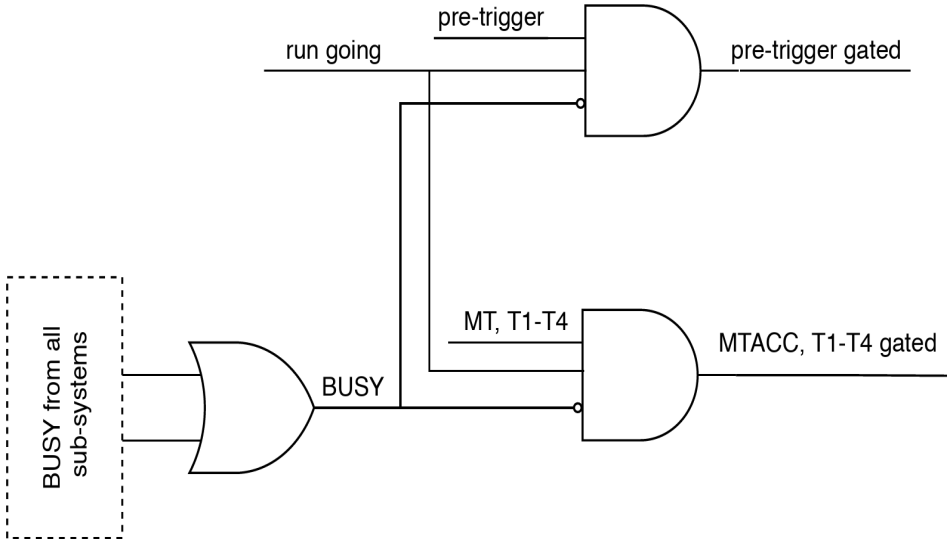
T4		
Signal	Active	Veto
S1	☑	☐
S1-2	☐	☐
S1-3	☐	☐
S1-4	☐	☐
S2	☑	☐
V0	☐	☐
S3	☑	☑
S3p	☐	☐
S4	☐	☐
V1	☐	☐
PSD	☐	☐
CED-6	☐	☐
CED-7	☐	☐
CED-8	☐	☐
THCa	☐	☐
DWC2Anode	☐	☐

Prescalers settings

Prescalers

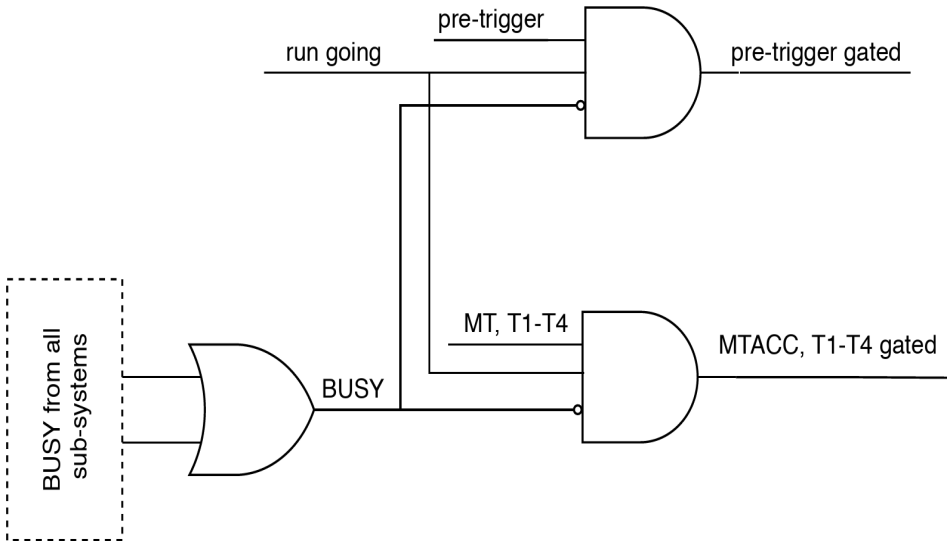
Trigger	Value
T1	100
T2	1
T3	1000
T4	0

Trigger Busy Logic



- L0 and L1 are generated only when there is run going (during the spill and when DAQ is enabled)

Trigger Busy Logic



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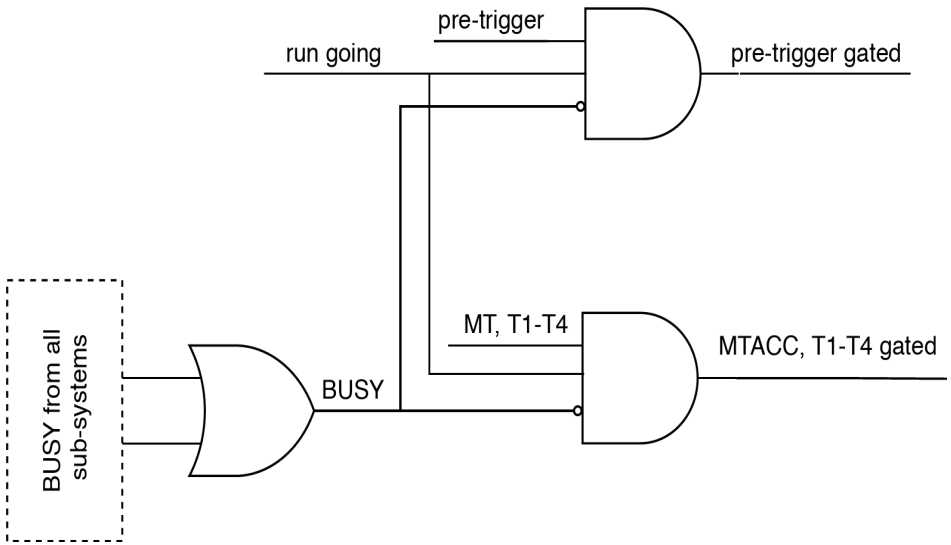

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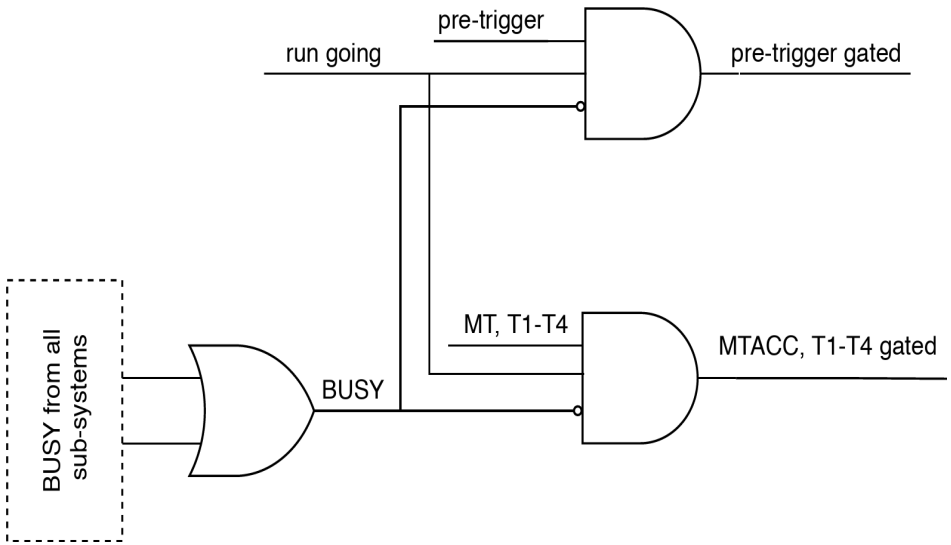

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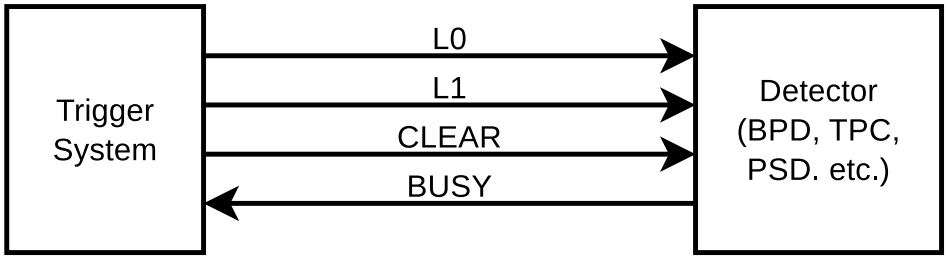
- T1 to T4 counts and T2/T1 ratio before gating tells what is physical ratio between events
- T1 to T4 counts after the gating tells how many events has been actually accepted and saved by DAQ

Detector handshake - valid event



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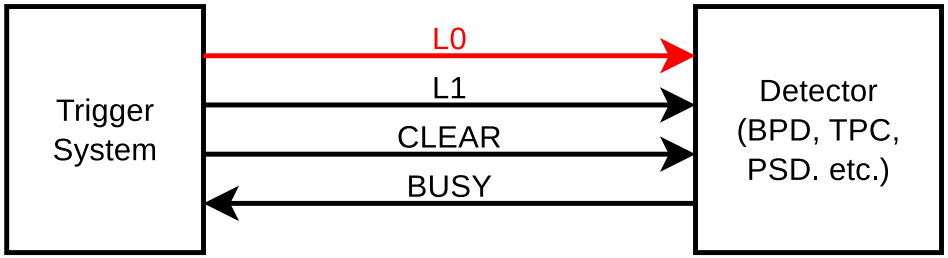

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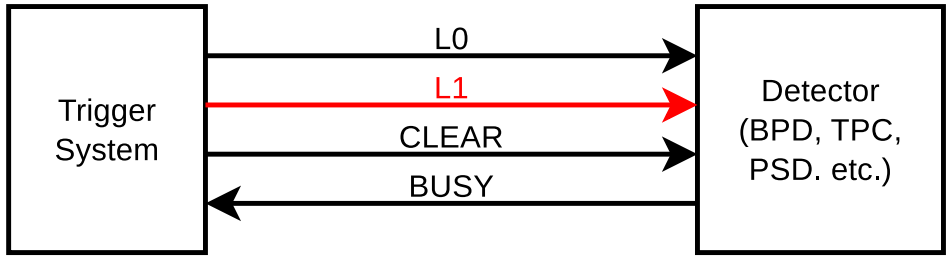

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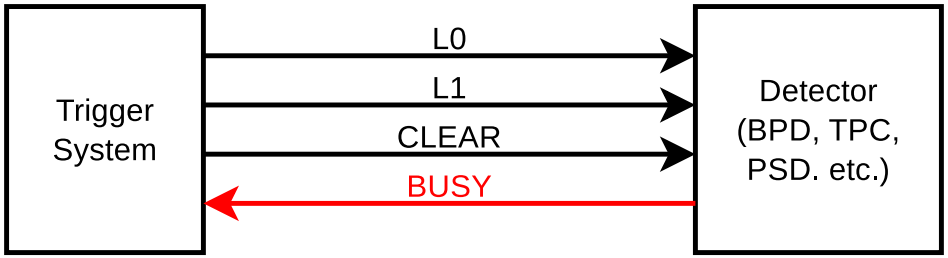

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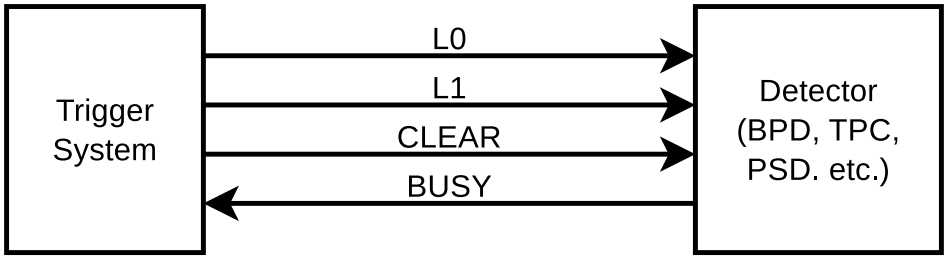

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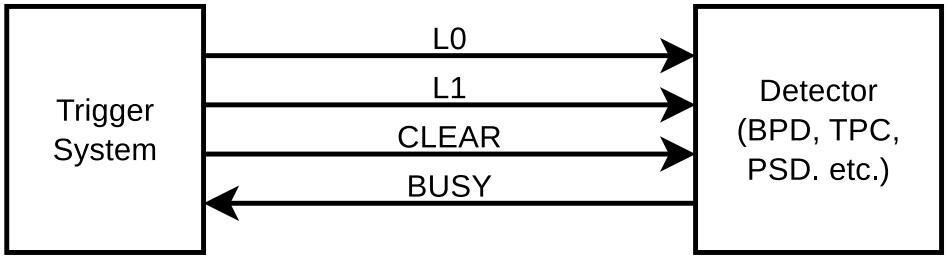

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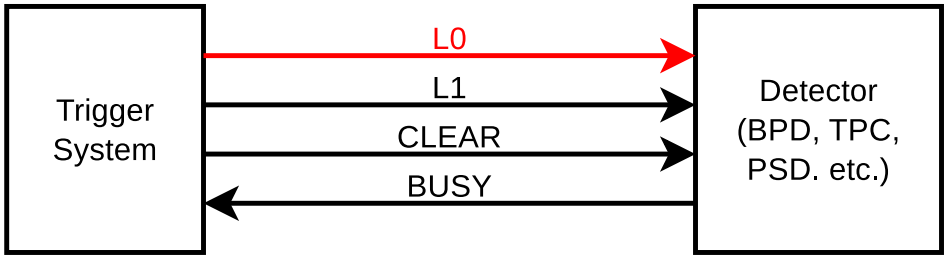

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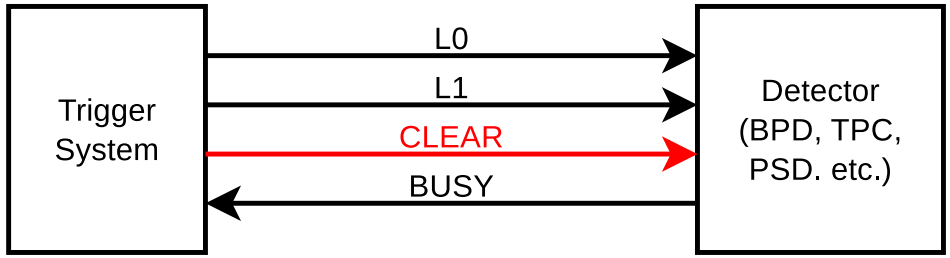

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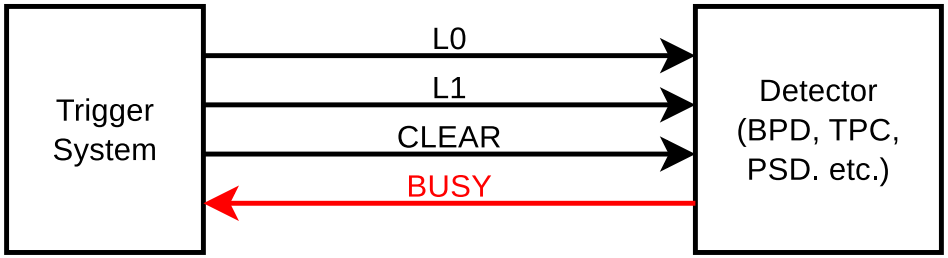

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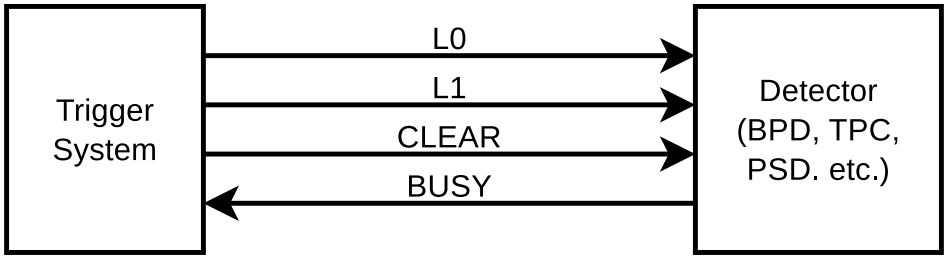

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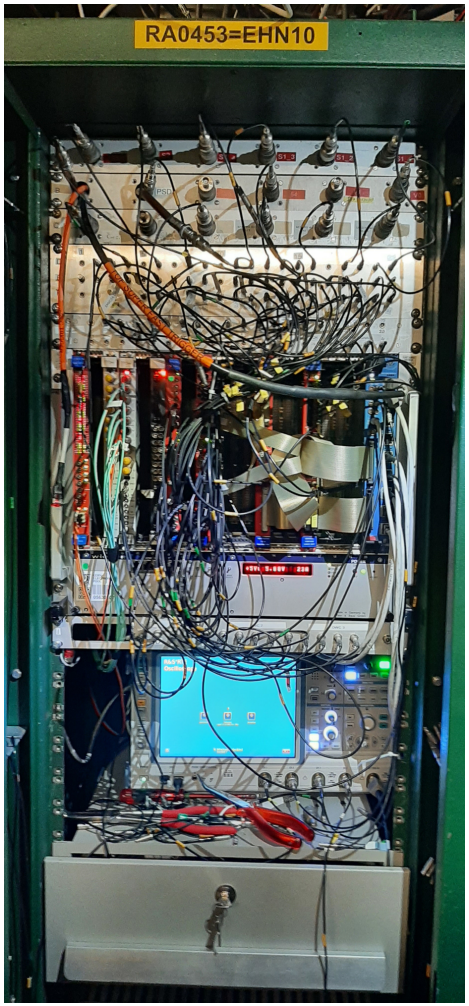
Future plans for the Trigger



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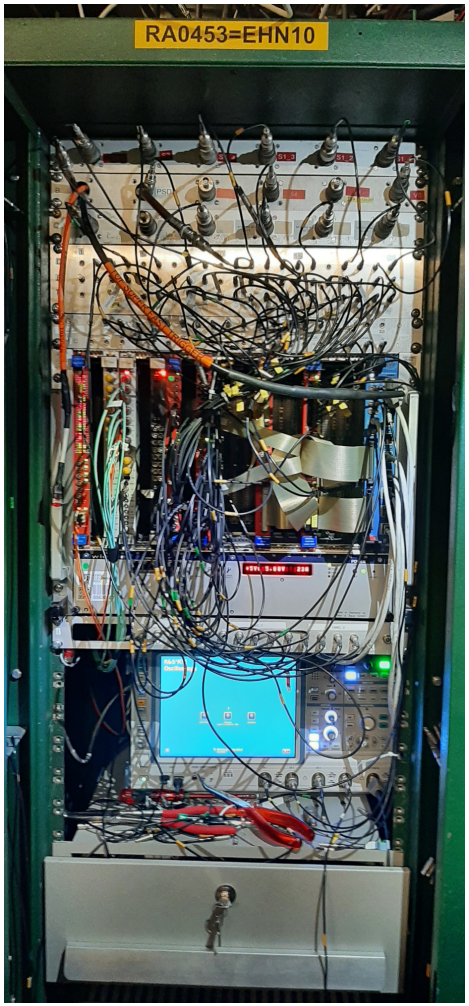

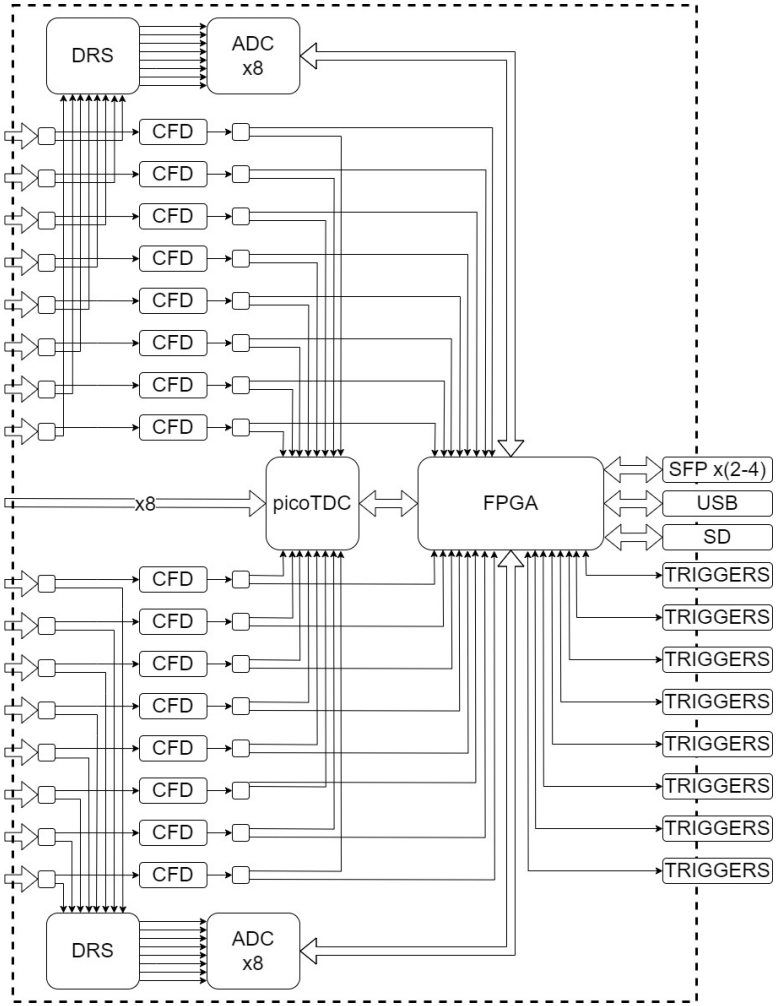

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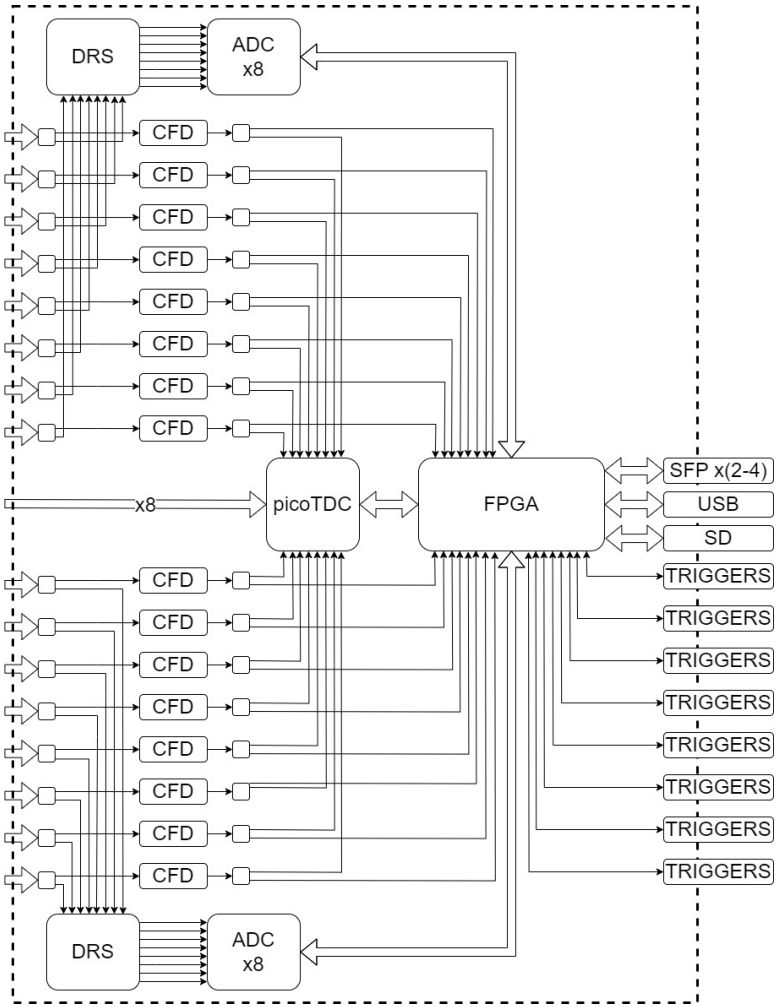

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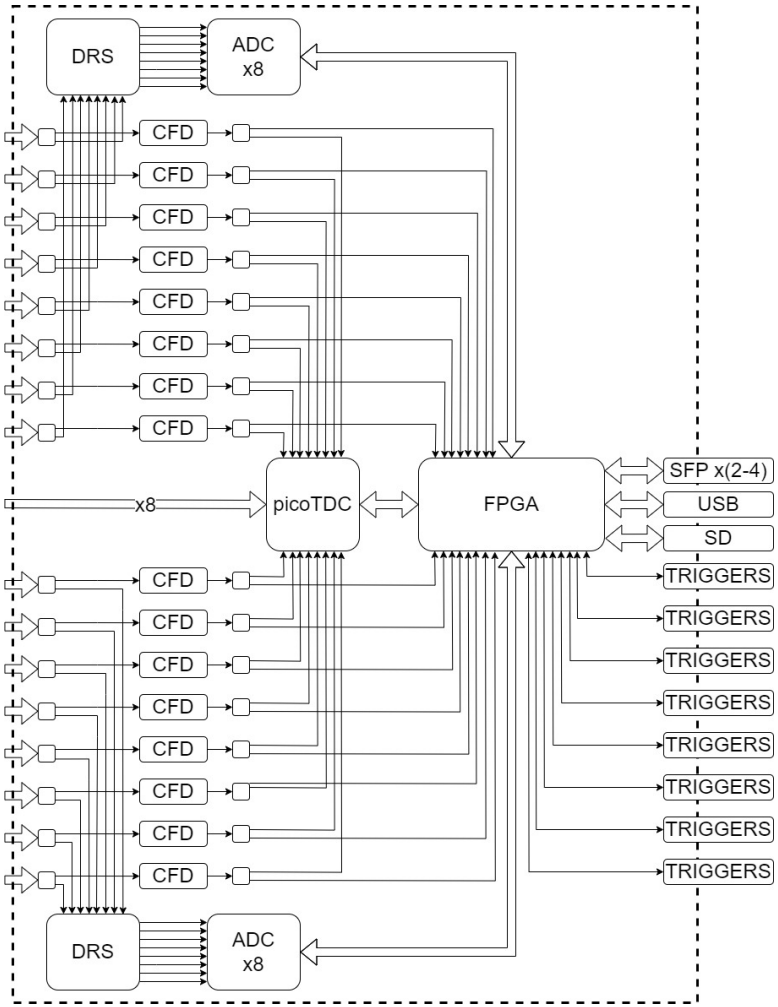

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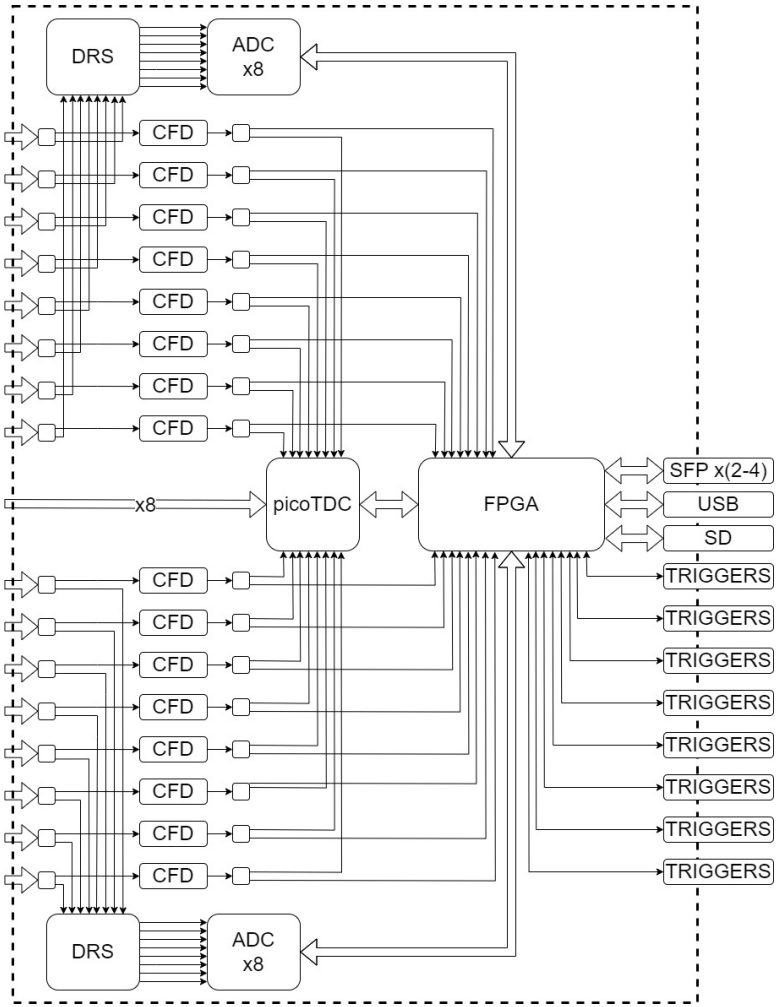

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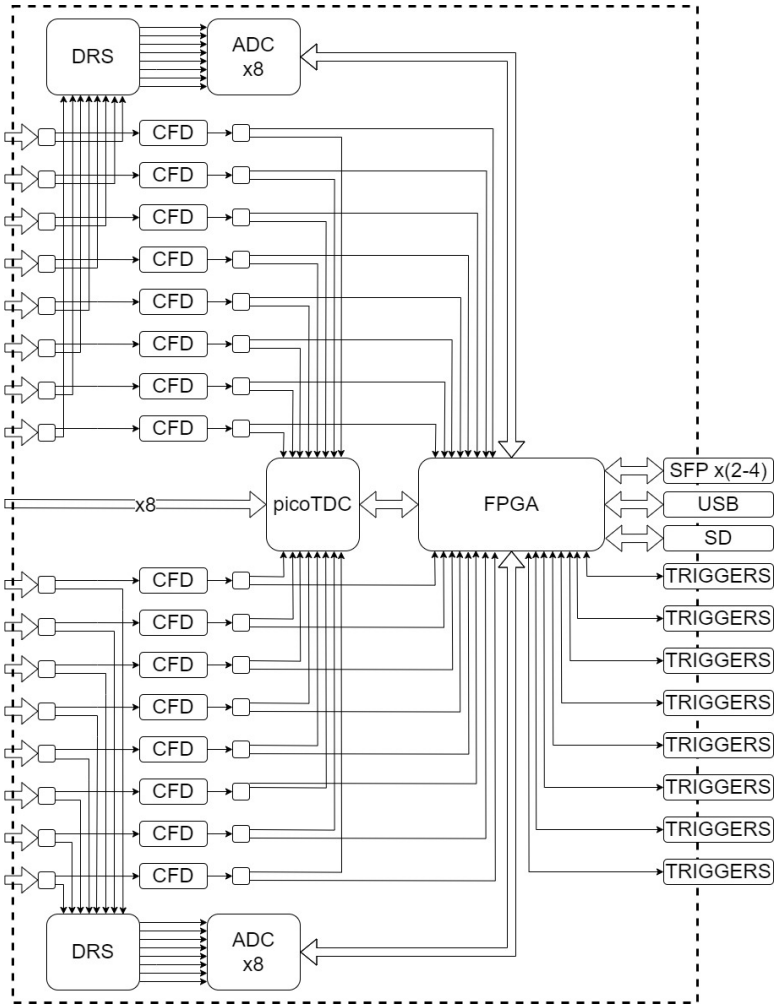

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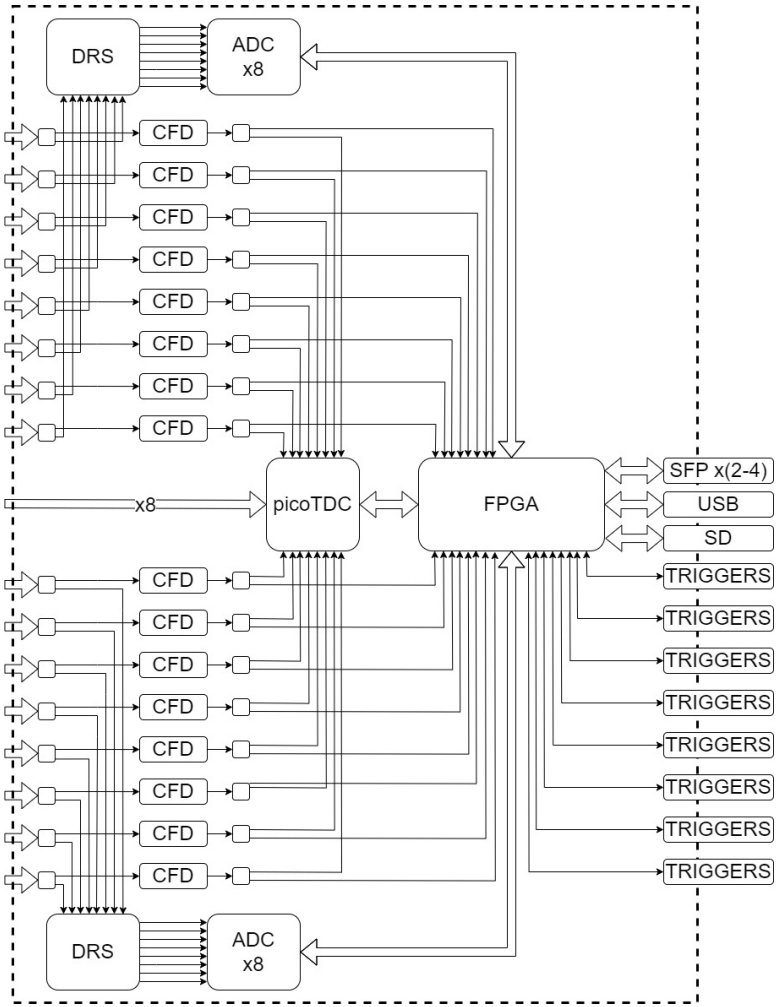

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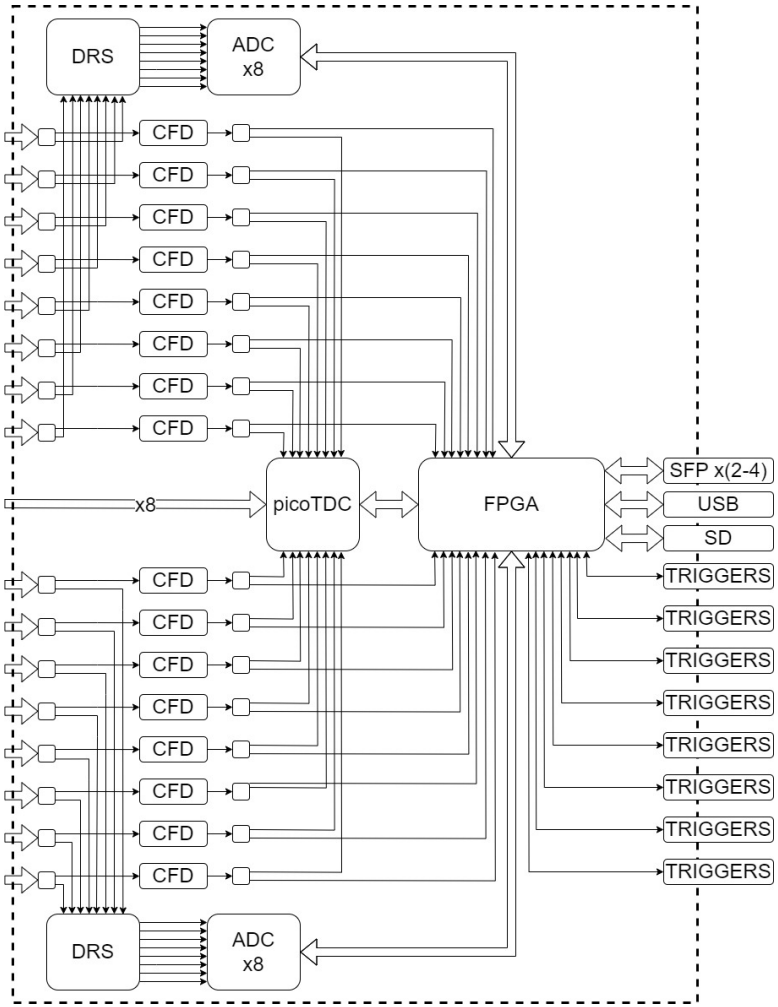

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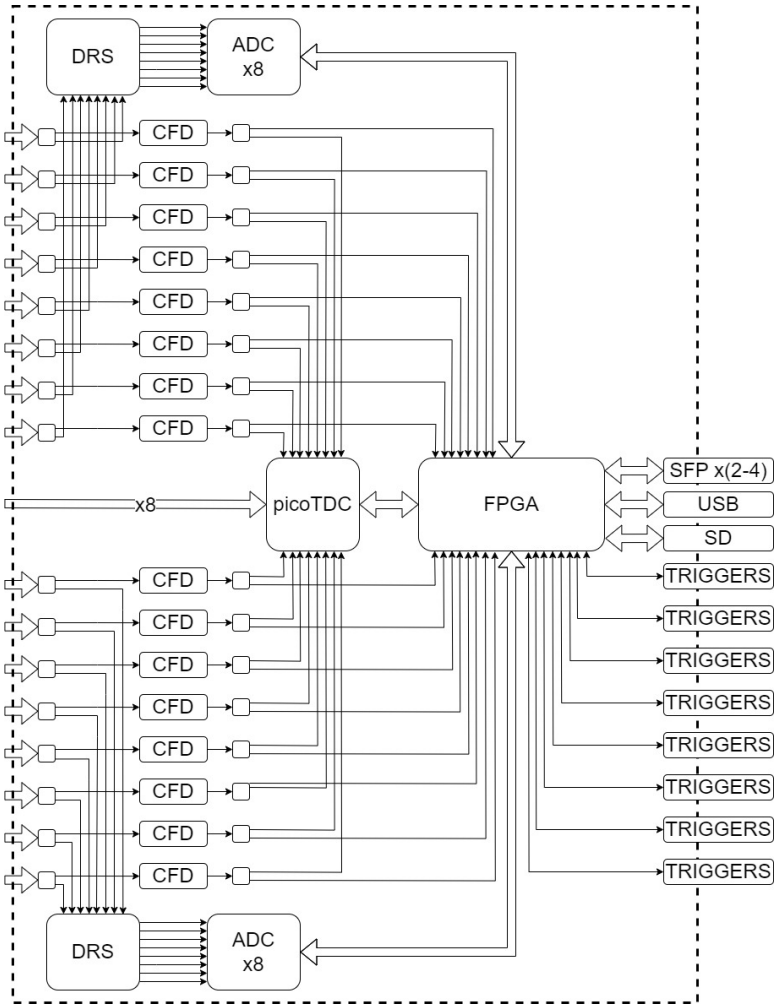

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- FPGA will have ARM processor capable to run DAQ node on the board
- Direct data transfer by fiber optic Ethernet (1G or 10G) directly to the Server Room

The End

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Thank You