Recovery of malfunctioning data transfer of readout in sPHENIX-INTT detector

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Tomoki Harada, Rikkyo University, for the sPHENIX Collaboration

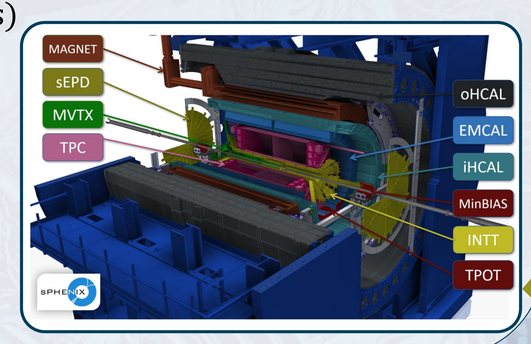
Abstract

sPHENIX is a second-generation experiment at RHIC, dedicated to precision studies of the quark-gluon plasma and the spin structure of the proton. A key component of the tracking system is the Intermediate Silicon Tracker (INTT), a two-layer barrel strip detector providing precise vertex reconstruction and bunch-by-bunch timing resolution essential for polarized p+p physics. Since its commissioning in 2023, the INTT has been operating with excellent stability and performance. During data analysis, however, a characteristic issue was identified: approximately 2% of readout chips are found to transmit only half of detected hits downstream data acquisition system, resulting in so-called *half-entry issue*, where chips record only half of the expected hits due to a malfunction of one output line in the FPHX readout chip. This poster presents a get around solution on this issue, has been a known issue since the early RIKEN test bench stage of the INTT development, trials with different firmware parameters on the detector, and dedicated offline analyses.

sPHENIX detector

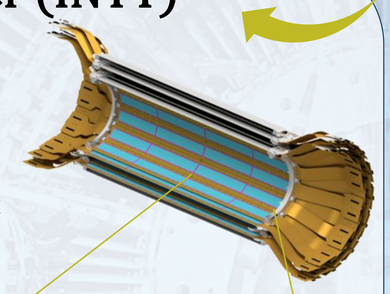
sPHENIX detector subsystems (acceptance: full 2π azimuth, $|\eta| < \sim 1.1$ rapidity)

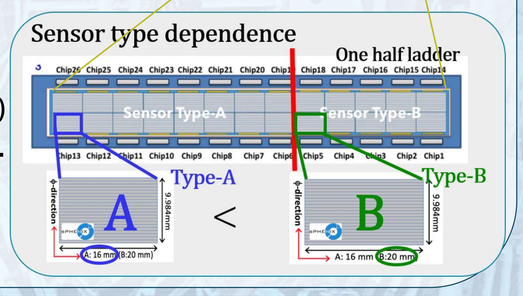
- Tracking system
  - MVTX (Monolithic Active Pixel Sensors)
  - INTT (Intermediate Silicon Tracker)
  - TPC (Time Projection Chamber)
- Calorimetry system
  - EMCal (Electromagnetic Calorimeter)
  - Hcal (Hadronic Calorimeter)
- Trigger and timing detector
  - MBD (Minimum Bias Detector)
- Magnet



INTermediate silicon Tracker (INTT)

- 2-layer barrel geometry
  →56 silicon ladders arranged in two cylindrical layers around the beam pipe.
- High granularity silicon strips
  →78μm pitch in Φ direction, Totaling 370k readout channels
- Sensor thickness
  →320μm ($\approx 0.34\% X_0$)
- Sensor types
  →Type A (16 mm z-length, small rapidity) / Type B (20 mm z-length, large rapidity).
- Bunch-crossing timing capability
  →Timing resolution better than 106 ns (one RHIC bunch spacing).



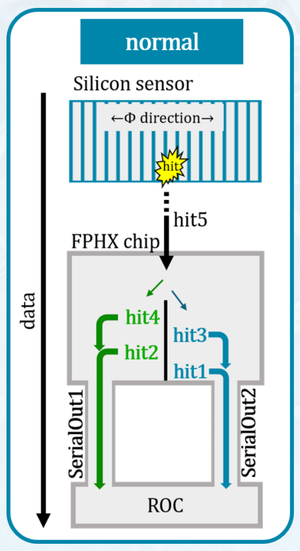


Half entry issue

There are two output lines implemented in the readout chip. Subsequent hits are transmitted through the two lines **alternately**.

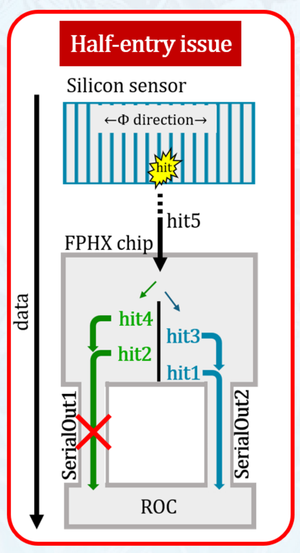
→If **one line is disconnected**, only half of the hits are transferred. this is the **Half-Entry issue.** This issue was observed in approximately **1.4% of all chips.**

🔍 To see how this problem appears in data, look at the **black histogram** (Run **with original setting) on the right**.



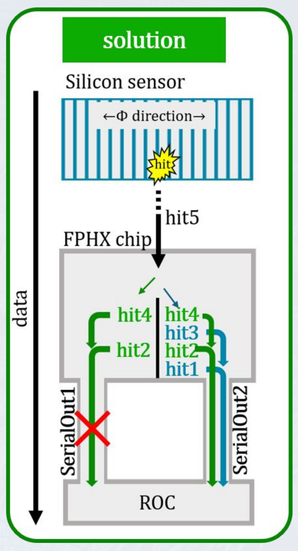
All hits are processed

When one output line **disconnected**,



Half of hits (hit2 & hit4) are lost

Solution

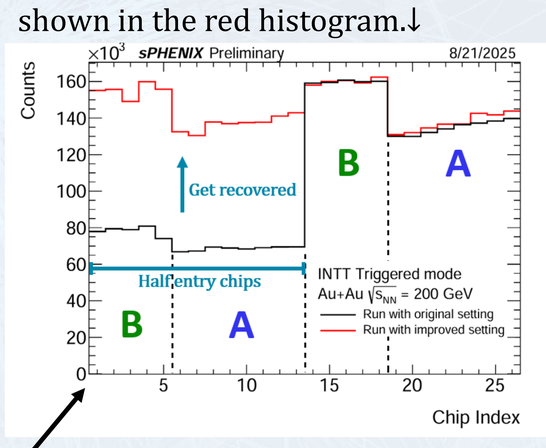


- The Half-Entry issue can be solved by adjusting the **slow-control parameters** of the FPHX chip. Through this parameter control, the chip can be instructed to **clone the hit data and send it through the other output line**, or to **reroute the data flow to avoid the disconnected line.**

- As a result, even if one transfer line is disconnected, the missing hit information is **successfully recovered**, and the detector can operate with the **expected data quality !**

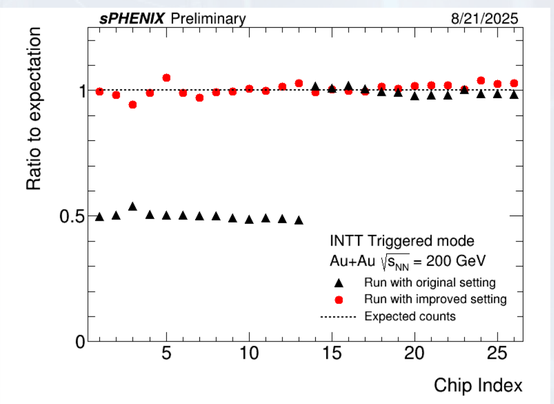
Result

Following the solution described above, the results from the customized run are shown in the red histogram.↓



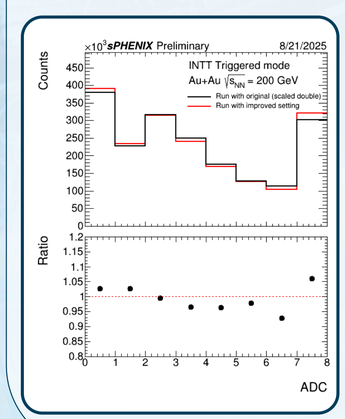
Chip counts comparison between run with original and improved setting. Chip 1 to 13 are all half-entry chips on this half ladder.

Only a limited number of affected chips could be recovered, but clear entry recovery was achieved, salvaging about **1%** of the lost data.

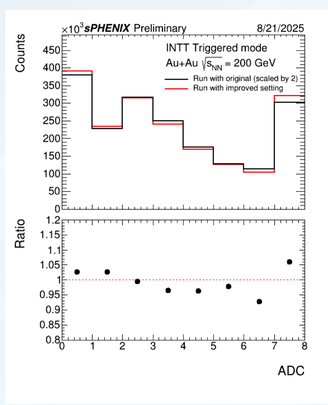


The expected number of entries for each chip was estimated using healthy chips from three reference runs, and the ratios of the observed entries in the ***Run with original setting*** and the ***Run with improved setting*** to these expected values are plotted.

Are recovered hits good ?



half-entry chips data



healthy chips data as comparison

The INTT has a 3-bit ADC, providing values from 0 to 7 (8 discrete levels). In the distribution, ADC 0 is dominated by noise, a clear MIP peak appears around ADC 2, and ADC 7 corresponds to overflow.

These characteristic features are observed both before and after the run, indicating that the recovered data are valid and consistent.

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