Comprehensive introduction to WR

White Rabbit
COLLABORATION

Training material

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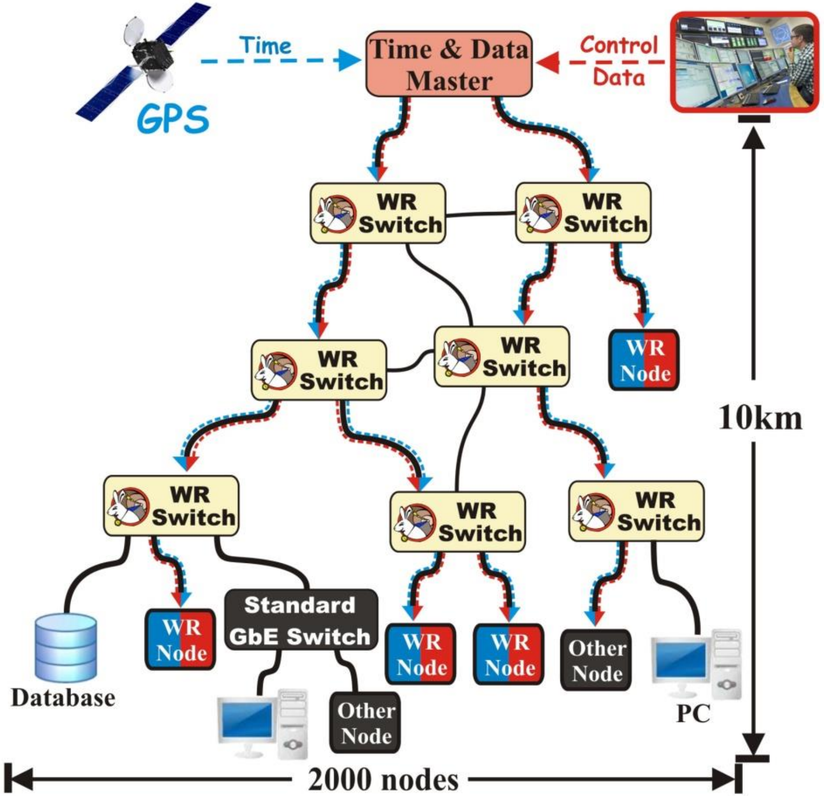
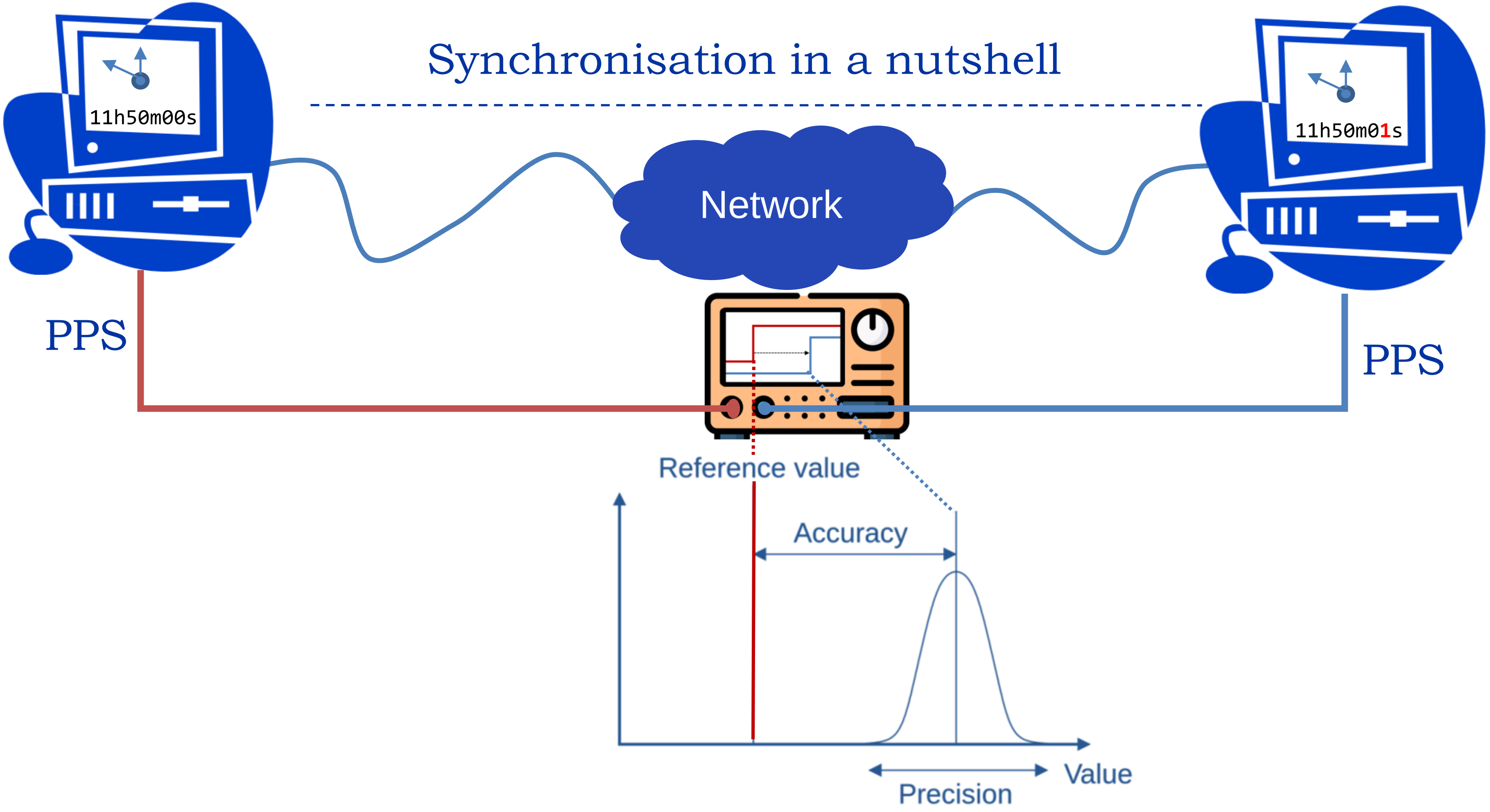
WR Collaboration / CERN

What is White Rabbit?

- Based on well-established standards
  - Ethernet (IEEE 802.3)
  - Bridged Local Area Network (IEEE 802.1Q)
  - Precision Time Protocol (IEEE 1588)
- Extends standards to provide
  - Sub-ns synchronisation
  - Deterministic data transfer
- Initial specs: 10km links and up to 2000 nodes
- Plug and play
- Open source & commercially available



Synchronisation in a nutshell



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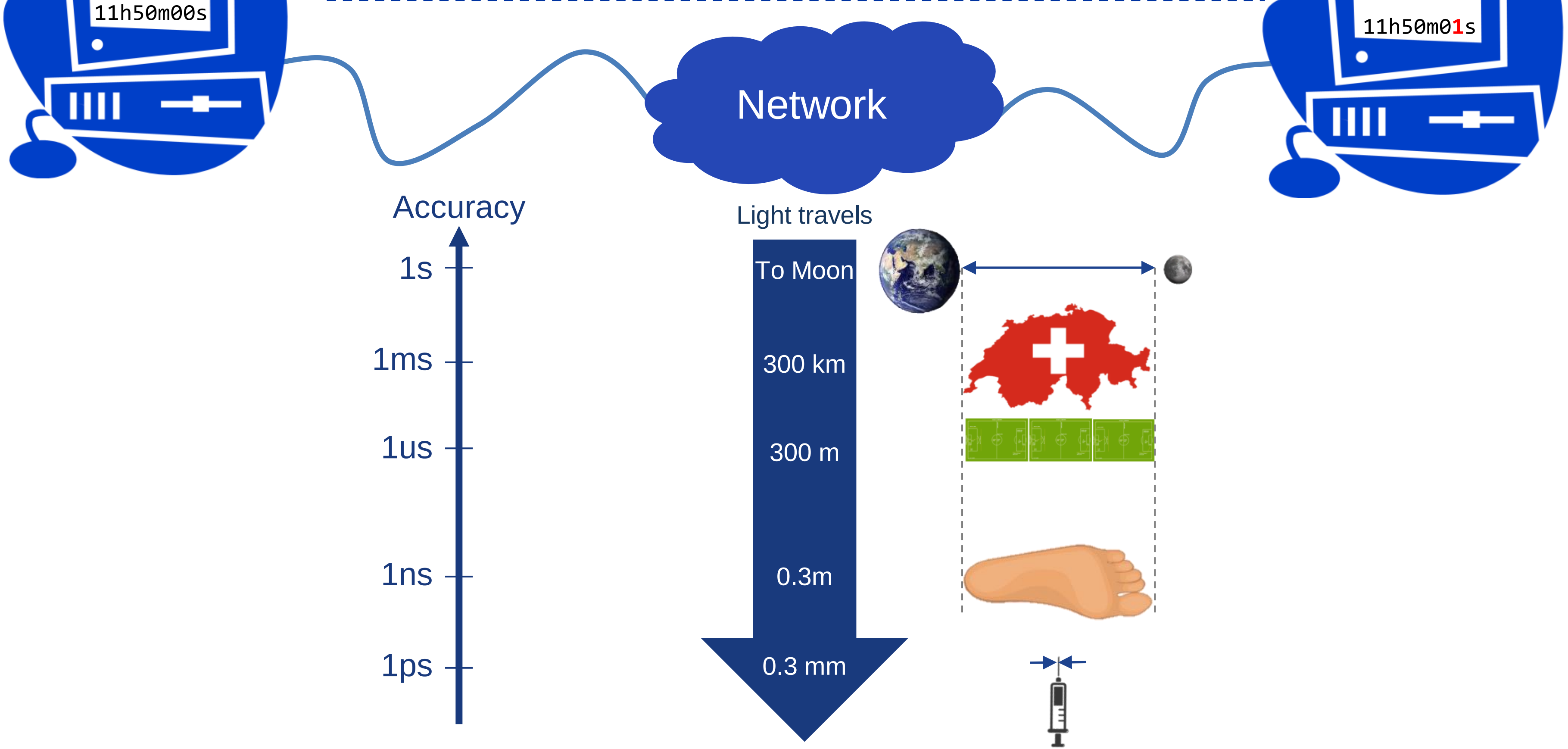


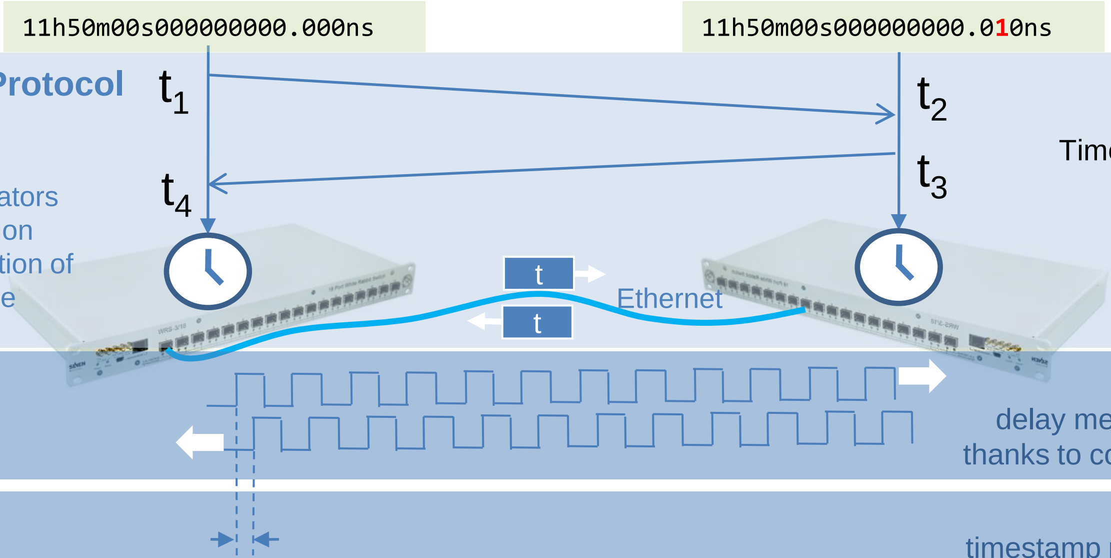
White Rabbit operation in a nutshell

White Rabbit = PTP + L1 syntonisation + phase detection + asymmetry correction

Precision Time Protocol (PTP, IEEE 1588)

PTP limitations:

- Free-running oscillators
- Timestamp resolution
- Symmetry assumption of medium & hardware



$$\text{Time\_cor} = \frac{(t_4 - t_1) - (t_3 - t_2)}{2} + \text{asym}$$

Frequency transfer

Enhance delay measurement thanks to common freq

Phase detection

Phase offset with ps precision

Enhance timestamp precision to ps level by using phase detection techniques

Asymmetry corrections

- Single bidirectional fiber
- Link delay model
- Calibration

Enhance time corrections accuracy by automatic medium asymmetry calculation and calibration of hardware delays

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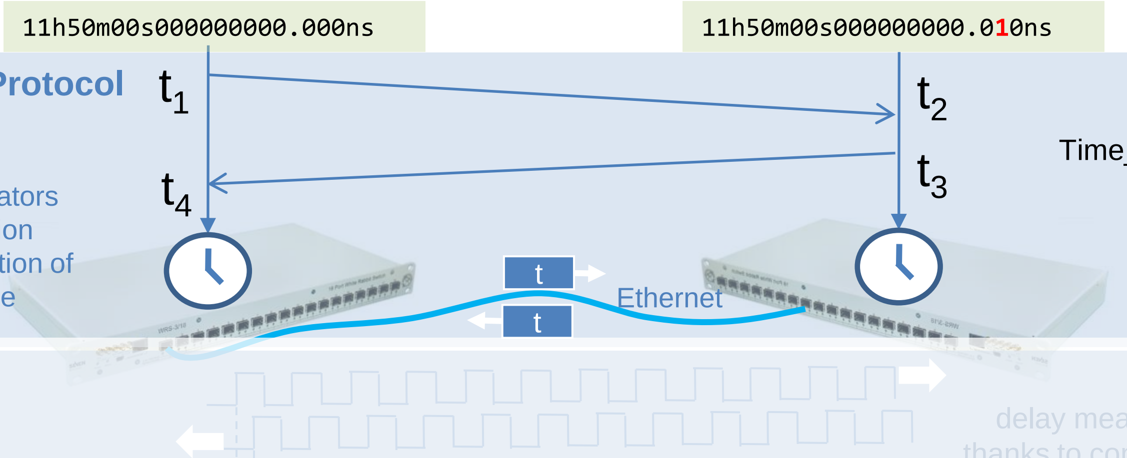

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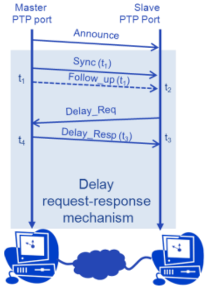
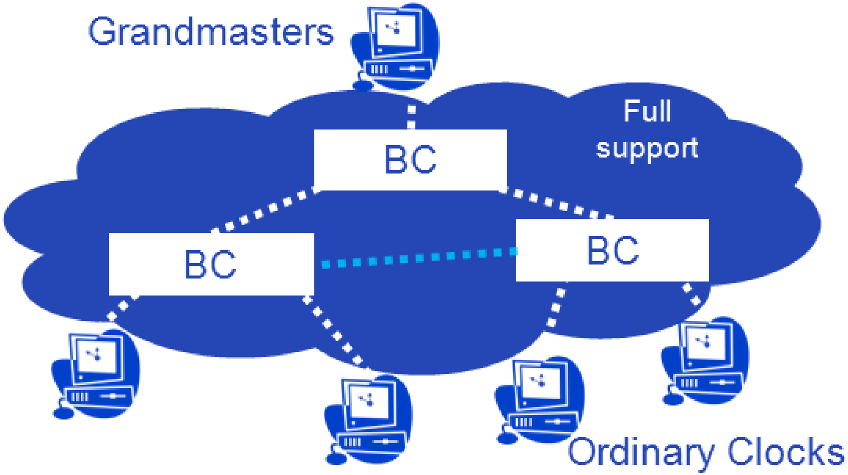
PTP overview

- Packet-based hierarchical time-transfer protocol
- PTP messages exchanged (relevant for WR)
  - Announce
    - Information needed to establish timing hierarchy (next slide)
  - Delay Request-response mechanism
    - Sync, Delay_Req, Delay_Resp, Follow_up (for two step)
    - Used to calculate delay and offset on the slave side
  - Optional: Signaling
    - Used to pass information for optional features
- Type-Length-Value (TLV) extension mechanism
  - Used to pass information for optional features
  - Can be attached to any time of PTP Message
- Hierarchical distribution with master-slave hops
  - Grandmaster – single source of time for entire network
  - Boundary Clock – relies time downstream
  - Ordinary Clock – consumer of time

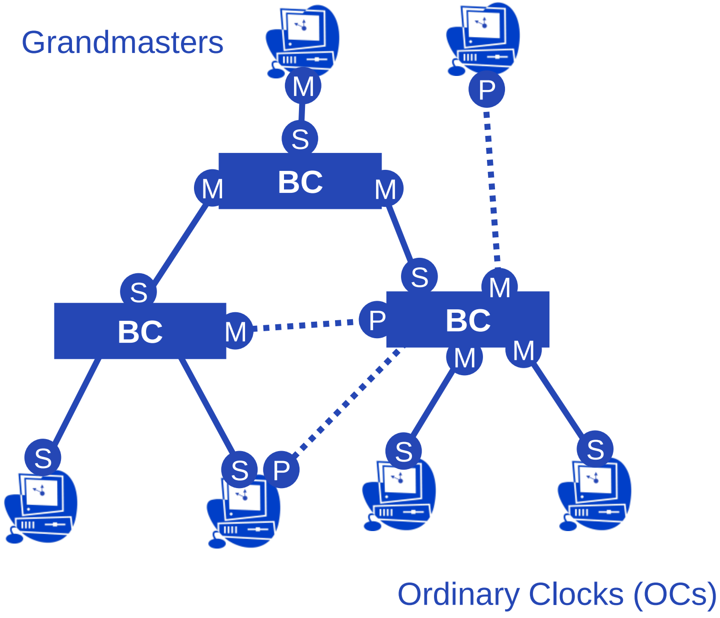




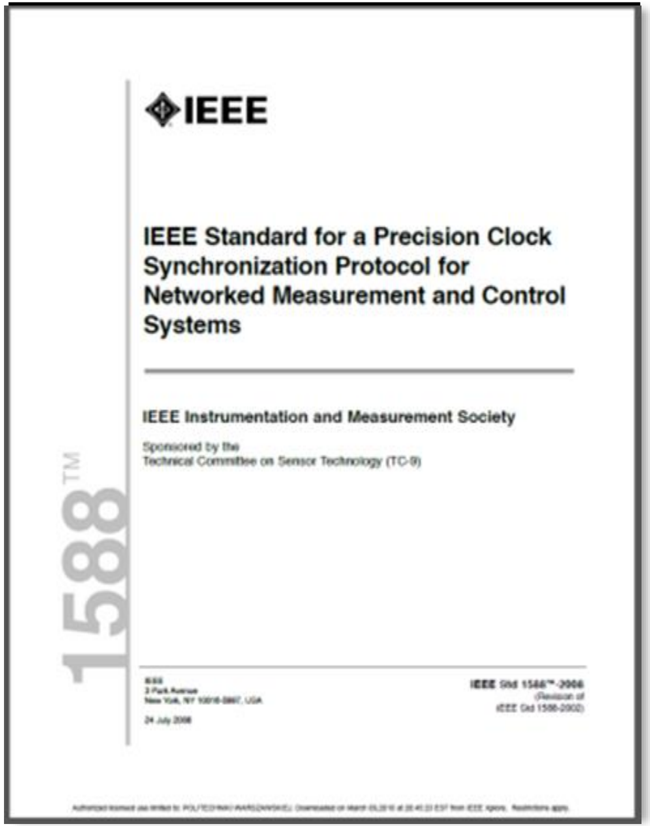
Timing Hierarchy

Two mechanisms in PTP to establish timing hierarhcy

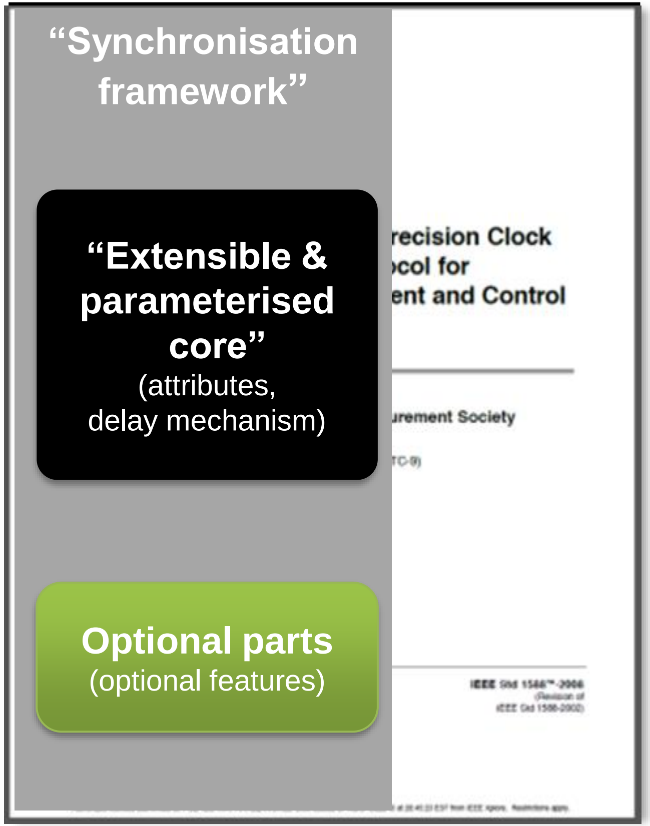
- Best Master Clock Algorithm (BMCA)
  - Based on information from Announce and local config
  - Distance-vector algorithm run individually on each devices
  - Selects one Grandmaster for entire network
  - Recommends state of each port:
    - Master (transmitting time)
    - Slave (receiving time)
    - Passive (redundant)
  - Dynamic reconfiguration when network changes, can take many seconds
- **External port configuration**
  - Manual configuration of each port state, via management
  - Static, no dynamic reconfiguration
  - No handling of mis-configuration



PTP Optional Features and Profiles



PTP Optional Features and Profiles



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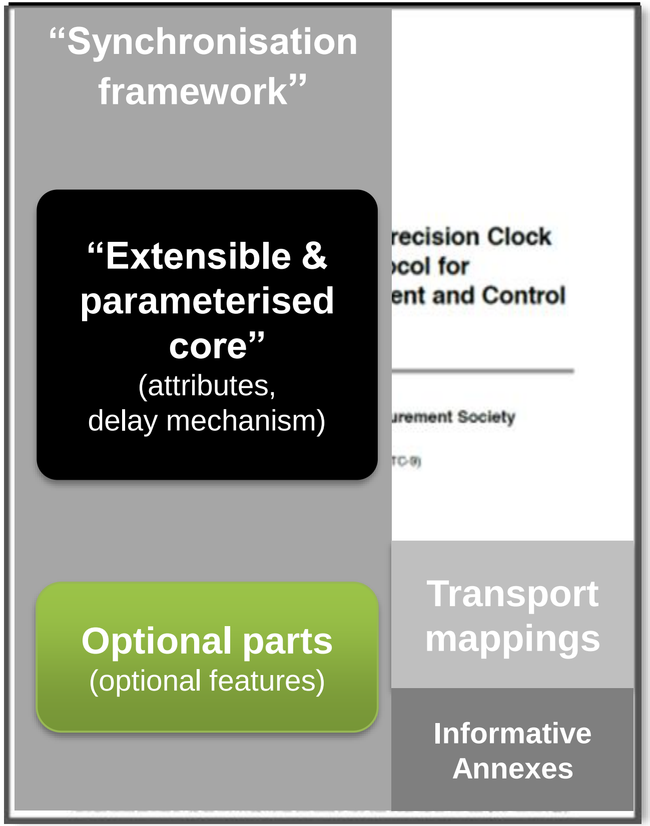

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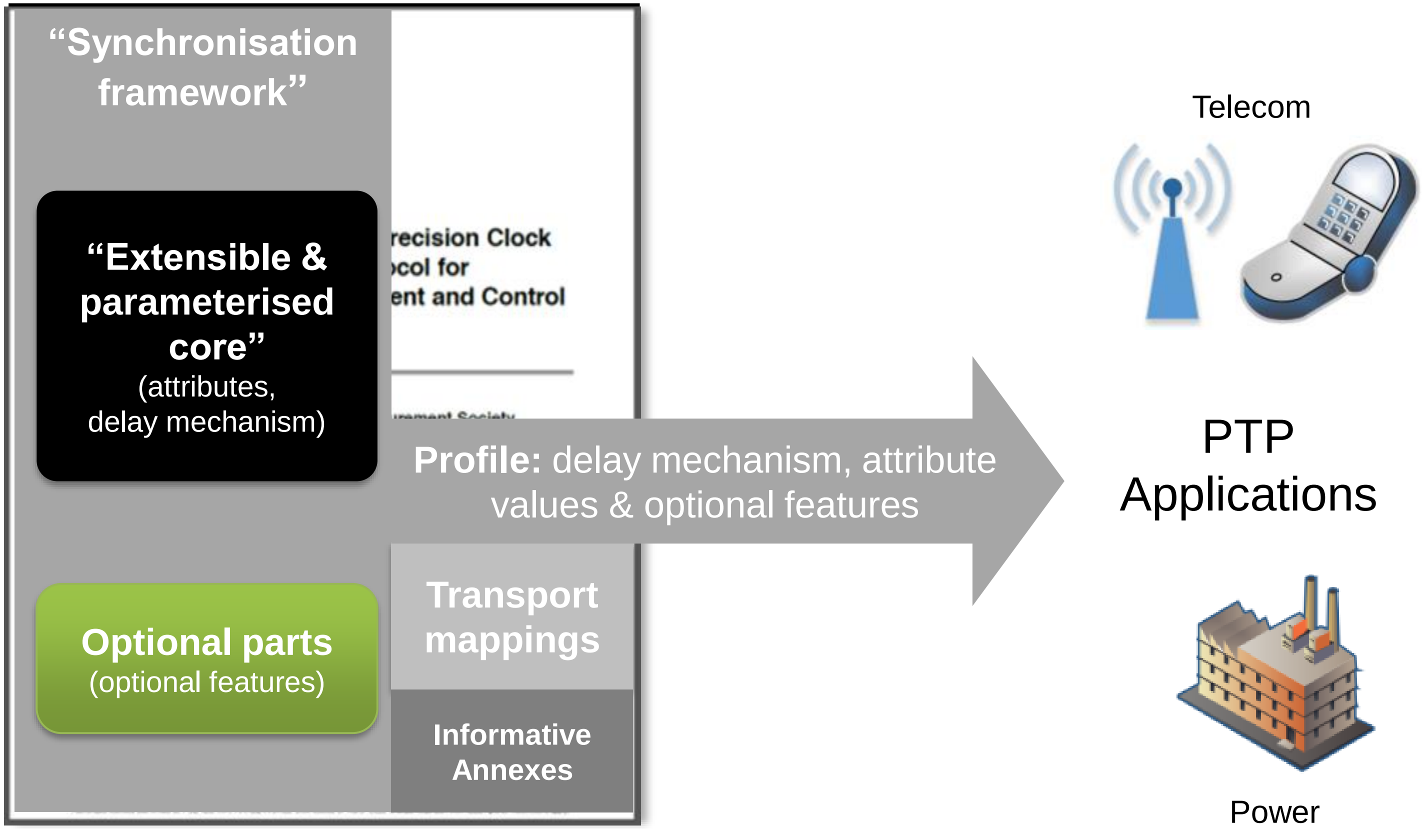

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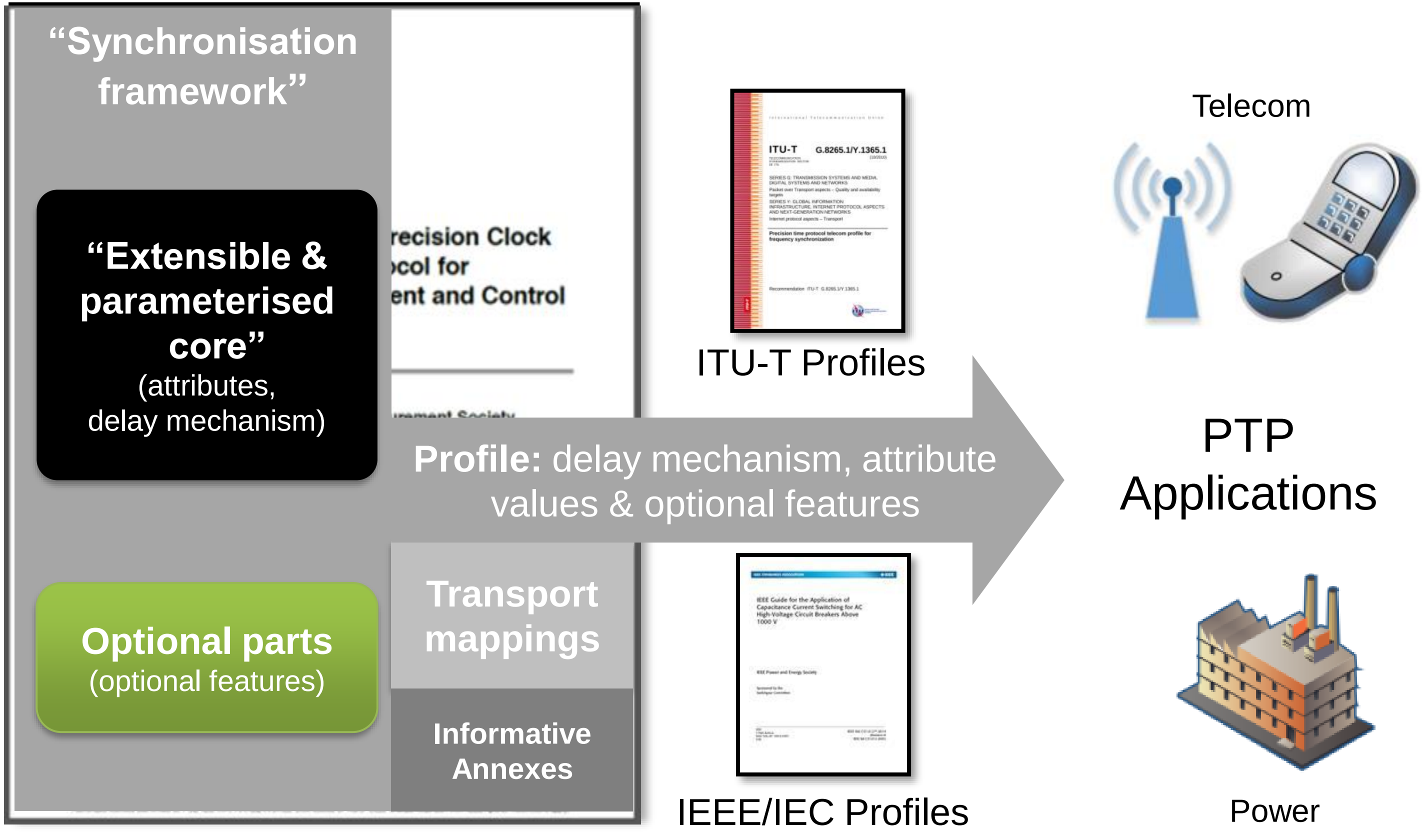

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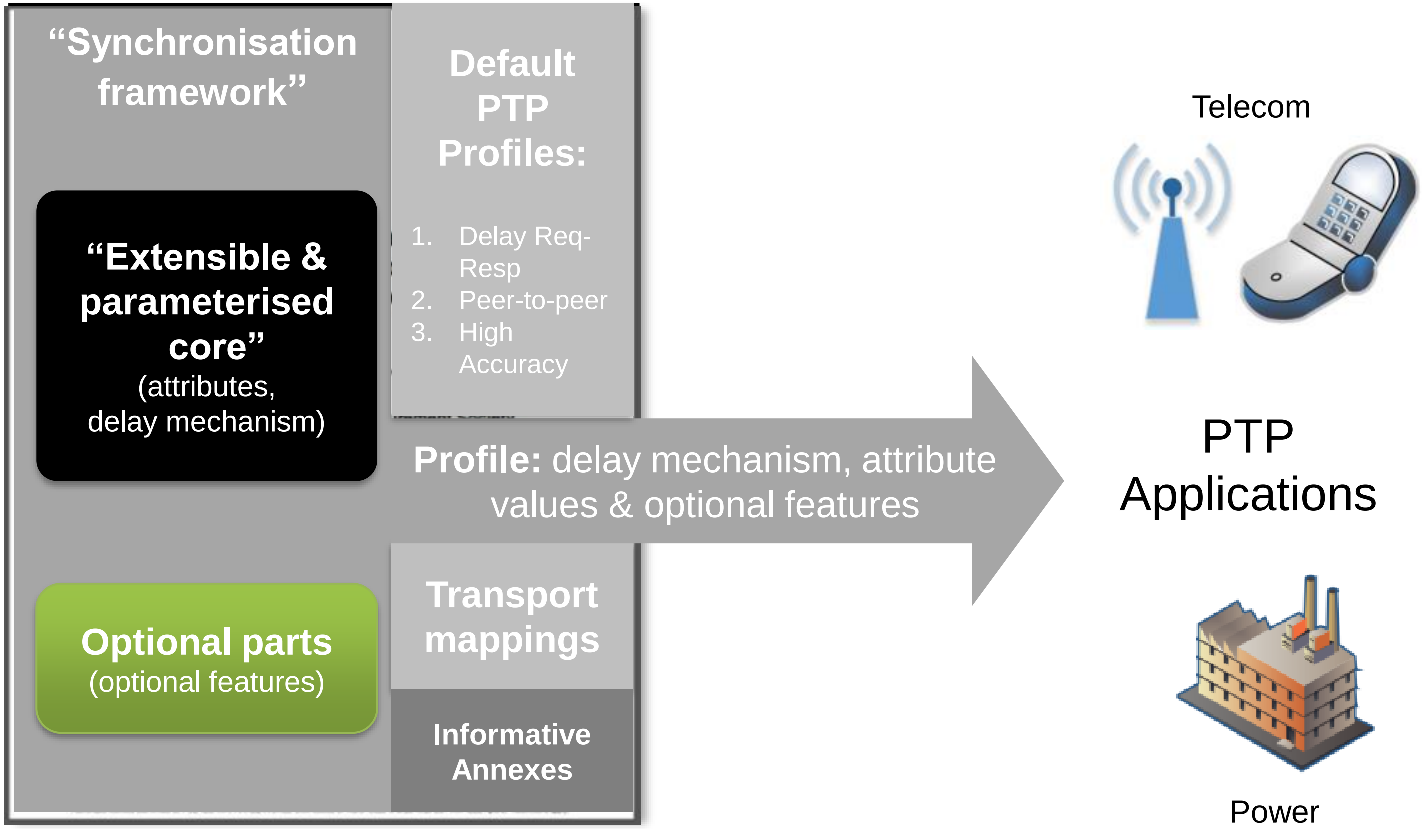
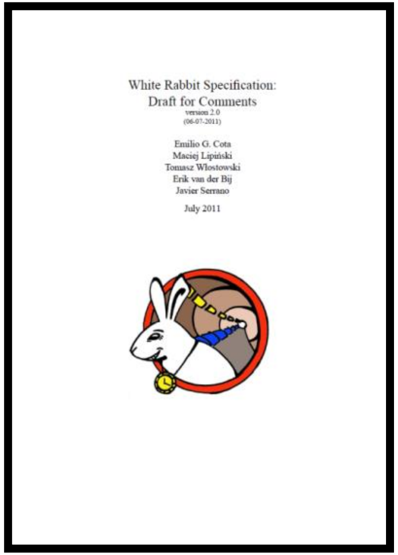


Original WR-PTP Extension and Profile (1)

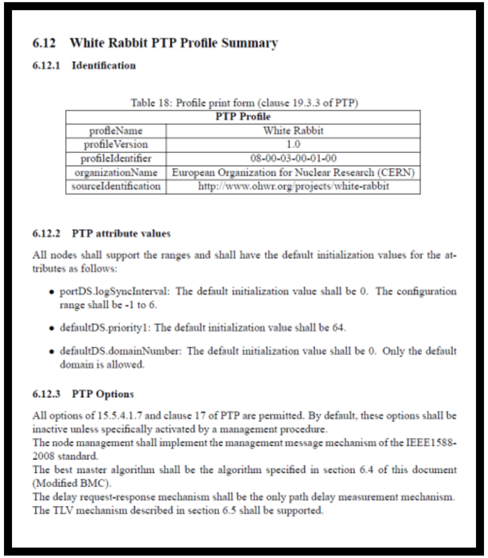
- Specified in: White Rabbit Specification: Draft for Comments, version 2.0, 2011
- Defines WR extensions to PTP Protocols
  - WR-specific Data Set Fields
  - Modified BMCA – obsolete
  - WR TLVs attached to Announce and Signaling messages
  - User-defined events in PTP State Machine
  - WR State Machine
- Defines WR-PTP Profile
  - Uses the WR extensions
  - Uses CERN OUI (“unofficial PTP Profile)
- Describes:
  - Link Delay Model
  - Delay Asymmetry Calculations
  - Hardware Support



White Rabbit Specification:
Draft for Comments
version 2.0
(06-07-2011)

Emilio G. Cota
Maciej Lipiński
Tomasz Wlostowski
Erik van der Bij
Javier Serrano

July 2011



6.12 White Rabbit PTP Profile Summary

6.12.1 Identification

Table 18: Profile print form (clause 19.3.3 of PTP)

PTP Profile	
profileName	White Rabbit
profileVersion	1.0
profileIdentifier	08-00-03-00-01-00
organizationName	European Organization for Nuclear Research (CERN)
sourceIdentification	http://www.ohwr.org/projects/white-rabbit

6.12.2 PTP attribute values

All nodes shall support the ranges and shall have the default initialization values for the attributes as follows:

- portDS.logSyncInterval: The default initialization value shall be 0. The configuration range shall be -1 to 6.
- defaultDS.priority1: The default initialization value shall be 64.
- defaultDS.domainNumber: The default initialization value shall be 0. Only the default domain is allowed.

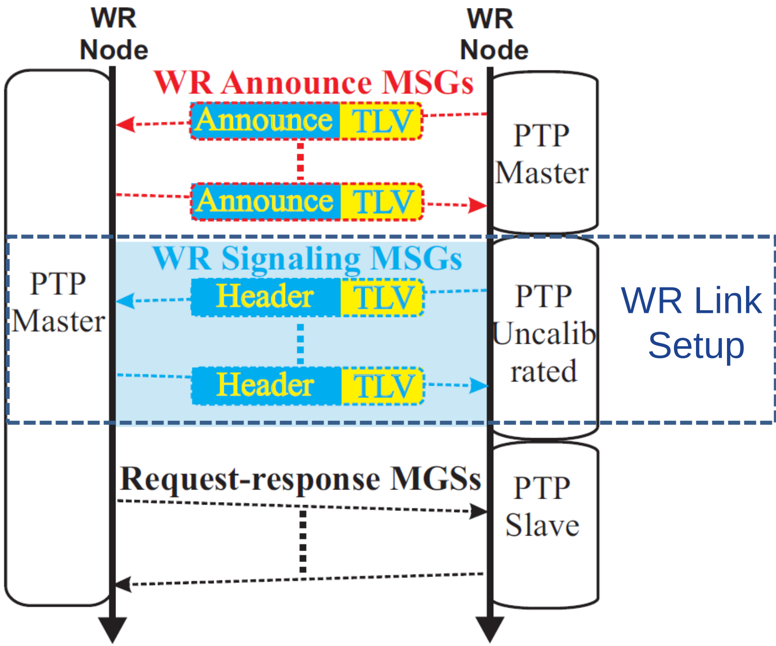
6.12.3 PTP Options

All options of 15.5.4.1.7 and clause 17 of PTP are permitted. By default, these options shall be inactive unless specifically activated by a management procedure.
The node management shall implement the management message mechanism of the IEEE1588-2008 standard.
The best master algorithm shall be the algorithm specified in section 6.4 of this document (Modified BMC).
The delay request-response mechanism shall be the only path delay measurement mechanism.
The TLV mechanism described in section 6.5 shall be supported.

https://white-rabbit.web.cern.ch/documents/WhiteRabbitSpec.v2.0.pdf

Original WR-PTP Extension and Profile (2)

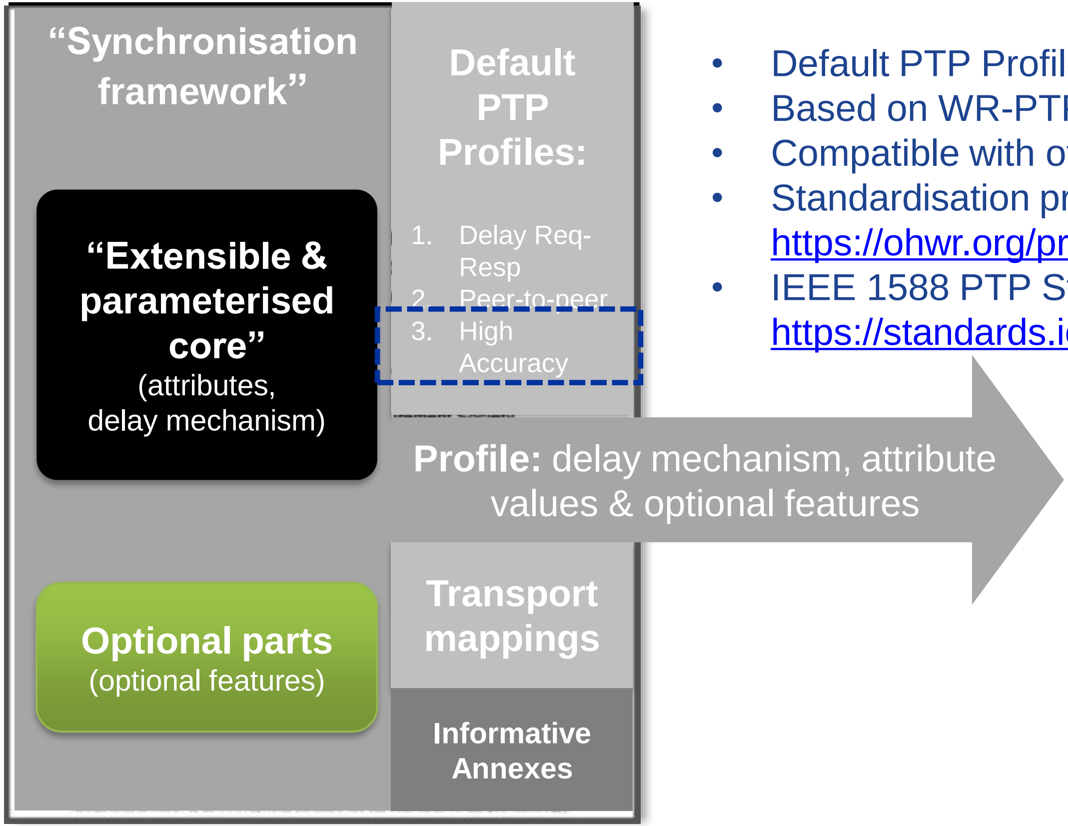
- WR Announce:
  - Includes WR TLV
  - Recognition of WR devices
- WR Link setup
  - Recognition of compatible WR config
  - Frequency locking
  - Calibration - obsolete
  - Exchange of WR-parameters
- Request-response mechanism
  - Sub-ns part of timestamp exchanged in correctionField
  - Nothing specific to WR



Divergences from the published from the WR Spec v2.0:

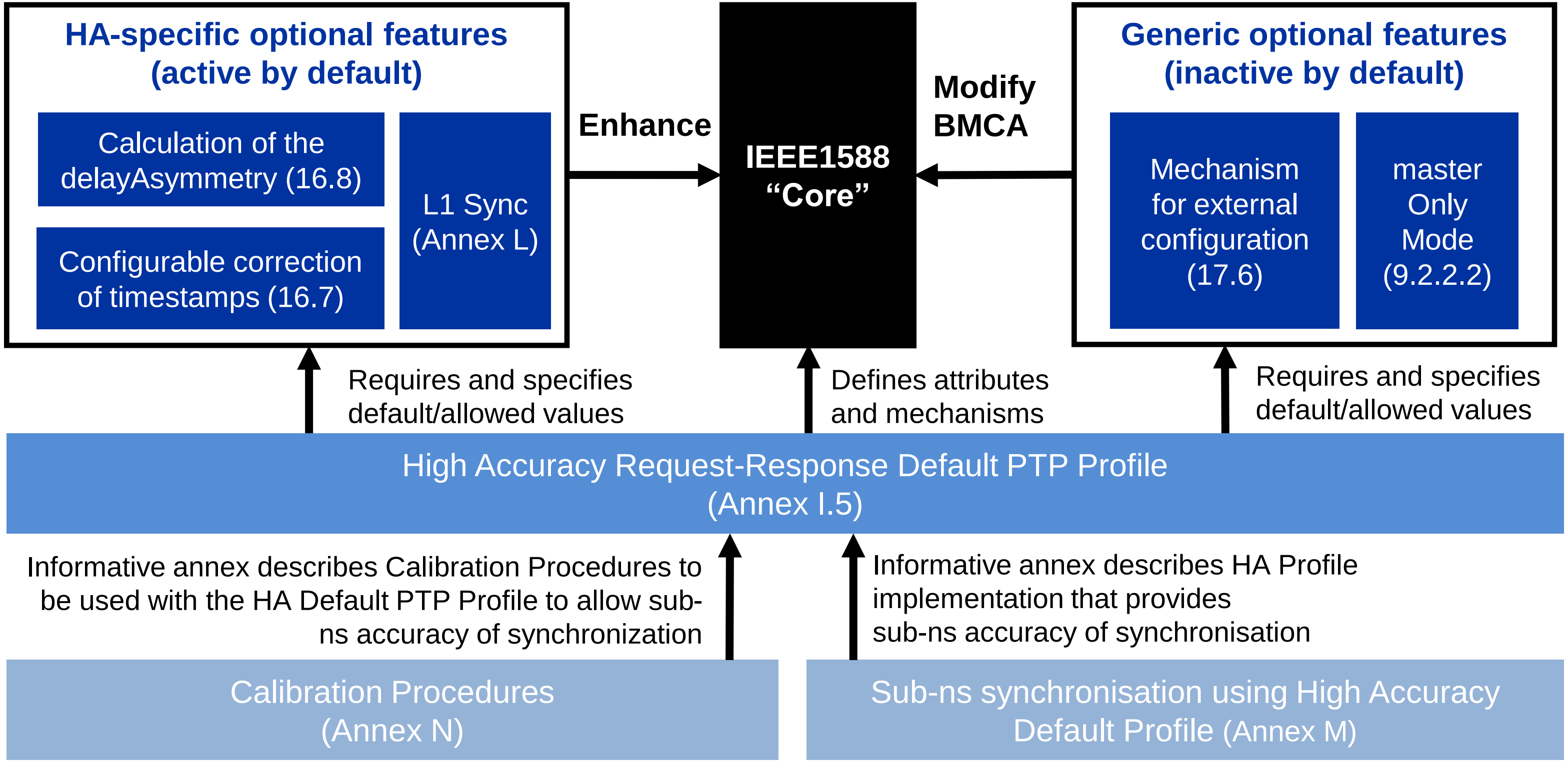
- **The value of magic number in WR TLVs is 0xDEAD (not 0xABCD)**
- **WR state timeouts specified for each WR state**
- **The modified BMCA specified in 6.4 is NOT used, WR devices use**
  - Default BMCA (“auto” mode), or
  - Fixed Port state (Master or Slave)

High Accuracy Default PTP Profile (HA PTP Profile)



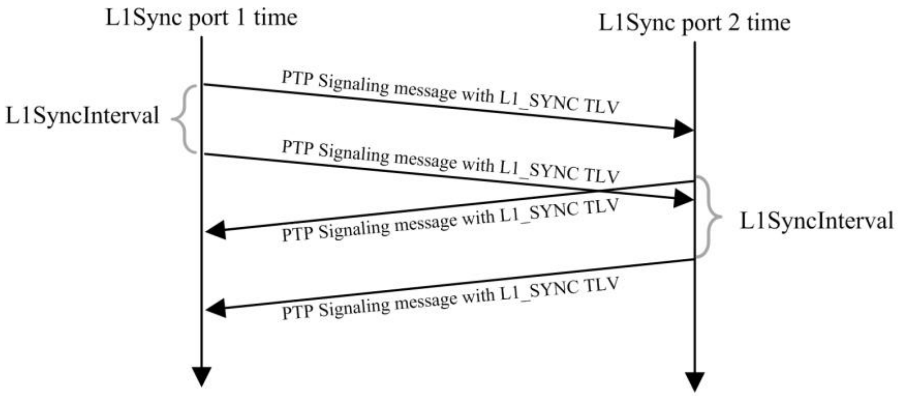
- Default PTP Profile included in 2019 edition
- Based on WR-PTP Profile and WR extension
- Compatible with other Default PTP Profiles
- Standardisation project and details: https://ohwr.org/projects/wr-std/wiki/wrin1588
- IEEE 1588 PTP Std 2019 edition : https://standards.ieee.org/ieee/1588/6825

Components of HA PTP Profile



L1Sync optional feature (extension)

- Data sets: storing config & status
- L1_SYNC TLVs:
  - Detection of L1Sync-supporting PTP Ports
  - Exchange of config/status/parameters
- FSM: control of establishing of frequency transfer (syntonization)
- Improvements with respect to WR-PTP
  - Exchange of information all the time
    (not only at the beginning)
  - Formalized and more flexible relationship between
    - PTP-based time transfer
    - L1-based frequency transfer



WR-PTP vs. HA-PTP

- Protocol-viewpoint: incompatible
- Hardware-viewpoint: no difference
- Detailed comparison: https://ohwr.org/project/wr-std/-/wikis/wrin1588
- WR Switches:
  - Implement and support WR-PTP and HA-PTP
  - Support auto-negotiation between WR-PTP and HA-PTP
- WR Nodes:
  - Implement WR-PTP and HA-PTP but support only one at a time (limited space)

White Rabbit operation in a nutshell

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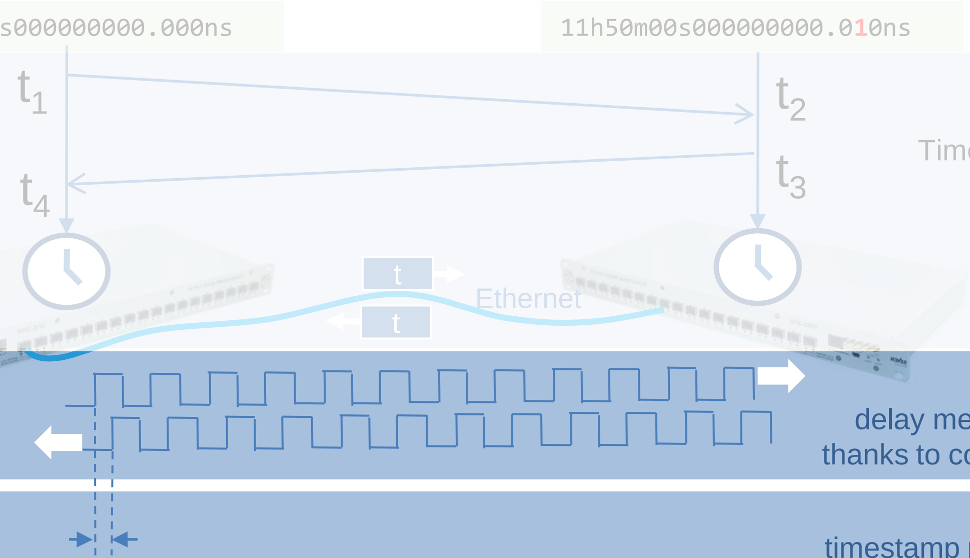

$$Time\_cor = \frac{(t_4 - t_1) - (t_3 - t_2)}{2} + asym$$

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Asymmetry corrections

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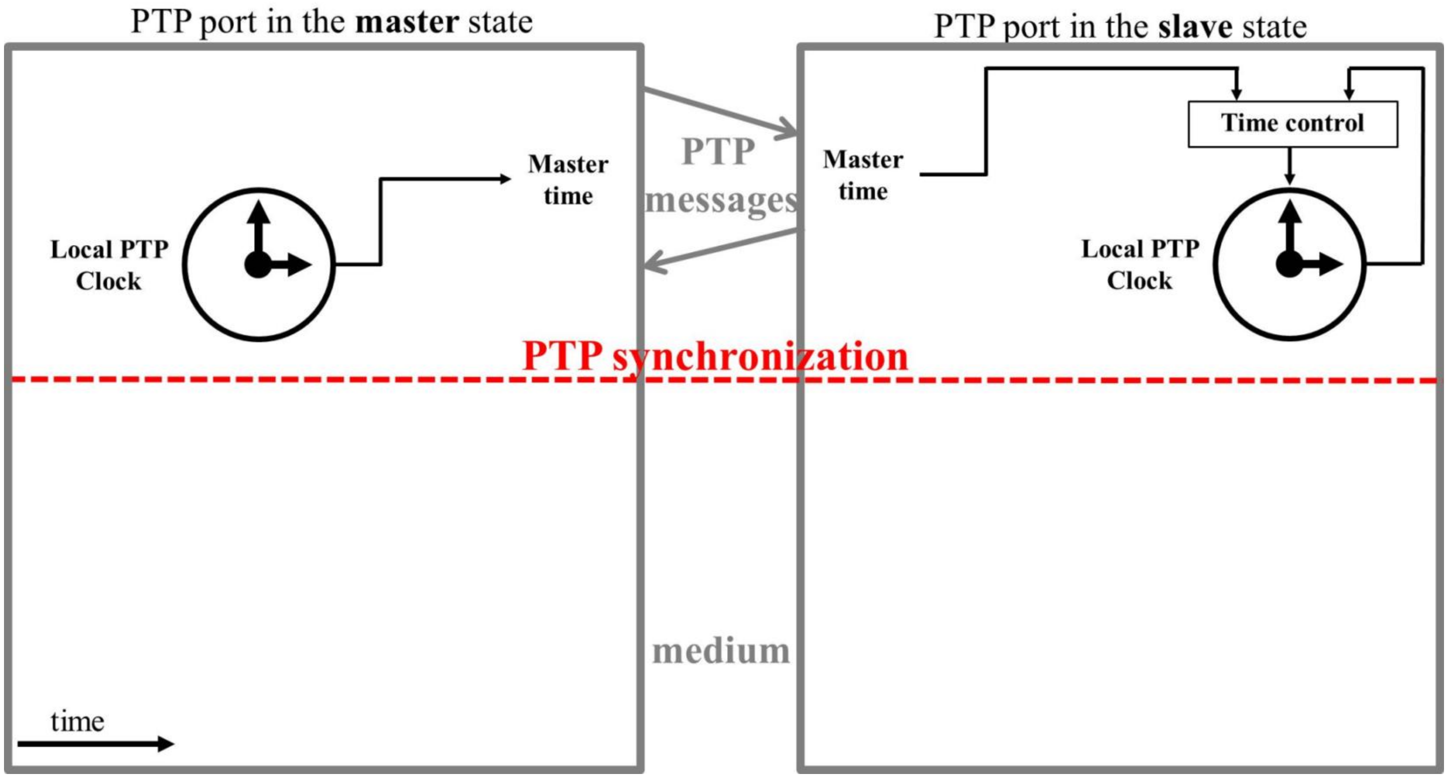
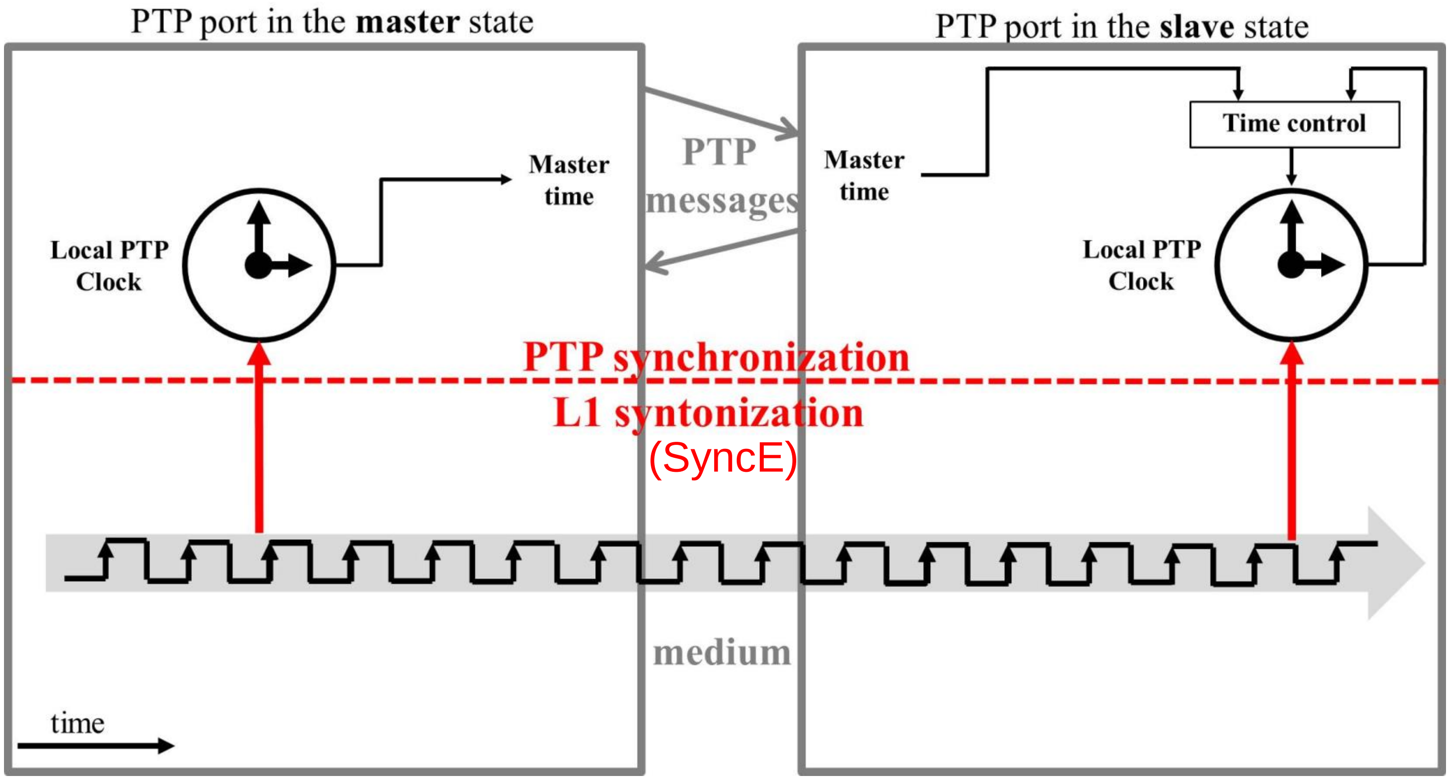
PTP synchronization vs. L1 Syntonization

Typical PTP implementation:



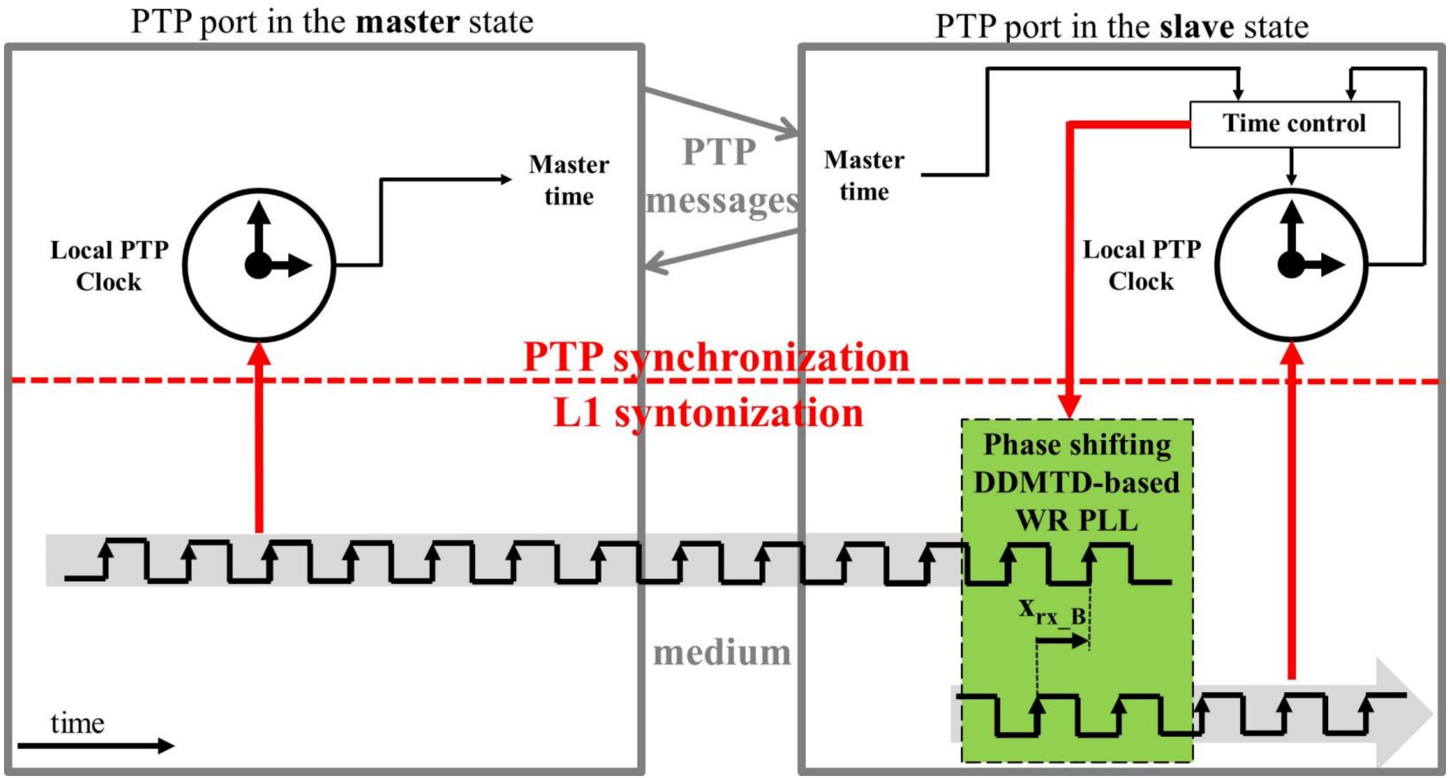
PTP synchronization vs. L1 Syntonization

G.8275.1: PTP telecom profile for time/phase with full support



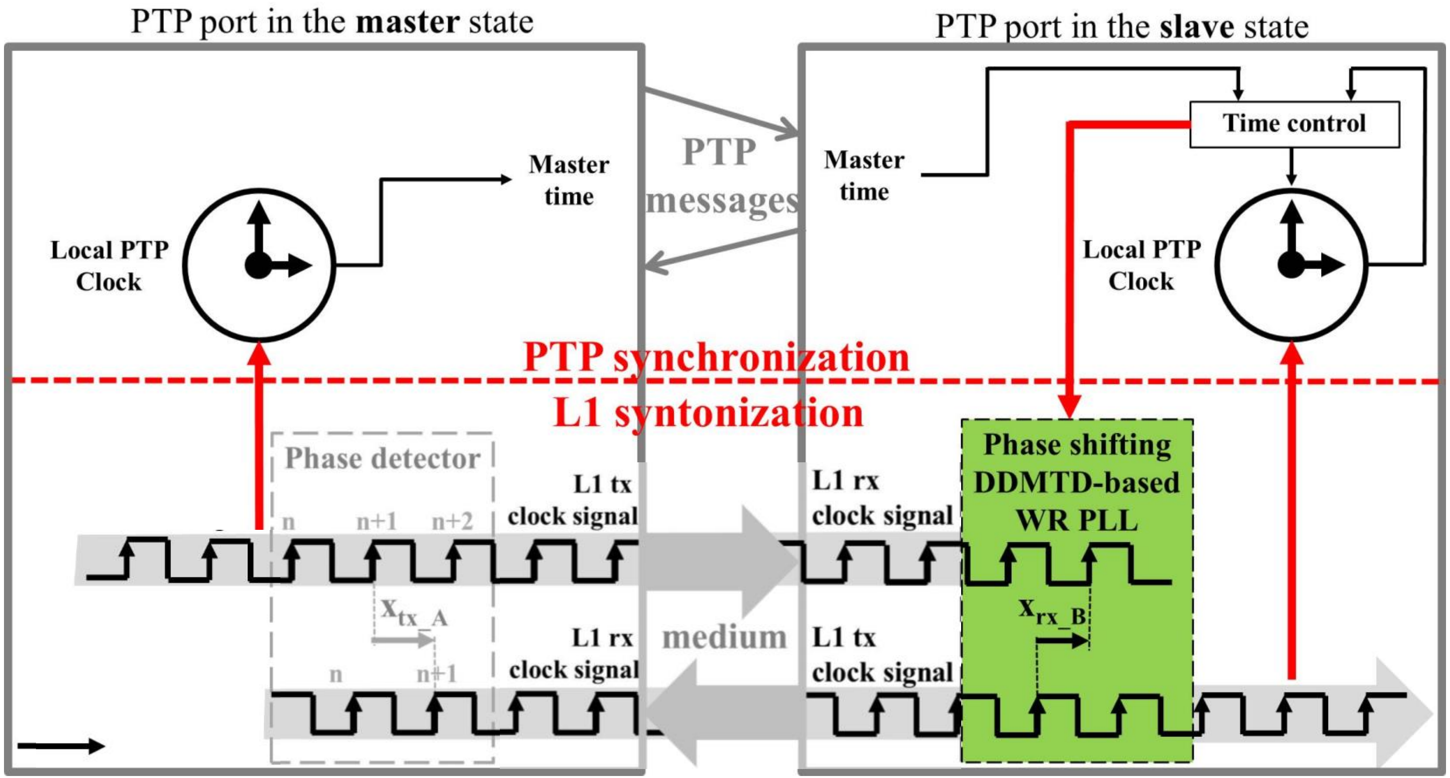
PTP synchronization vs. L1 Syntonization

White Rabbit / High Accuracy Default PTP Profile:



PTP synchronization vs. L1 Syntonization

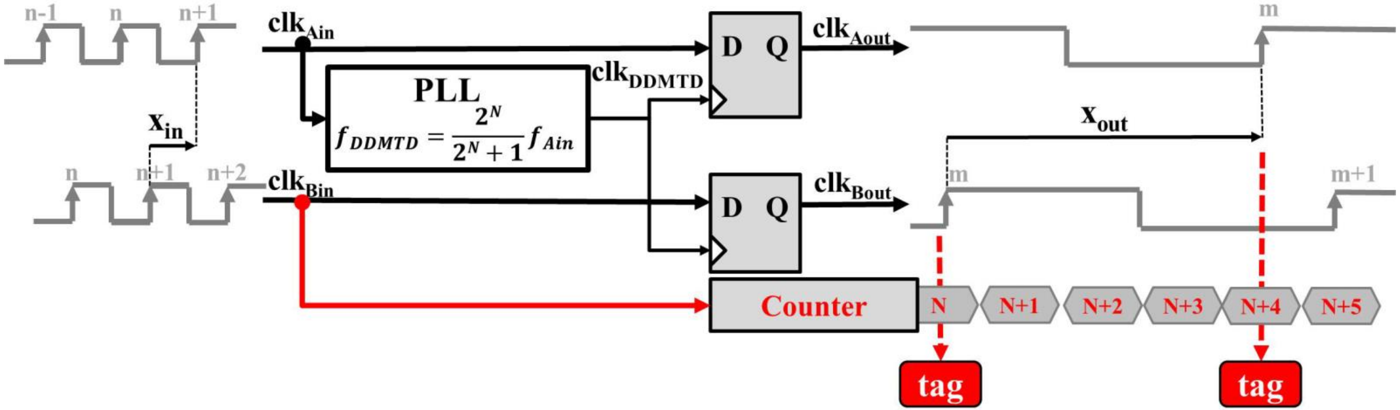
White Rabbit / High Accuracy Default PTP Profile - detailed:



Phase detection

Digital Dual Mixer Time Difference (DDMTD)

- Clever implementation of a phase detector in an FPGA
- WR parameters:
  - clkin = 62:5 MHz
  - clkDDMTD = 62:496185 MHz (N=14)
  - clkout = 3:814 kHz
- Uses D-flip-flops to zoom-in phase offset
- Allows for phase measurements at picosecond level



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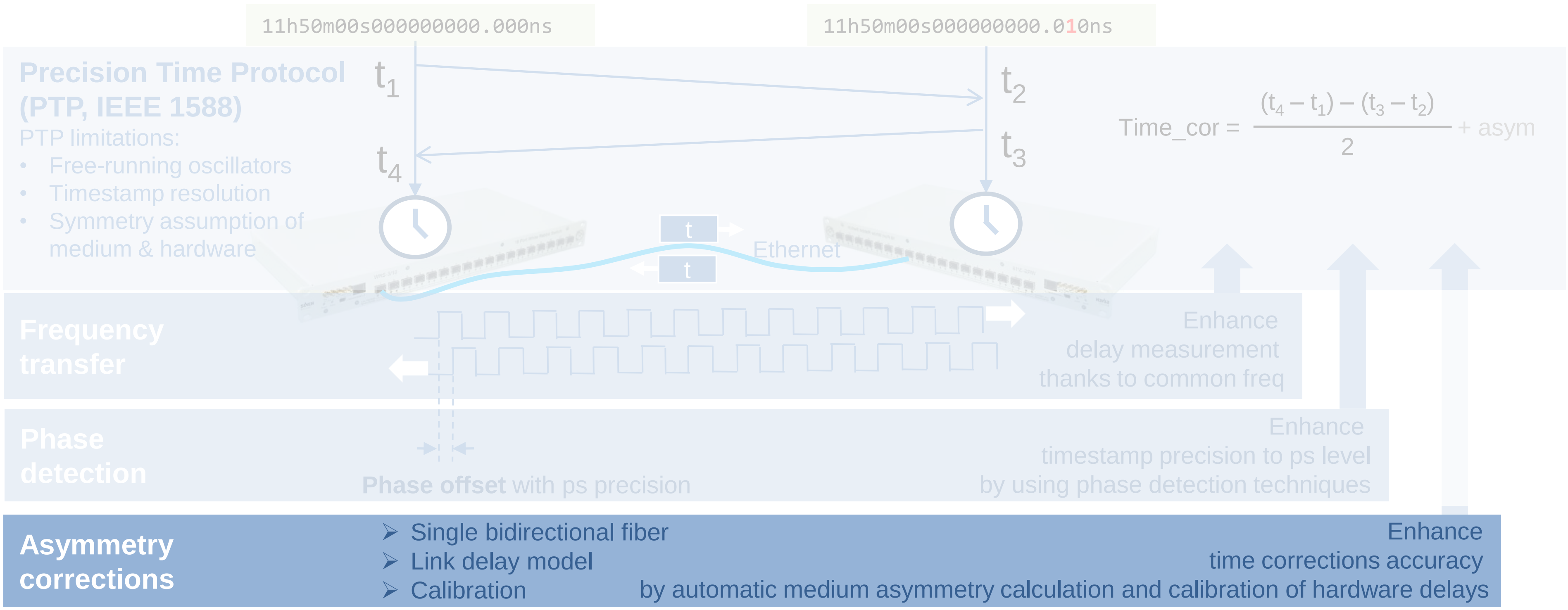
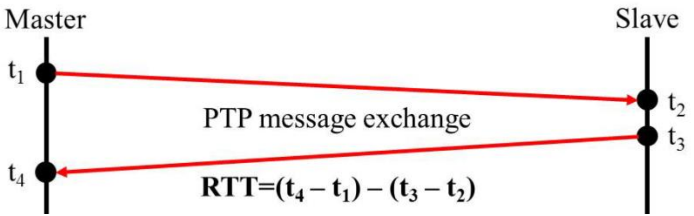


Asymmetries and link delay model

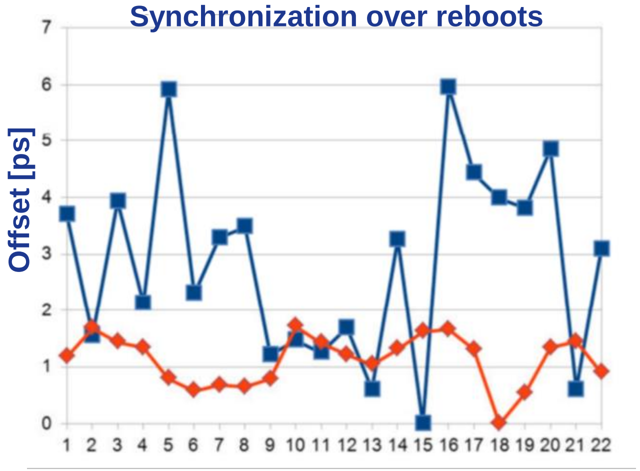
- Correction of RTT for asymmetries



White Rabbit Performance

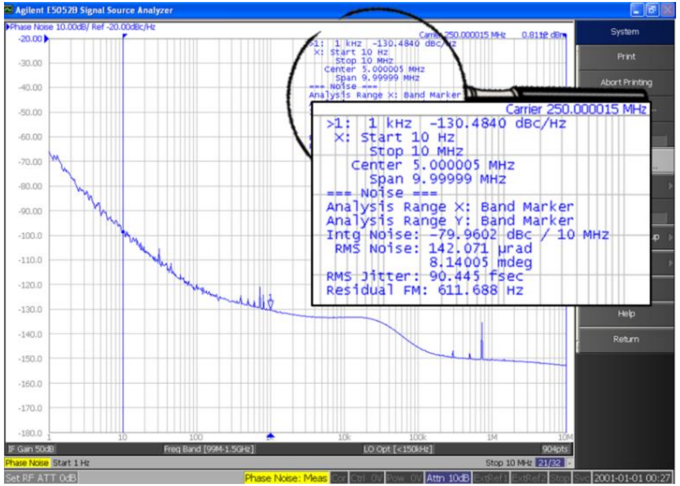
Time transfer performance

- Network-level: < 1ns accuracy
- A single link (<10km): < 20ps accuracy
- Long-distance support: ~1000km
  (up to 100km with < 500ps accuracy)



Frequency transfer performance

- Standard: 11ps RMS
- Low jitter: 2ps RMS
- Best jitter: 100fs RMS



See "Intro to Oscillators" presentation at 16h45 for explanation on frequency measurements

White Rabbit Devices

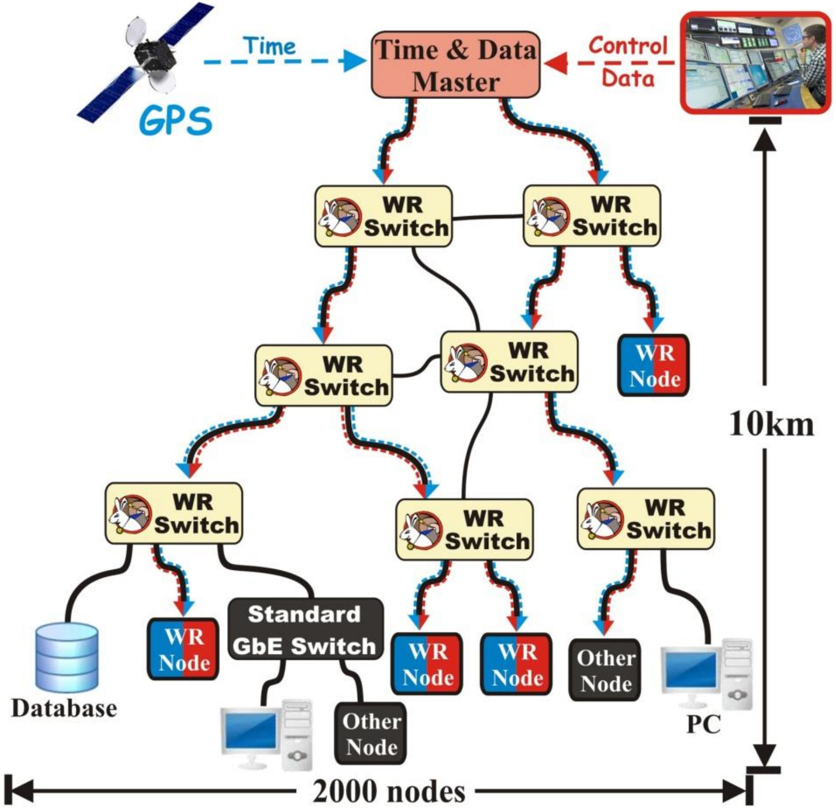
- WR Switch (open-source)
  - HW v3 – current
  - HW v4 – future

- WR Node
  - Open source

  - Proprietary

* Timing fanout

List of WR devices:
https://ohwr.org/project/white-rabbit/-/wikis/WRCompanies



White Rabbit Switch v3

- **Hardware**:
  - 18 ports of 1 Gbps
  - Xilinx Virtex 6 + ARM CPU
  - Main types:
    - Standard
    - Low-jitter

- **Firmware** (software + gateware):
  - Official releases by WR Team at CERN
  - Calibrated to CERN's Golden Calibrator
  - Low Phase Drift Calibration (LPDC)
    - Phase repeatability over link-up/reboot
    - Supported on ports 1-12
  - Current release: v7.0
    - Not all WRS hardware types compatible

WR Switch type	Precision (sdev)		Accuracy (mean)	
	GM-in/out Jitter RMS (1 Hz – 100 kHz)	GM-in/BC-out Jitter RMS (1 Hz – 100 kHz)	Ports 1-12 (LPDC)	Ports 13-18
"Standard"	9ps	11 ps	<20ps	<200ps
"Low jitter"	1ps	< 2 ps		

Compatibility of the official firmware releases with commercially available WR Switches

This table lists for which commercially available WR Switches the release firmware available on this page can be used (i.e., with which WR switches it is compatible).

WR switch name	Type	Vendor	Compatible with official firmware release	Hardware
WRS	Creotech	Standard	v3.3 and later	SCB 3.4
WRS-LJ	Creotech	Low Jitter	v6.0 and later	SCB 3.4+LJD
WRS	Safran	Standard	v3.3 and later	SCB 3.4
WRS-3-LJ/18	Safran	Low Jitter	Not compatible	SCB-LJ 1.0
WRS-3-LJ/18_ (*)	*Safran*	*Low Jitter*	*As of upcoming release*	*SCB-LJ 2.0*
WRS-LJ	OPNT	Low Jitter	v6.0 and later	SCB 3.4.1+LJD
WRS-18A	SyncTech	Low Jitter	v7.0 and later	FL-SCB-v1.5
WRS-18B	SyncTech	Fanless and Low Jitter	v7.0 and later	FL-SCB-v1.5

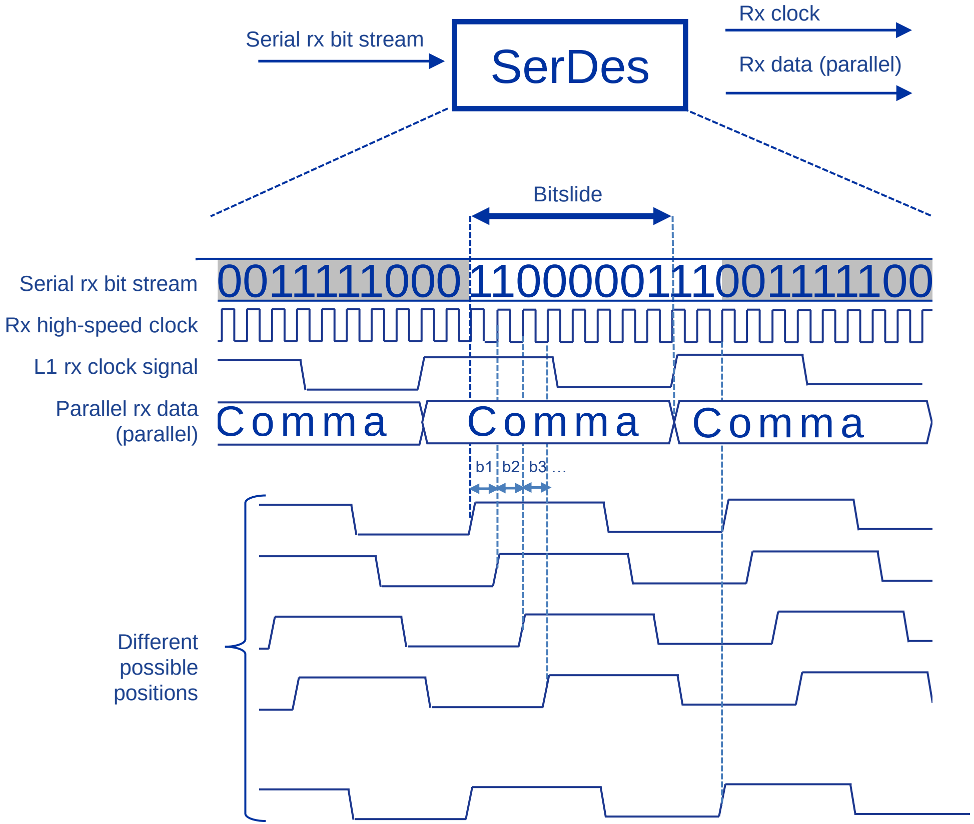
(*) *NOTE: New version of hardware that will be compatible with future official firmware releases, inquire with the company.*

https://ohwr.org/project/wr-switch-sw/-/wikis/home

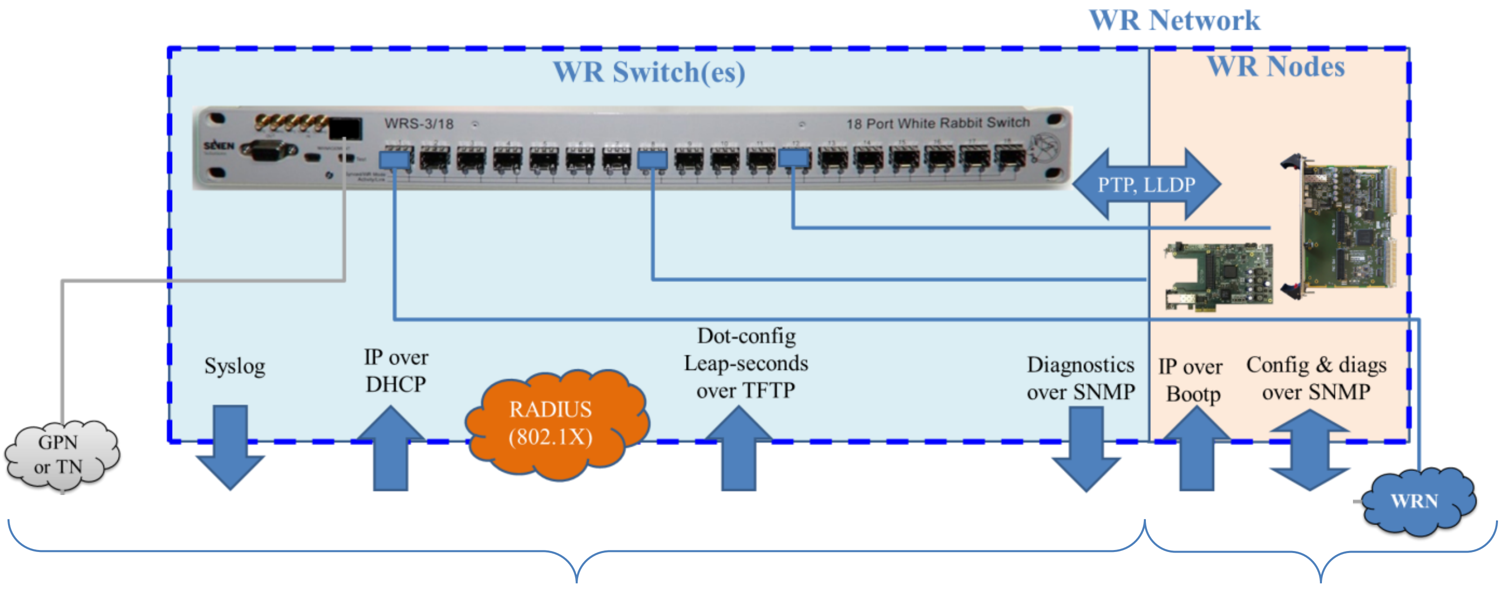
LDPC vs. bitslide

- **Bitslide**
  - Repeatability over reboots <200ps
  - Bit-level misalignment between
    - **Serial word boarder** and
    - **L1 rx clock signal** recovered from the serial bit stream
  - Determined by determining bit position
  - Problem: b1 ≠ b2 ≠ b3 …
  - Bitslide measurements (in ps) inaccurate

- **Low Phase Drift Calibration (LDPC)**
  - Repeatability over reboots <20ps
  - Restart Clock and Data Recovery (CDR) until known bit position
  - Reports bitslide zero (actual value included in relative calibration)



Networking Services



<u>WR Switch services (config/monitoring) over</u>

- Standard Ethernet network (GPN=General Purpose Network or TN=Technical Network)
- Management Port

<u>WR Node services (config/monitoring) over</u>

- WR Network
- WR Port

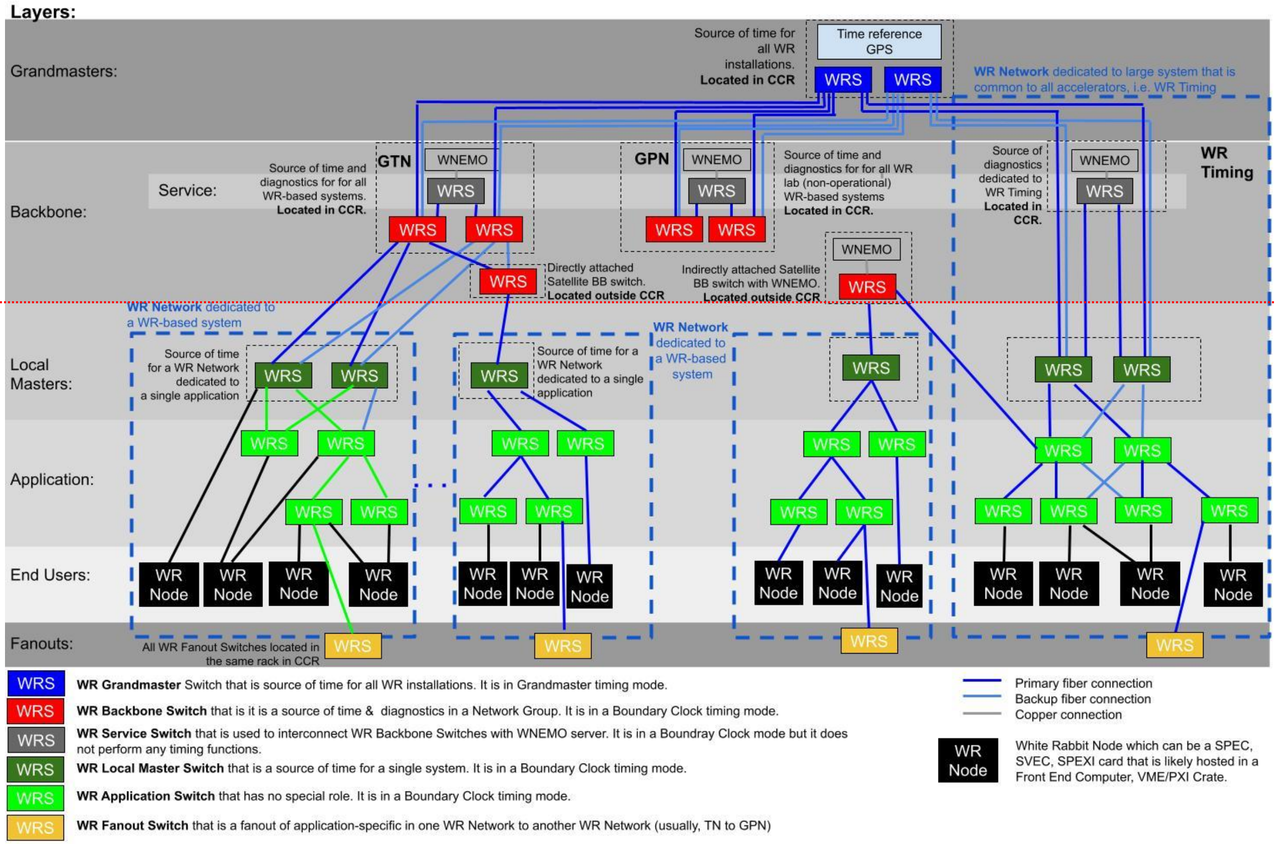
Network architectures

No application data in backbone.
Only diagnostics and time

Time

WR Node Diagnostics

Application Data:
- Contained to one application network
- Exchanged between networks only via dedicated switches



In this presentation you learned

- Basics and components of WR Operation
- PTP, WR-PTP, HA-PTP
- L1 Syntonization and DDMTD
- Types of Devices and WR Switches
- Performance
- Bitslide vs. LPDC
- Networking Services
- Network architecture at CERN