MiniDT readiness (SXA5)

MiniDT @ SND@LHC meeting Nov 26th 2024

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Preparation in LNL (Oct/Nov 2024)

- Luigi+Licia in LNL 29/10 to work with Franco at the 4 "Lemma" miniDTs
- Cosmics were taken (w/ scintillators) using the "MUTOMCA" readout
 - Using per-channel timeboxes to spot & classify problems
- Chamber naming:
 - Lemma1 = Curatolo 2 = MiniDT2
 - Lemma2 = Amapane 5 = MiniDT5
 - Lemma3 = Zanetti 3
 - Lemma4 = Gonella 4
- Grand summary:
 - Reviewed the mapping to understand data vs hardware
 - Reviewed the issues found in data with Franco
 - Opened all 4 chambers and fixed (?) most of the problems
 - Added glue to cover screws where missing (improve tightness)

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Classification of problems (attempt)



-600 -400 -200

200

-800

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Timeboxes Lemma1 = MiniDT2



Timeboxes Lemma2 = MiniDT5



Timeboxes Lemma3



Timeboxes Lemma4

Many "D"s + intermediate cases. Gas not ok?



Summary NB: channels in [0,63]. Details in backup

- Lemma1: ch2 (~1/4 n. hits) missing strip
- Lemma2: ch23 FEB dead; ch42 inefficiency
- **Lemma3**: ch8 (~1/3 n. hits) missing strip; ch44-ch48 (neighbouring cells) missing cathode
- Lemma4: ch12-ch16 (neighbouring cells) missing cathode; ch49 missing wire; ch62 (chamber side) missing cathode
 - Also: bad time box shapes in general in Lemma4. Gas?

Results after repairs at LNL

- Lemma1 = MiniDT2: "perfect"
- Lemma2 = MiniDT5: "perfect"
- **Lemma3**: cathodes fixed; optical inspection of channel8: strip found to have a ridge, probably causes ΔV wire-strip to be lower than nominal (drawing some current...)
- **Lemma4**: after more issues (wire replaced twice, FEB replaced), finally fixed the dead channel. But latest data show we might now have a lateral cathode not connected
- Lemma1 and Lemma2 chosen for SND installation; Lemma3 can be good as a spare; Lemma4 should be made "perfect" with one more opening.

Travel to CERN 18/11-21/11

- We took to CERN:
 - Two chambers, power supplies, FEB slow control (NEW!), HV distribution box, cables etc
 - MiniDTs close to DT chambers in SXA5
 - HV prepared by Lisa from SY4527 in the mobile rack
 - Gas line prepared by Mimmo (independent line, exhaust joining DT exhaust)
 - Trying to read out with OBDT theta in the minicrate, Giulia taking care of handling all related tools
 - Added two scintillators with all needed NIM electronics for a cosmics trigger
 - Added as well a NIM-LVDS adapter equipped with one Yamaichi connector, to inject the scintillator trigger into DT readout through a FE cable

Pictures of MiniDTs @ SXA5

 MiniDTs on the DT table, with scintillators on top (HV side)







Pictures of MiniDTs @ SXA5



We put additional power supplies on the desk close to the DT table, FE side



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• MiniDT

First data taking / MiniDT2

- We expect a cosmic rate of about 5 Hz / channel
- Observed mildly noisy channels in MiniDT2 (max rate ~80 Hz)
 - About 5 channels consistently above 20 Hz
 - Not too bad, just 24 hours after installation

First data taking / MiniDT5

- MiniDT5 much more noisy
- Max rate > 1.5 kHz
 - ~30 channels above 200 Hz
 - Much worse situation than MiniDT2

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Cosmics w/ scintillator / MiniDT2

- Just 5 minutes runs,
 ~10k cosmic triggers
 - Rate of scintillator about right
 - Timeboxes appear and it seems they could be ~fine

Cosmics w/ scintillator / MiniDT5

 Same data for MiniDT5

HV currents (Nov 23rd)

Custom	Name	↔ I0Set	↔ V0Set	IMon	VMon	Pw
01.000	Wires	1.0 uA	0.0 V	0.0 uA	0.0 V	Off
01.001	Strips	150.0 uA	0.0 V	0.0 uA	0.0 V	Off
01.002	miniDT_W	12.0 uA	3600.0 V	0.1 uA	3600.0 V	On
01.003	miniDT_S	20.0 uA	1800.0 V	0.0 uA	1800.5 V	On
01.004	CHANNEL04	10.0 uA	2000.0 V	0.0 uA	0.0 V	Off
01.005	CHANNEL05	10.0 uA	0.0 V	0.0 uA	0.0 V	Off
01.006	CHANNEL06	30.0 uA	0.0 V	0.0 uA	0.0 V	Off
01.007	CHANNEL07	30.0 uA	0.0 V	0.0 uA	0.0 V	Off
01.008	CHANNEL08	30.0 uA	0.0 V	0.0 uA	0.0 V	Off
01.009	CHANNEL09	30.0 uA	0.0 V	0.0 uA	0.0 V	Off
01.010	CHANNEL10	0.0 uA	0.0 V	0.0 uA	0.0 V	Off
01.011	CHANNEL11	6.0 uA	0.0 V	0.0 uA	0.0 V	Off
02.000	Beams	30.00 uA	0.00 V	-0.104 uA	1.50 V	Off
02.001	miniDT_K	10.00 uA	1200.00 V	0.020 uA	1199.95 V	On

Next steps / todos

- Will be at CERN again next week
 - Leonardo working on testing the FEPGs at SXA5
 - Licia and I trying again MiniDT readout and checking noise&c
- Can be at CERN again Dec 16-19
 - Let's see if MiniDTs require further massaging
 - Chances for tests of VCU118 readout?
- Final readout goal: integration with SND DAQ (January?)
 - Add portable VME crate with SND-like TTC system
 - Add one SND Veto plane (scint bars + SiPMs + TOFPET + DAQ board)
 - Run VCU118 on SND TTC and send synch bits to dedicated DAQ board
 - → <u>Demonstrate the two streams stay synchronised!</u>

Backup

Chamber commissioning in LNL

Lemma1

- Bad time box (strip?) in channel 2
 - Wire 1 Layer 3
 - Found strip pin was disconnected
 - Mistake or discharge?
 - Reconnected

Lemma 2

- Channel 23 (Wire 6 Layer 1) DEAD
 - Found dead input in FEB
 - FEB replaced
- Channel 42 (Wire 11 Layer 3) very few hits, but time box-shaped
 - Checked HVC, seemed fine
 - Checked FEB, seemed fine
 - Replaced FEB as an attempt

Lemma 3/1

- Channel 8 (wire 3 layer 4) is inefficient (less than 50% of the hits wrt adjacent cells) and the shape is not good (much signal close to the wire, much less from the drift region)
- It was found the capacitance on the HVC board for this channel was 60% larger than normal
 - Consequence: smaller signals to FEB
- HVC replaced

Lemma 3/2

- Timebox of ch44 (W12L4) and ch48 (W13L4) pointing to bad cathode
- This is a relatively common problem, as cathode pins connect quite loosely to the l-beam
- Franco developed a plastic cap to improve fixing (next slide)

Cathode pin plastic plug

- Right: cut end-plug to show how the cathode contact spring behaves
- Bottom: cathode of W12-13 in layer 4 after the insertion of the additional plastic plug

 Correct position

Incorrect
 position

Correct position, with additional plastic plug

Lemma 4

- Many bad timeboxes, "bad-strip-like" but we attribute this to bad gas when data were taken. To be followed up. Meanwhile, fixed other evident issues:
 - Ch12 and Ch16 (W4L4 and W5L5) bad cathode
 - Ch62, W16L3 (side cell) bad cathode
 - Loose HV pins, added plastic caps
 - Ch59, W15L1: wire HV was disconnected and isolated
 - Measured 60 ohm wire-strip
 - Pulling the wire pin a bit, it was clear the wire was trapped in the strip corner, it was freed. Not sure the wire tension will be ok now. Anyway, HV was reconnected, to be tested...

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Improving gas tightness

- Found 3/4 chambers had no extra glue on the cover frame screws
 - One of the frame designs is not perfect and the O-ring does not fully keep such screws out of the gas volume, thus additional sealing with Araldite was needed
 - Glue was added and left to cure, Franco to take care of closing the chamber before putting them back into data taking

Licia improving gas tightness

Franco fixing cathode pins

Lemma 1 present status

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Lemma2 present status

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Lemma4 present status

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Backup

Mappings and other tools

Mapping

For channel IDs in [0.63] from left to right, as seen from frontend side (this is also MuTomka numbering of readout channels)

C H	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
w	1	1	1	1	2	2	2	2	С	3	3	3	4	4	4	4	5	5	5	5	6	6	6	6	7	7	7	7	8	8	8	8
L	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1

C H	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
w	9	9	9	9	10	10	10	10	11	11	11	11	12	12	12	12	13	13	13	13	14	14	14	14	15	15	15	15	16	16	16	16
L	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1	4	2	3	1

Looking at the chamber FE side, with FE connectors

									_		
L4	W1	L4	W2	2L4	Wa	BL4	•	••	•••		
L3	W1L3			W2	2L3	W3	BL3	•	••	•	
L2	W1	IL2	W	2L2	W	3L2				•••	
L1	W1L1			W	2L1	W	3L1		••		

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HV mapping

How to check FE settings

New FE slow control

- Prepared (last minute...) new box to control the frontend
- Based on BeagleBone Black (thanks Antonio Bergnoli!) + 3.3V-5V level shifter to handle I2C interface to chambers' power board
- It works as a solution for installation on SND (with a better box...):
 - allow remote connection (Ethernet)
 - control the JTAG cable for backend firmware upgrades

