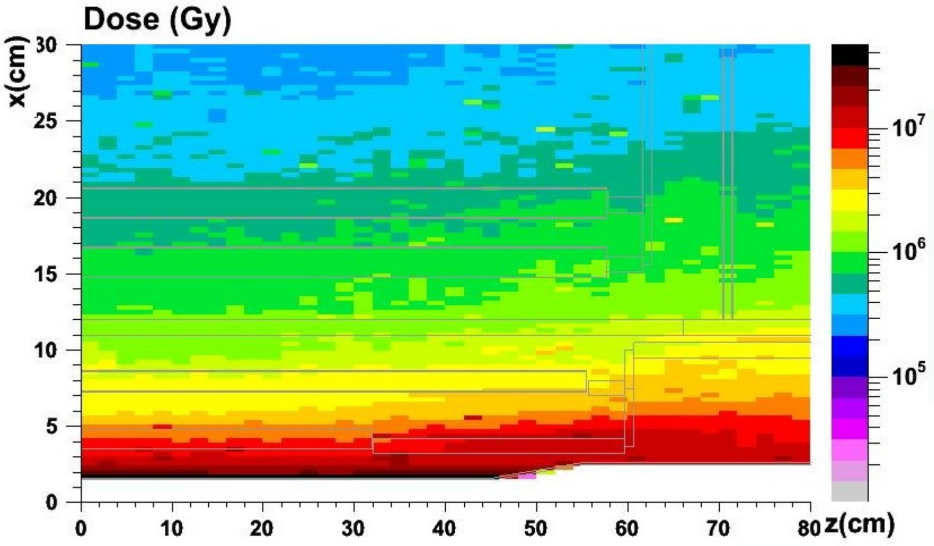
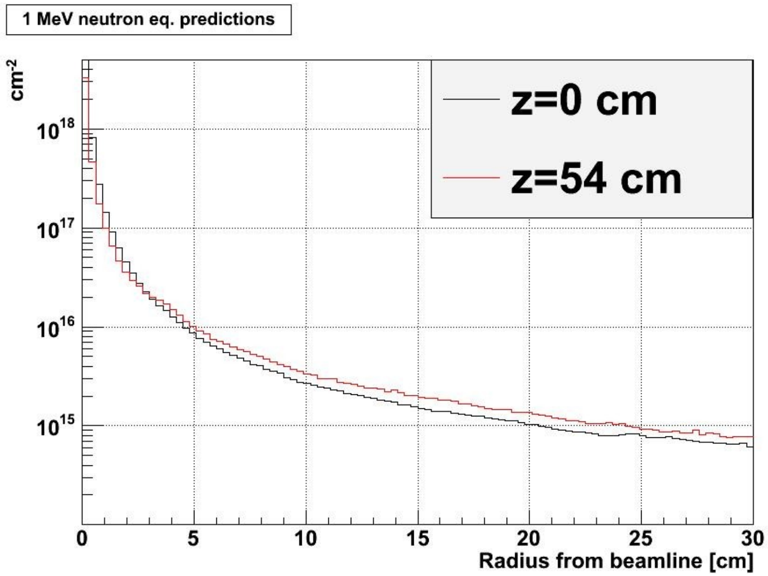
Development of radiation-hard active sensors in 180 nm HV CMOS technology

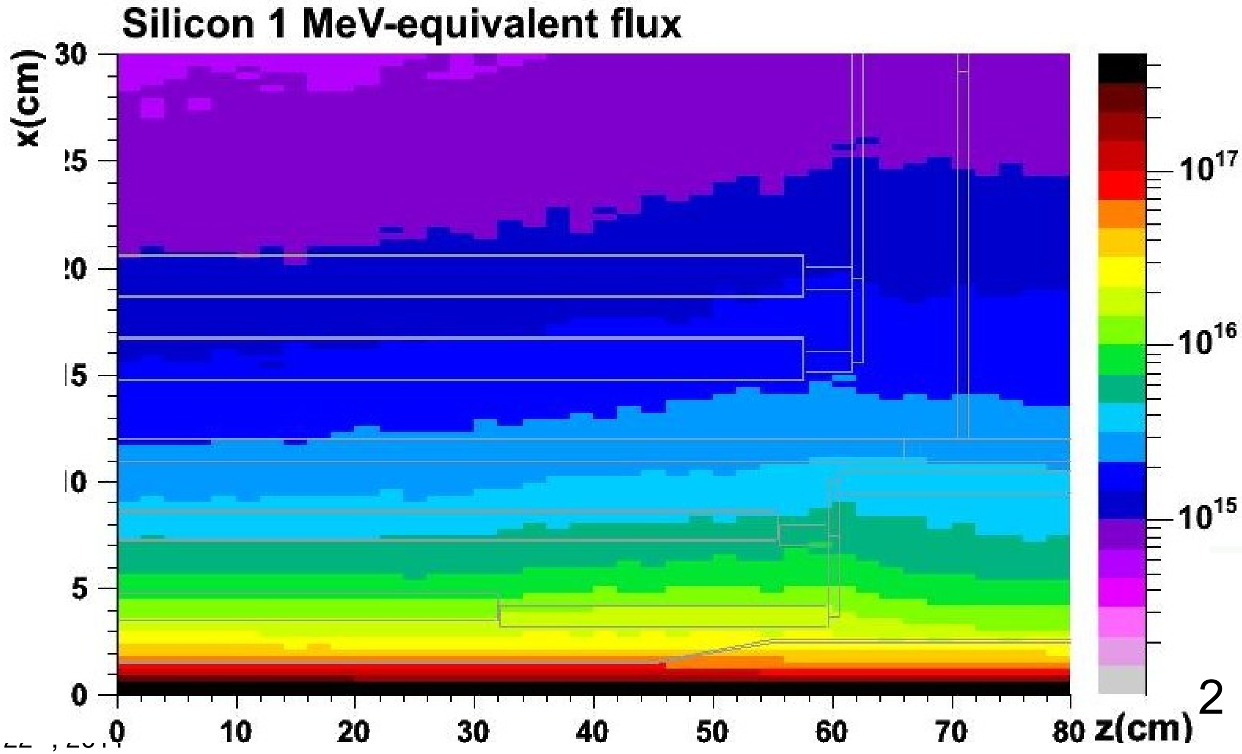
Daniel Muenstermann (CERN)
with most plots stolen from Ivan Peric (U Heidelberg)

Reminder: fluences at HL-LHC

- integrated luminosity: 3000 fb^{-1}
- including a safety factor of 2 to account for all uncertainties this yields for ATLAS:
    - at 5 cm radius:
        - ~$2 \cdot 10^{16}$ n_{eq} cm^{-2}
        - ~1500 MRad
    - at 25 cm radius
        - up to 10^{15} n_{eq} cm^{-2}
        - ~100 MRad
        - several m^2 of silicon







Active sensors

Implications

- High fluences: trapping dominant
  - reduce drift distance, increase field → reduce drift time:
    - 3D sensors
    - thin silicon
    - low depletion depth 'on purpose':
      - low(er) resistivity silicon
      - dedicated annealing to increase N_{eff}
- Large areas: low cost of prime importance
  - industrialised processes
  - large wafer sizes
  - cheap interconnection technologies
- Idea: explore industry standard CMOS processes as sensors
  - commercially available by variety of foundries
    - large volumes, more than one vendor possible
  - 8” to 12” wafers
    - low cost per area: “as cheap as chips”
  - (partially too) low resistivity p-type Cz silicon
    - thin active layer
    - wafer thinning possible

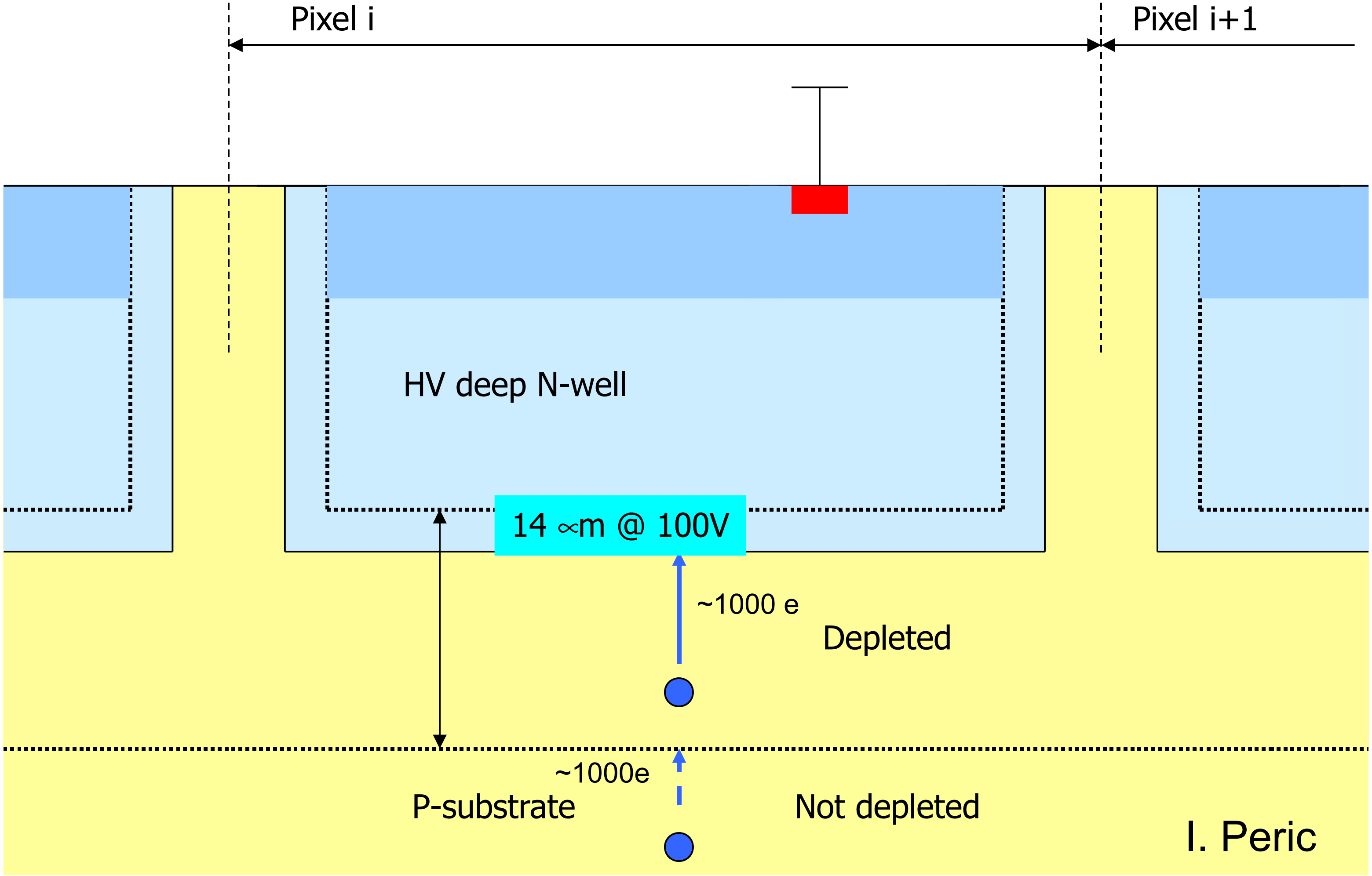
AMS H35 and H18 HV-CMOS

- Project initiated and led by Ivan Peric (U Heidelberg)
- Austria Micro Systems offers HV-CMOS processes with 350 and 180 nm feature size, the latter one in cooperation with IBM
  - biasing of substrate to ~100V possible
  - substrate resistivity ~20 Ohm*cm → $N_{eff} > 10^{14}/cm^3$
    - radiation induced N_{eff} insignificant even for innermost layers
  - depletion depth in the order of 10-20 µm
  - on-sensor amplification possible - and necessary for good S/N
    - key: small pixel sizes → low capacitance → low noise
  - additional circuits possible, e.g. discriminator
    - beware of 'digital' crosstalk
  - full-sized radiation hard drift-based MAPS feasible, but challenging
    - aim for 'active sensors' in conjunction with rad-hard readout electronics first

- Scope of the talk:
  - Introduce the concept
  - Present first results with test chips
  - Outline a planned submission

A HV-CMOS sensor...

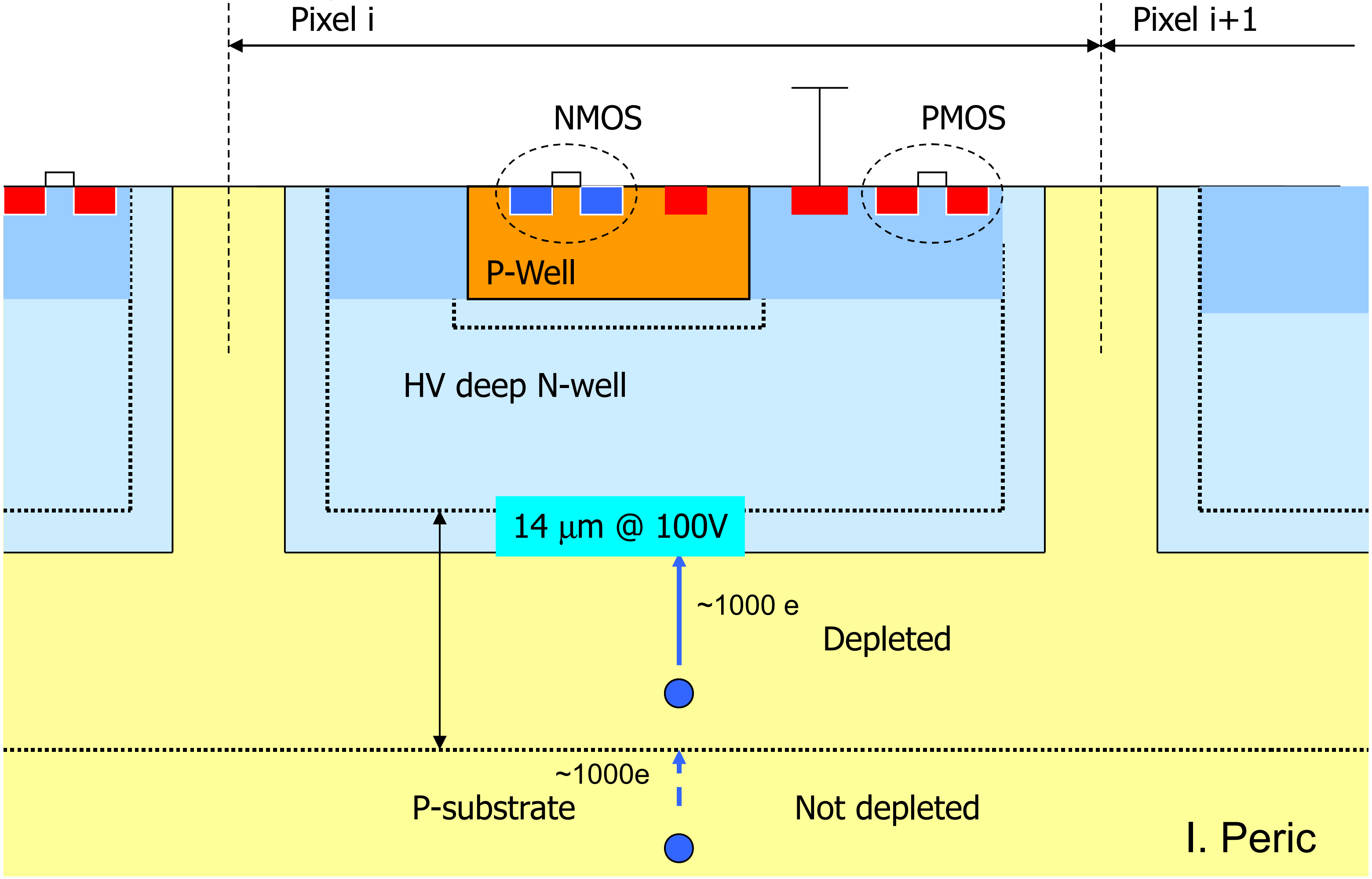
- essentially a standard n-in-p sensor
- depletion zone 10-20 μm: signal in the order of 1-2ke-
  - challenging for hybrid pixel readout electronics
    - new ATLAS ROC FE-I4 might be able to reach this region – but no margin



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

…including active circuits

- implementation of
  - first amplifier stages
  - additional cuircuits: discriminators, impedance converters, logic, …
- deep sub-micron technology intrinsically rad-hard

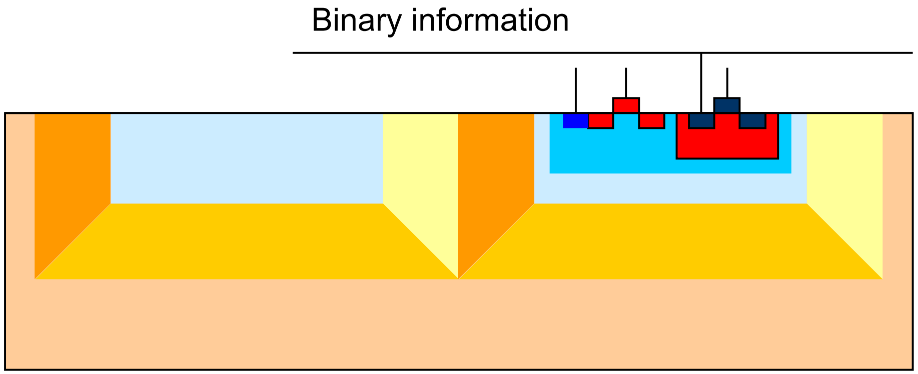


CMOS electronics placed inside the diode (inside the n-well)

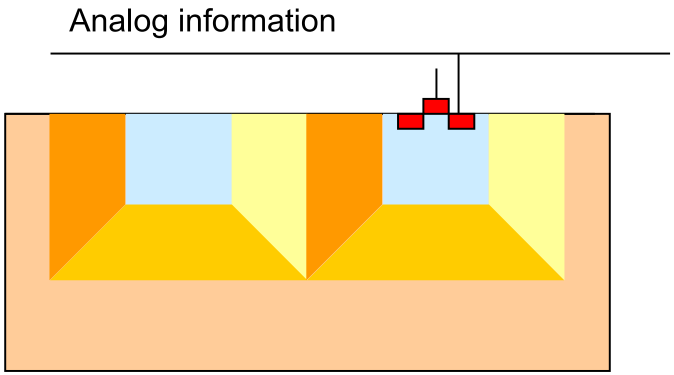
Prototypes

- Several test-chips submitted in both technologies already

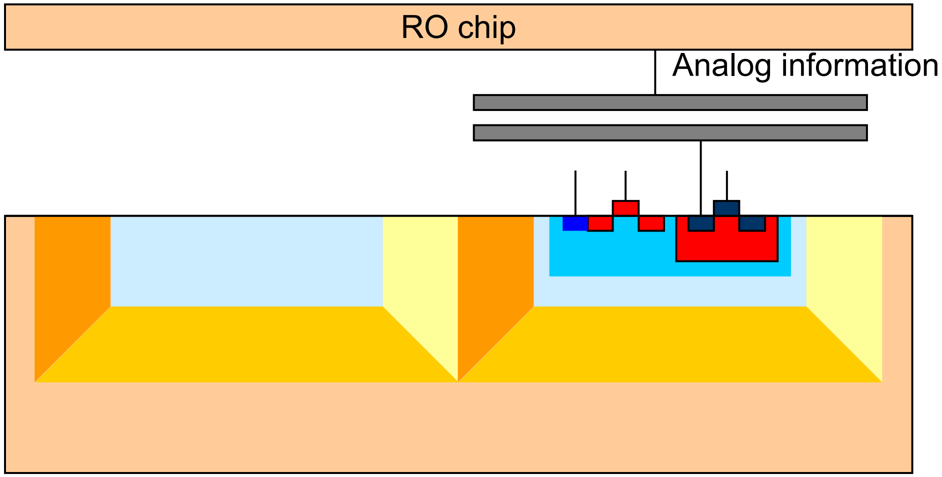
SDA with sparse readout
("intelligent" CMOS pixels)
HV2/MuPixel chip



SDA with frame readout
(simple PMOS pixels)
HVM chip



SDA with capacitive readout
("intelligent" pixels)
Capacitive coupled pixel
detectors
CCPD1 and CCPD2 detectors



Prototype summaries

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55µm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns

Bumpless hybrid detector

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60µm
RO type: capacitive
Noise: 80e
MIP signal 1800e

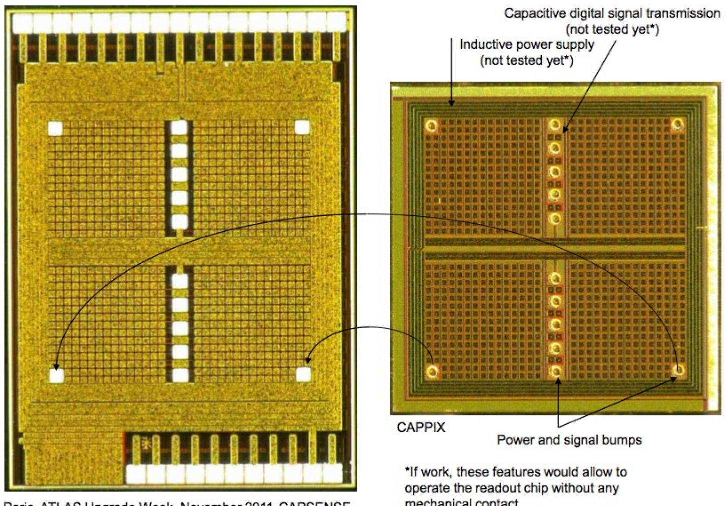
CCPD2 Chip
Edgeless CCPD
Pixel size 50x50µm
Noise: 30-40e
Time resolution 300ns
SNR 45-60

Irradiations of test pixels
60MRad – SNR 22 at 10C (CCPD1)
$10^{15}n_{eq}/cm^2$ – SNR 50 at 10C (CCPD2)

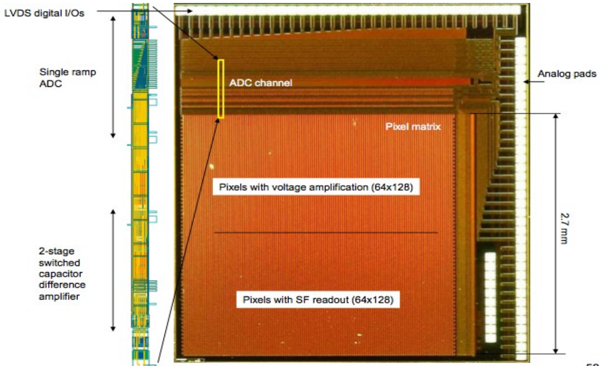
Frame readout - monolithic

PM1 Chip
Pixel size 21x21µm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7µm
Uniform detection

PM2 Chip
Noise: 21e (lab) - 44e (test beam)
Test beam: Detection efficiency 98%
Seed Pixel SNR ~ 27
Cluster Signal/Seed Pixel Noise ~ 47
Spatial resolution ~ 3.8 ∝m

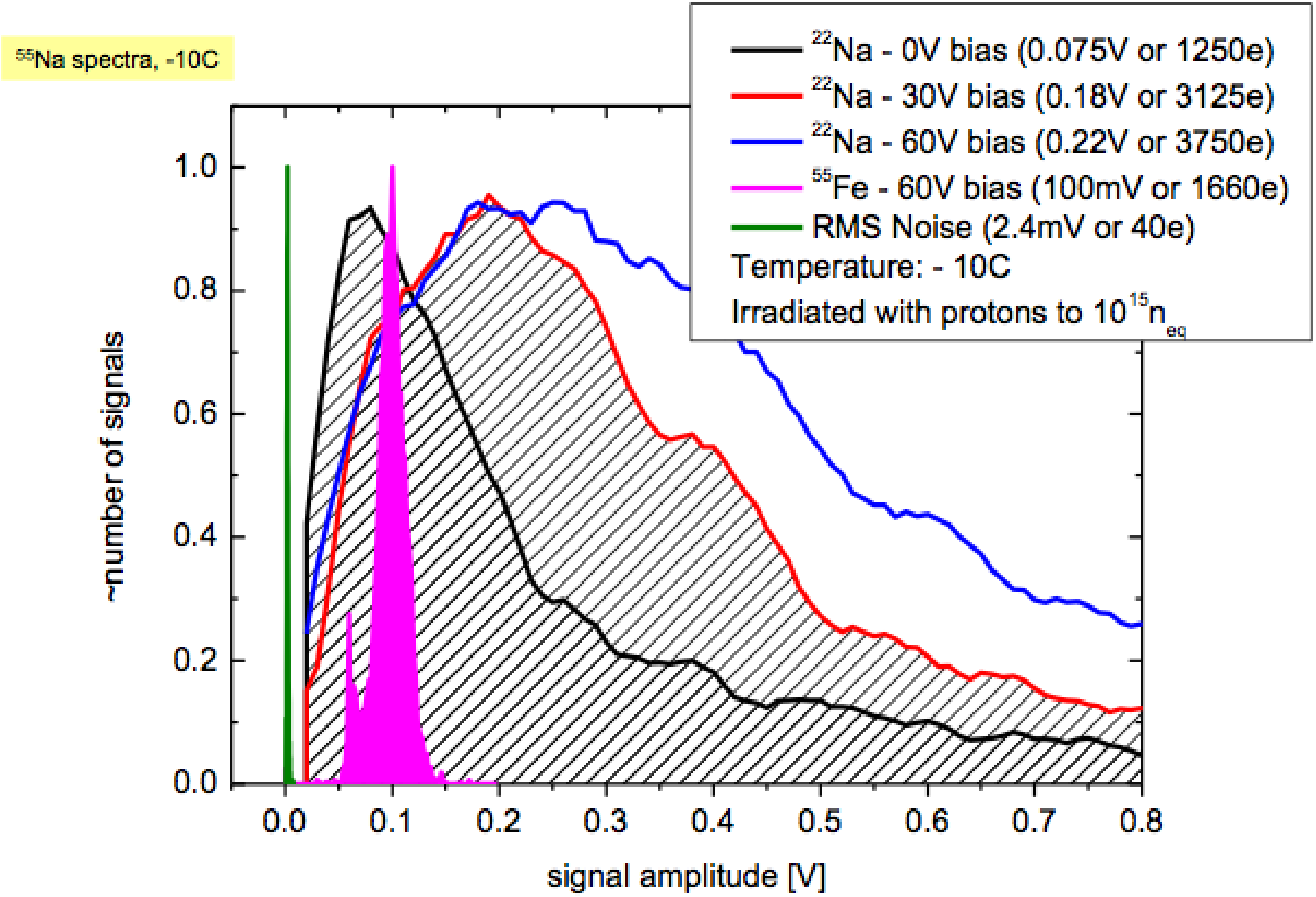


*If work, these features would allow to operate the readout chip without any mechanical contact



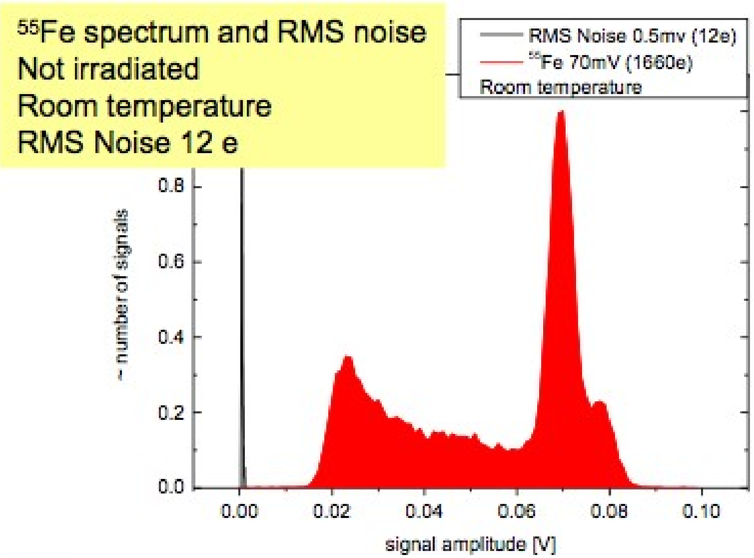
Some irradiated prototype results

- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- generally very good S/N ratio

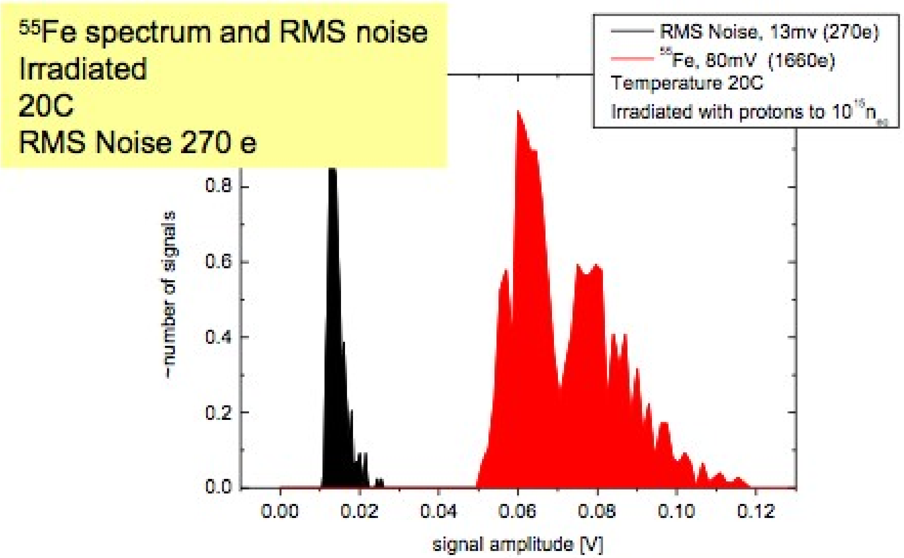


Some irradiated prototype results

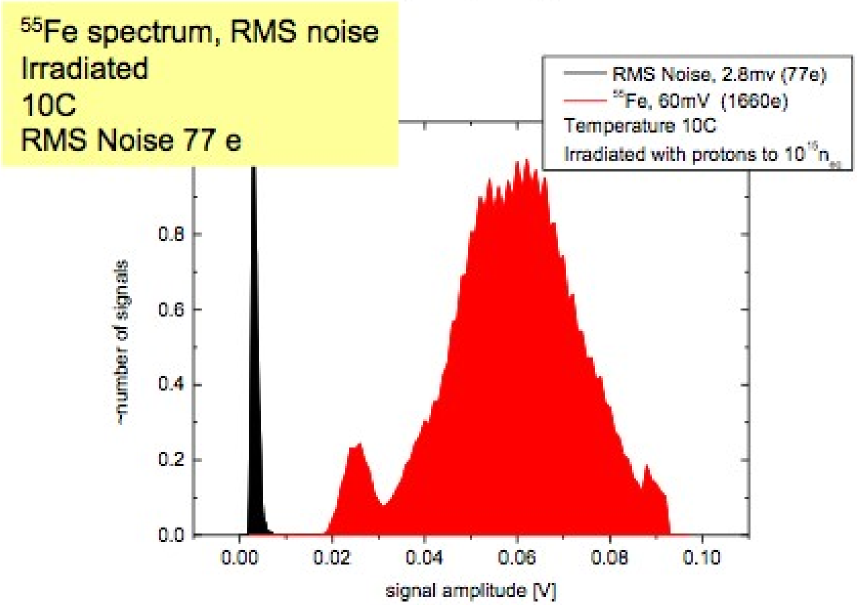
- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- FE-55 performance recovers after slight cooling



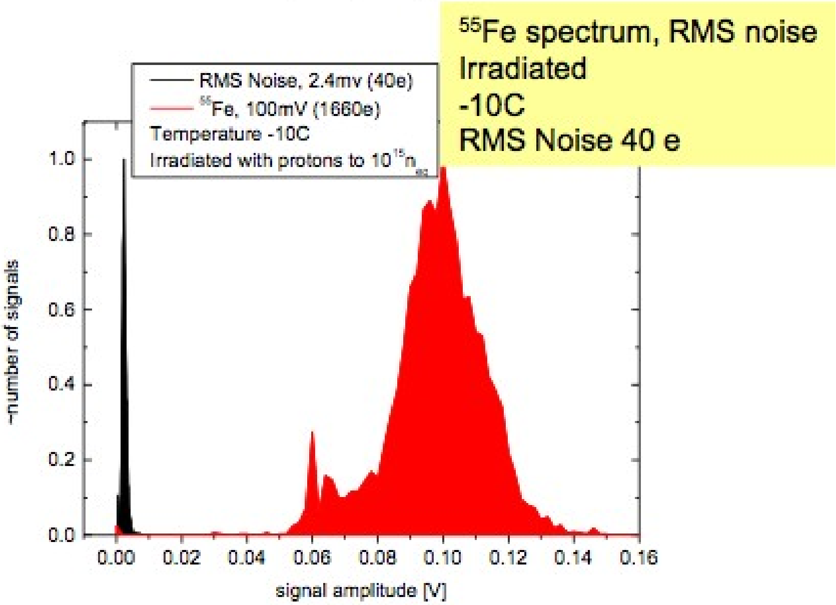
^{55}Fe spectrum and RMS noise
Not irradiated
Room temperature
RMS Noise 12 e



^{55}Fe spectrum and RMS noise
Irradiated
20C
RMS Noise 270 e



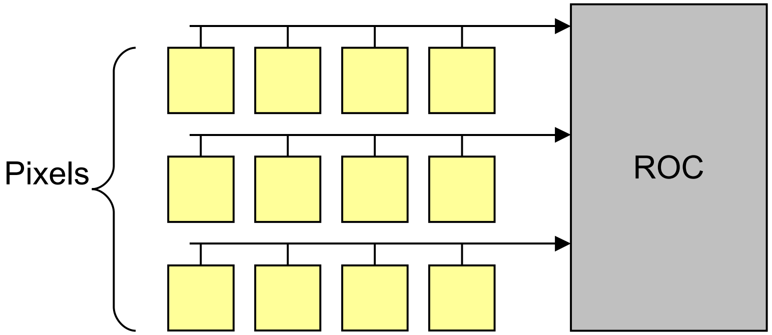
^{55}Fe spectrum, RMS noise
Irradiated
10C
RMS Noise 77 e



^{55}Fe spectrum, RMS noise
Irradiated
-10C
RMS Noise 40 e

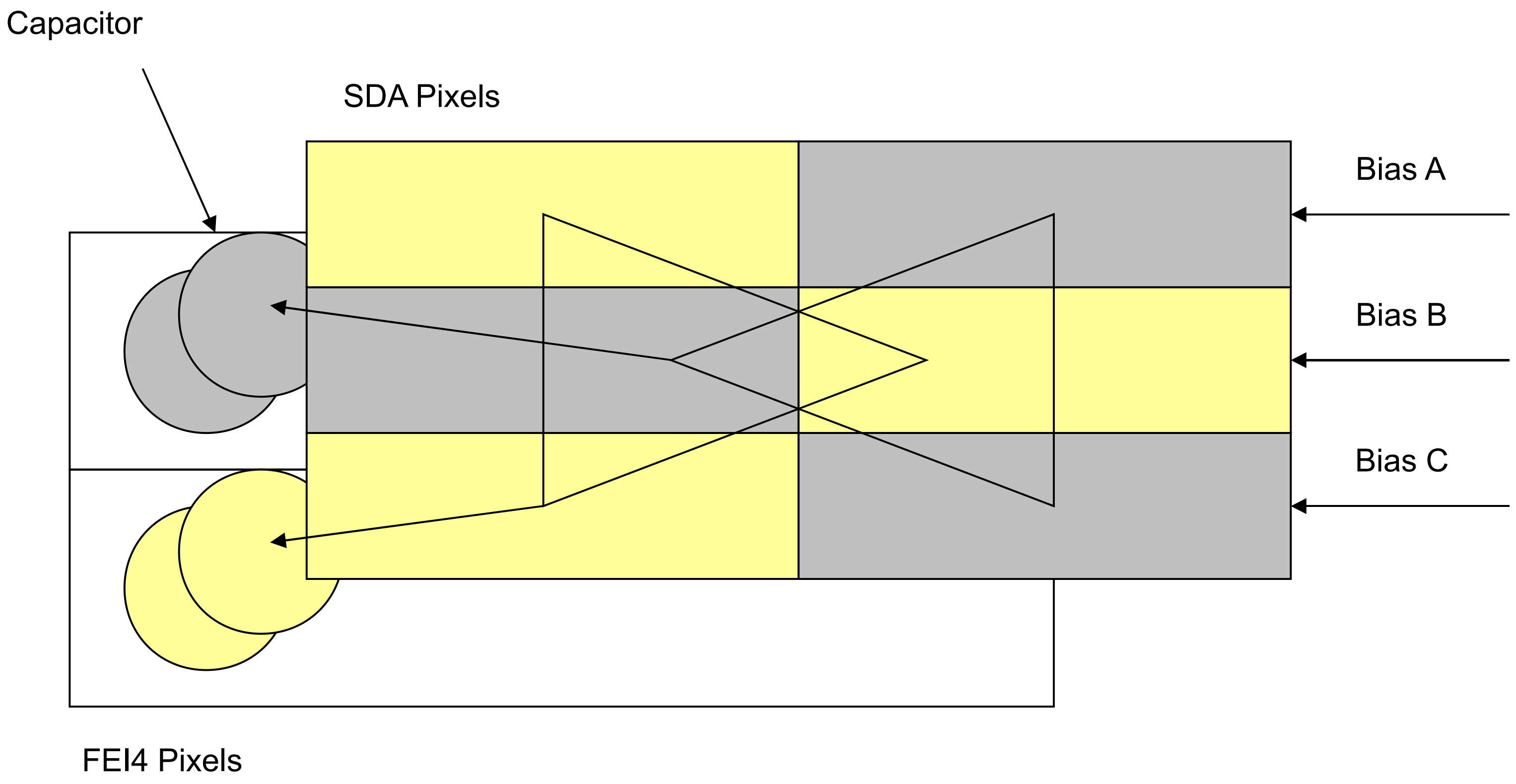
From MAPS to active sensors

- Existing prototypes would not suitable for HL-LHC, mainly because
  - readout too slow
  - time resolution not compatible with 40 MHz operation
  - high-speed digital circuits would affect noise performance
- Idea: use HV-CMOS as sensor in combination with existing readout technology
  - fully transparent, can be easily compared to other sensors
  - can be combined with several readout chips
  - makes use of highly optimised readout circuits
  - can be seen as first step towards a sensor being integrated into a 3D-stacked readout chip (not only analogue circuits but also charge collection)
- Basic building blocks: *small* pixels (low capacitance, low noise)
  - can be connected in any conceivable way to match existing readout granularity, e.g.
    - (larger) pixels
    - strips



Pixels

- Possible/sensible pixel sizes: 20x20 to 50x125 µm
  - 50x250 µm (current ATLAS FE-I4 chip) too large
  - combine several sensor “sub-pixels” to one ROC-pixel
    - sub-Pixels can encode their address/position into the signal e.g. as pulse-height-information instead of signal proportional to collected charge
    - routing on chip is well possible, also non-neighbour sub-pixels could be combined and more than one combination is possible



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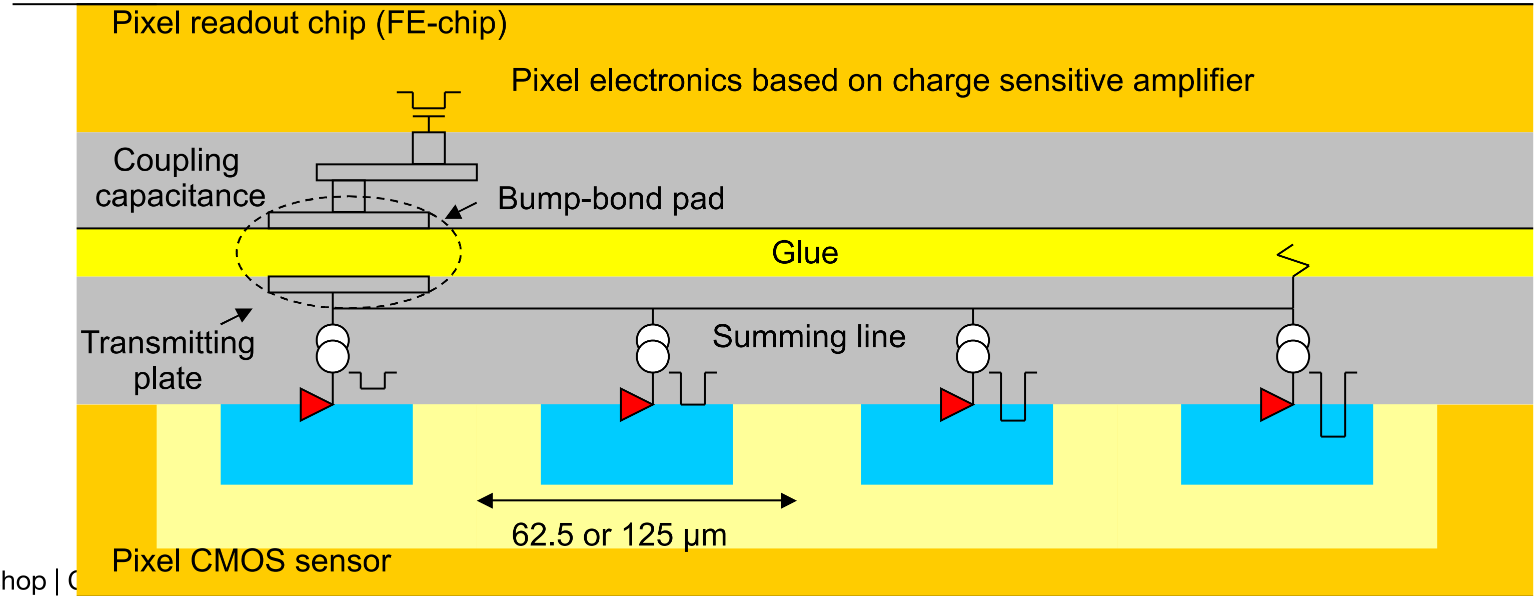
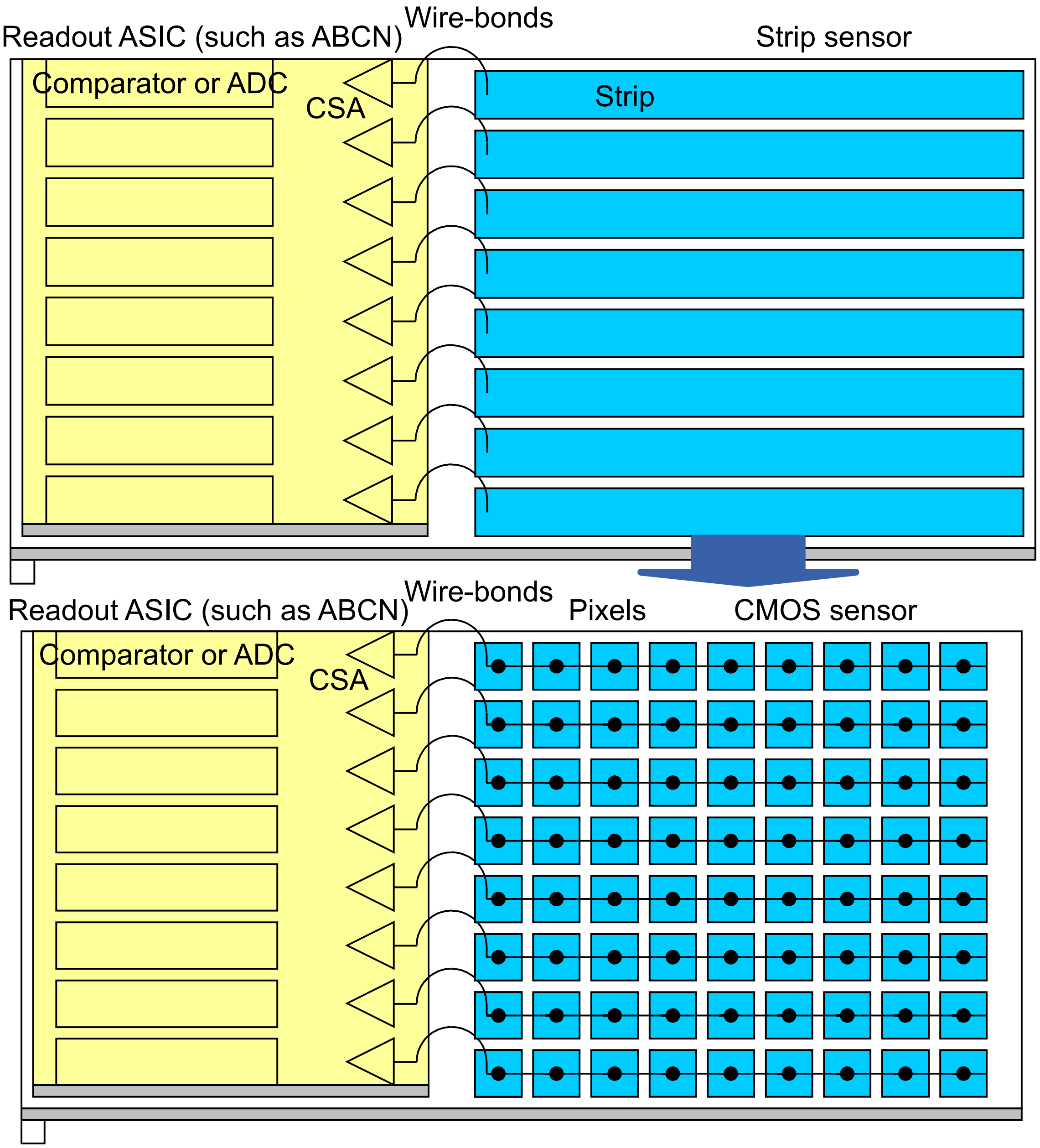
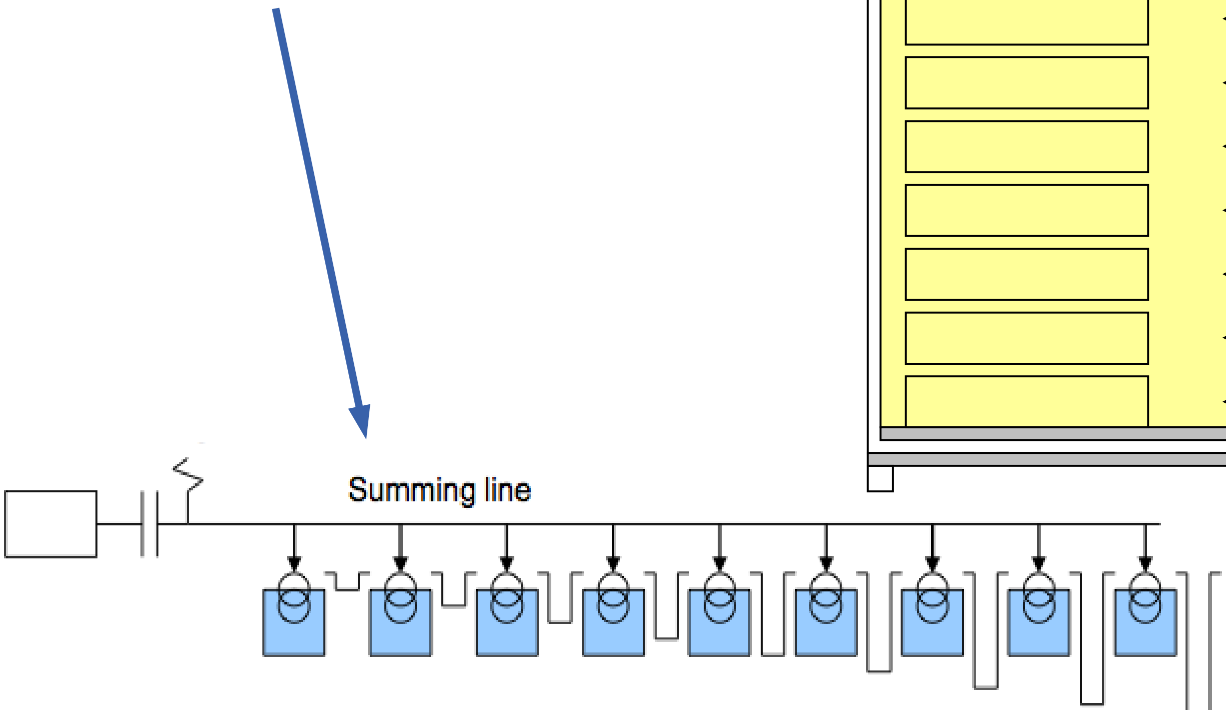
- Only reason not to use AC coupling with pixel sensors up to now was small coupling capacitance in association with low signal
  - amplification possible, hence AC transmission not a problem at all
  - would allow to get rid of costly bump-bonding



Strips

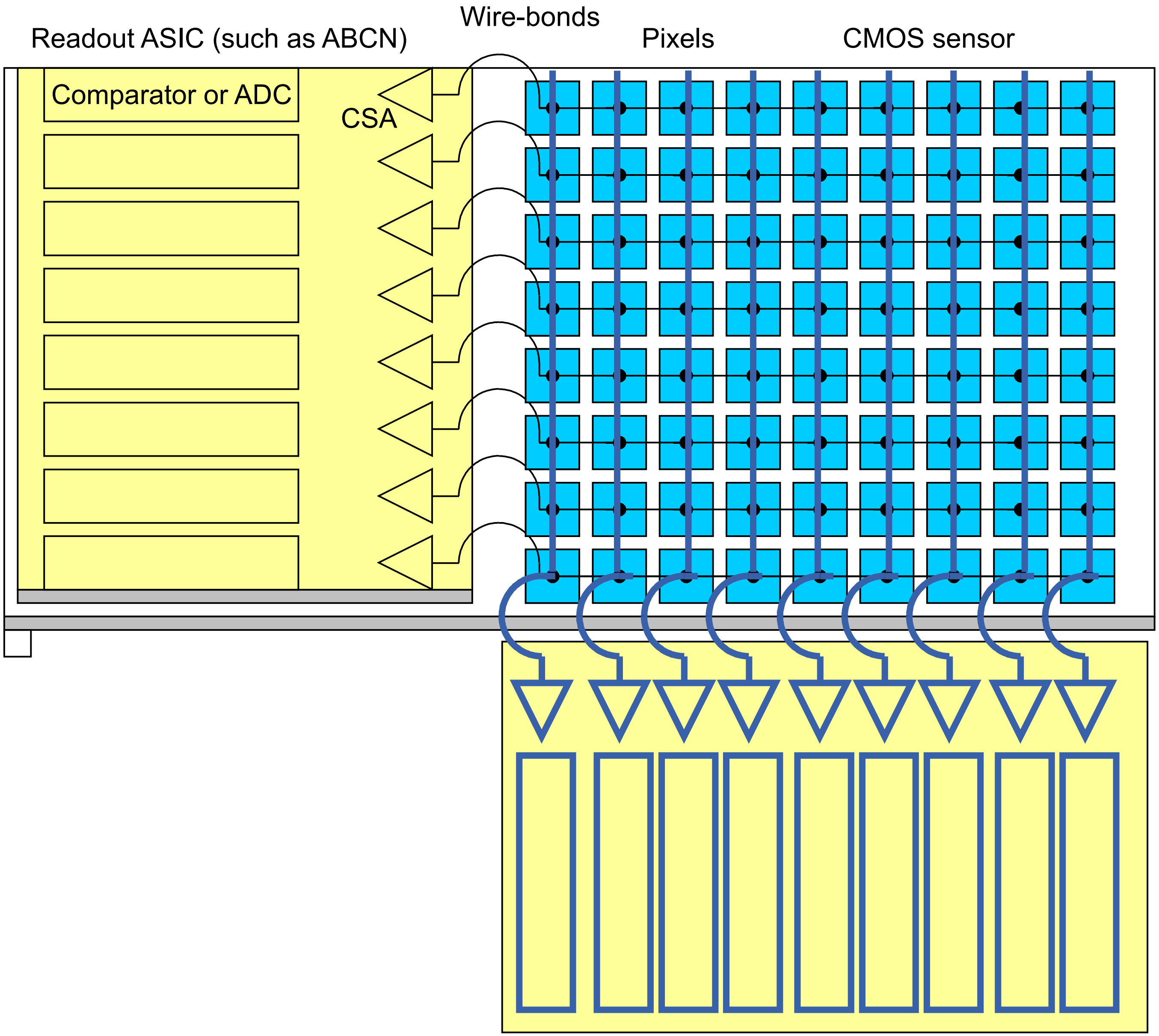
- Easiest idea would be to simply sum all pixels within a virtual strip
- Hit position along the strip could be again encoded by pulse height for analogue readout chips (e.g. Beetle)





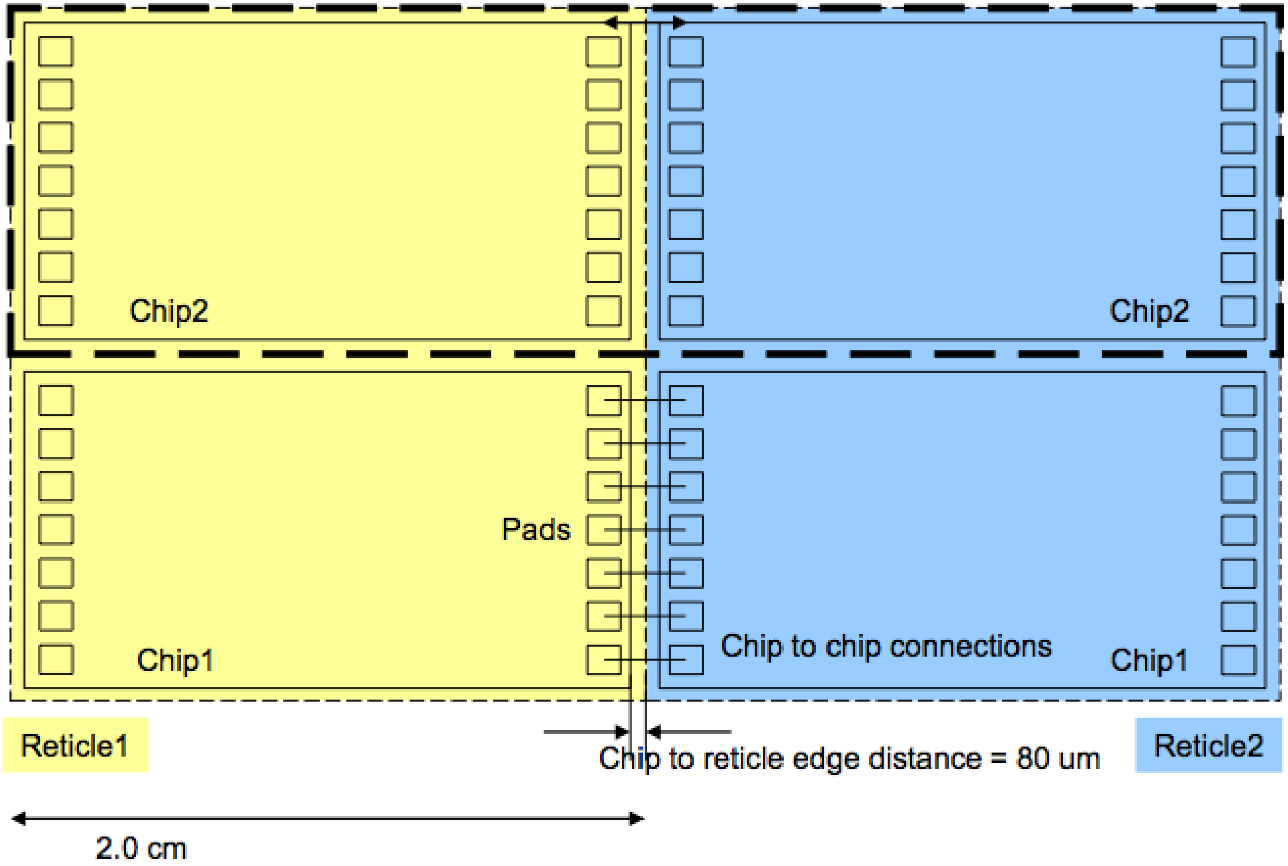
Strips

- Signals are digital so multiple connections are possible, e.g.
  - “crossed strips”
  - strips with double width but only half the pitch in r-phi



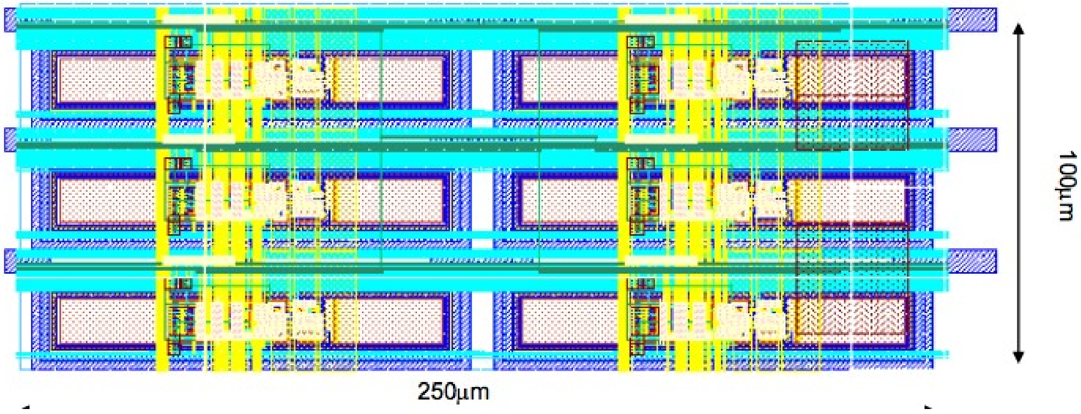
Reticule size/stitching

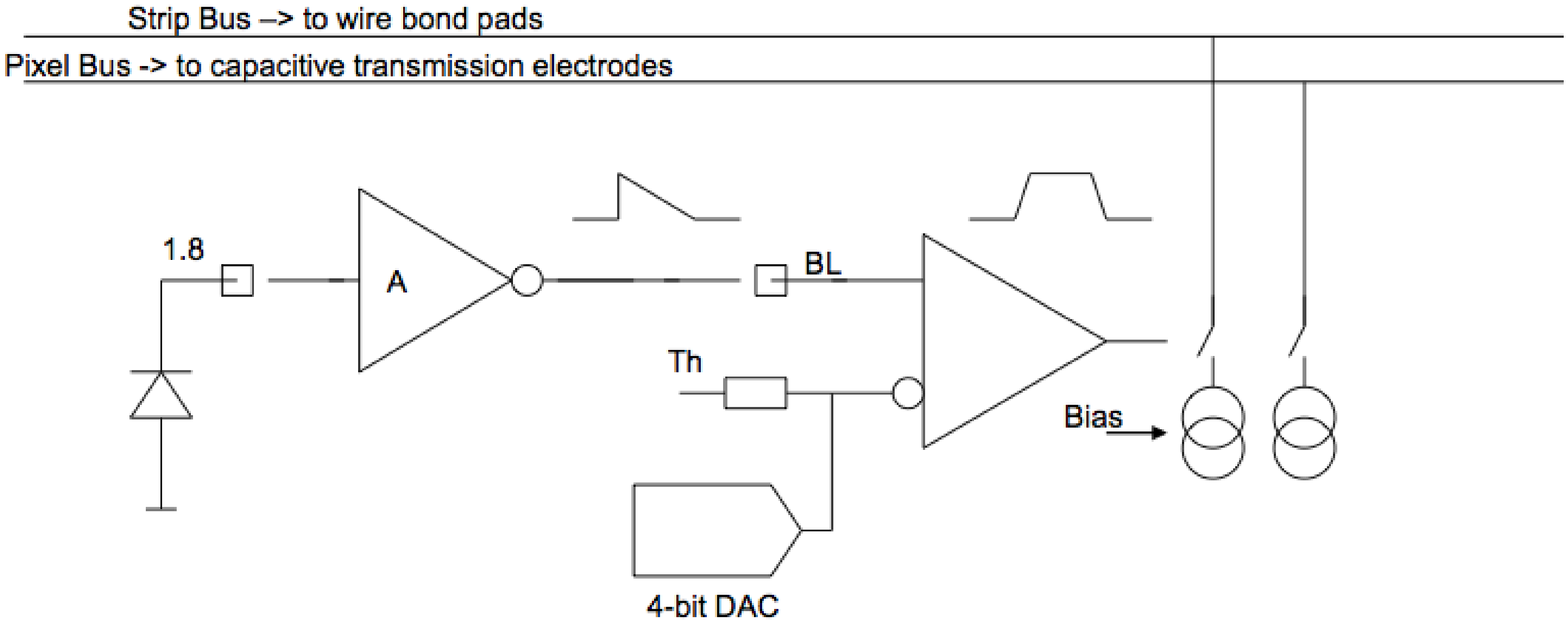
- Sensor size is currently limited by reticule size of ~2x2 cm
  - however, the yield should be excellent (very simple circuit, essentially no “central” parts) so it might be interesting to cut large arrays of sensors from a wafer and connect individual reticules by
    - wire-bonding
    - post-processing (one metal layer, large feature size)
- There are HV-CMOS processes/foundries which allow for stitching
- Very slim dicing streets
  - Gaps between 1-chip modules could be rather narrow



Current plans

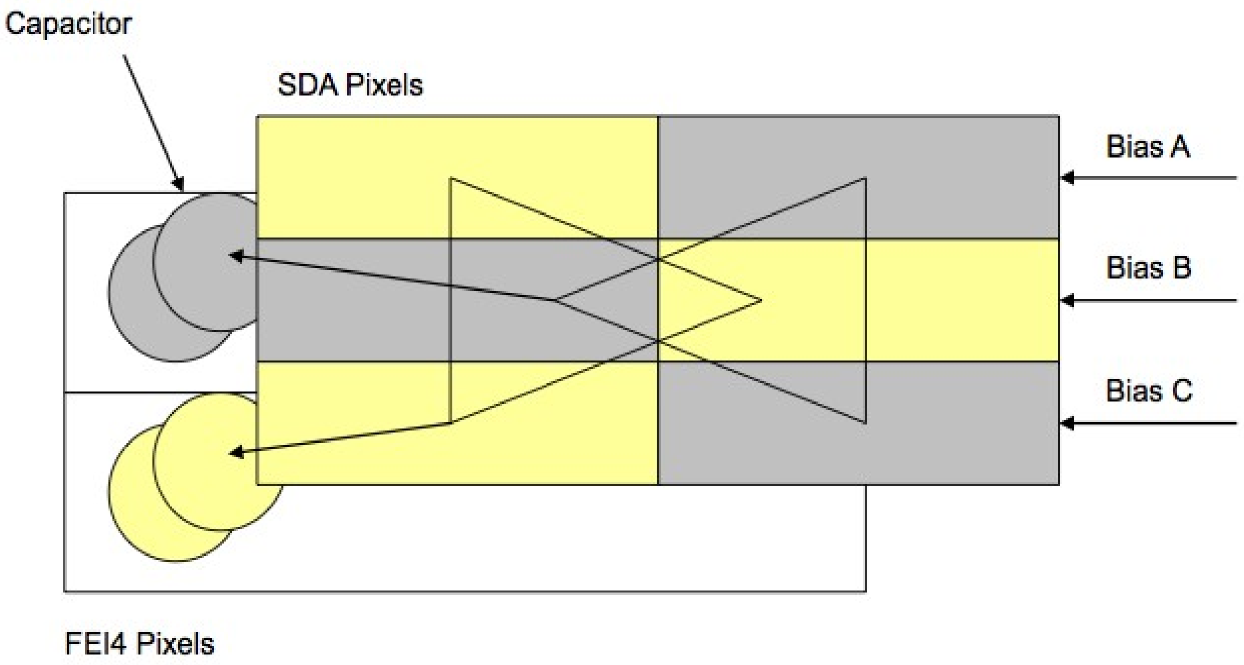
- ATLAS institutes plan to submit a combined active strip/pixel sensor
  - pixels match new ATLAS FE-I4 readout chip
    - capacitive coupling
    - bump-bonding possible
  - strips should be compatible with ATLAS ABCN and LHCb/Alibava Beetle
  - size: ~2x4mm

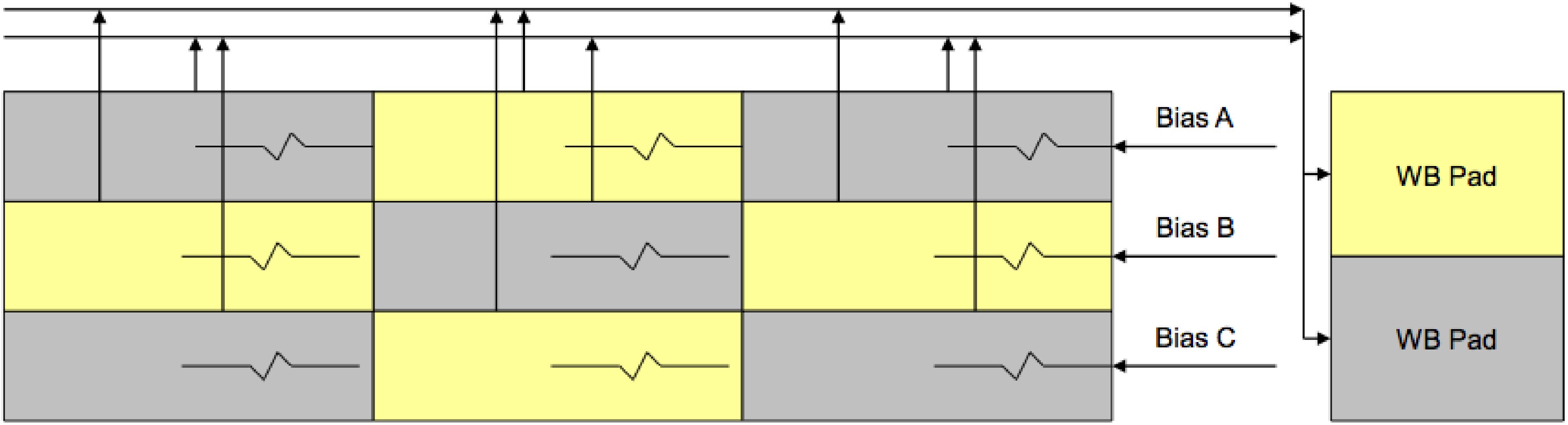




Current plans

- Sub-pixel positions are encoded by 3-level pulses
  - additive: unique pulse heights for all pixel combinations
  - FE-I4's 4-bit ToT should be able to disentangle





Conclusions

- HV-CMOS processes might yield radiation-hard, low-cost, improved-resolution, low-bias-voltage sensors
- First test chips indicate rad-hardness up to at least 1e15 neq/cm2
- Process can be used for
  - drift-based MAPS chips (baseline for µ3e-Experiment at PSI)
  - 'active' n-in-p sensors
- First design being submitted within ATLAS framework suited for
  - capacitively coupled pixel sensors
  - “virtual” strip sensors
- Irradiation and testbeam campaign planned for 2012
  - up to HL-LHC fluences
  - testbeam at CERN with Timepix telescope
- Hope to have raised interest in the community, will report on first “sensor” results at the next RD50 meeting
  - if successful, might be sensible to also pursue an RD50-centric project to be able to include interest from all LHC experiments (and beyond)