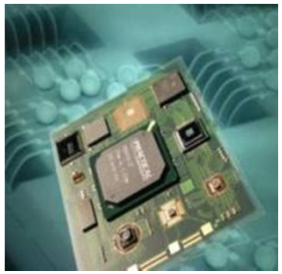
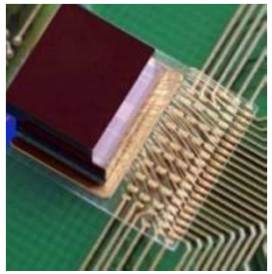




Wafer Level Packaging and Flip Chip Assembly for Hybrid Module Manufacturing

Fraunhofer Institute for Reliability and Microintegration
Gustav-Meyer-Allee 25
13355 Berlin
Germany

Dipl.-Ing. Thomas Fritzsch
Contact: thomas.fritzsch@izm.fraunhofer.de

"Workshop on Quality Issues in Current and Future Silicon Detectors"
CERN, 3-4 November 2011

Fraunhofer IZM

Outline

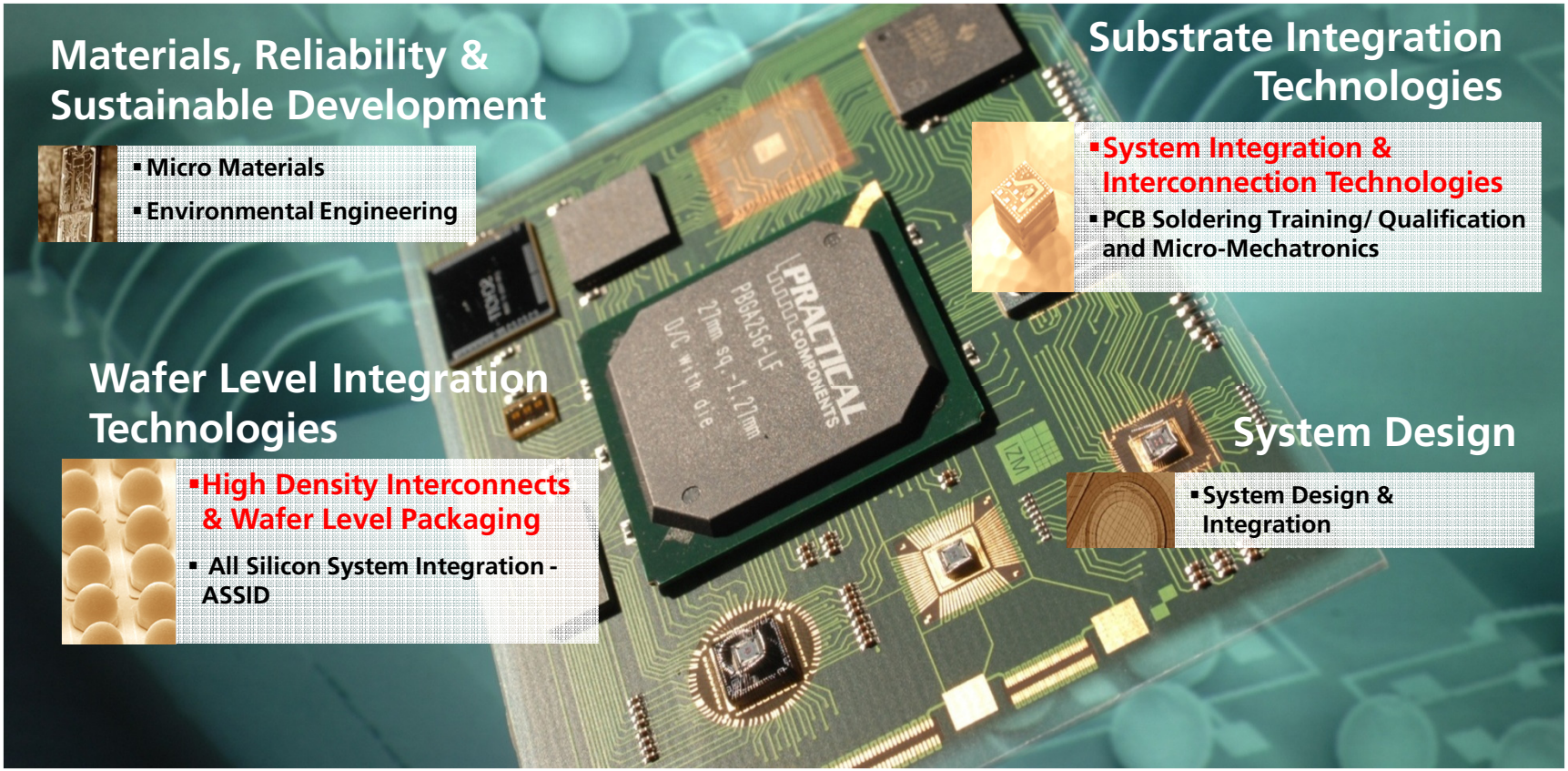
Wafer Level Packaging and Flip Chip Assembly for Hybrid Module Manufacturing

- Wafer Level Packaging Equipment
- Processes on Wafer Level
- Flip Chip Assembly
- Additional technologies for future detector modules:
  - Single chip processing for prototypes
  - Thinned readout chip – flip chip assembly

thomas.fritzsch@izm.fraunhofer.de

Fraunhofer IZM – Focus of Activities

Hybrid Module Manufacturing – Involved Departments

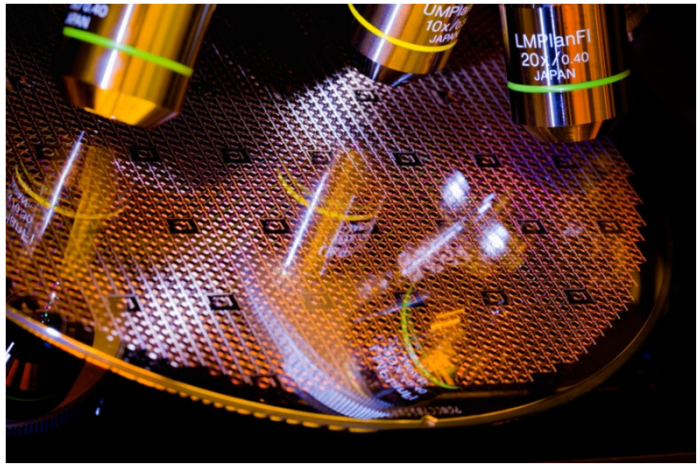


- Material characterisation
- Process evaluation
- Reliability testing
- Failure analysis
- Sample production
- Training courses

thomas.fritzsch@izm.fraunhofer.de

Wafer Level Packaging Technologies

- Layer Deposition
  - Sputtering, Evaporation
  - Electroplating
- Photostructuring
  - Resist
  - Polymeric Dielectrics
- Dry and Wet Etching
- Chemical Mechanical Polishing
- Grinding, Saw Dicing
- Thin Wafer Handling, Wafer Bonding
- Characterisation, Measurement, Inspection



Cleanroom facility 800 sqm

thomas.fritzsch@izm.fraunhofer.de

Process Capabilities from 100mm to 200mm and 300mm

Sputtering
UNAXIS – TiW, Au, Cu, Ti, Cr, CrNi,
Al, AlSi

Lithography
Suess Microtech MA45, MA6, MA200, MA300
EVG IQ Mask Aligner, EVG spin- and spray coating tools
ACS 200 (ACS300)

Electroplating
SEMITOOL, RENA, Rammgraber
Cu, Au, Ni, Sn, SnPb, SnAg, In

Waferbonding
EVG Gemini (oxide, glue, solder, metal)

Dry Etching
MATRIX, STS Silicon Etch, STS Oxid Etch

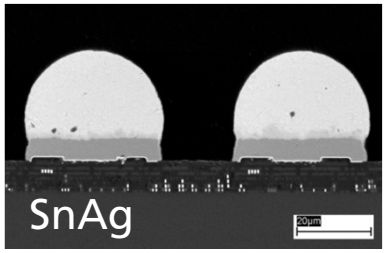
Oxide Deposition
Thermal Oxide (4“, 6“), PECVD Oxide (6“, 8“)

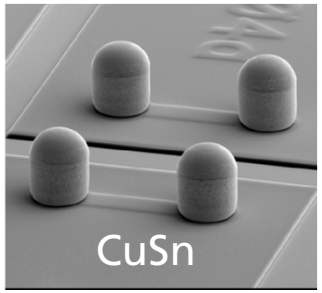
Thinning and Saw Dicing
Disco grinding tool, saw dicing for glass and silicon

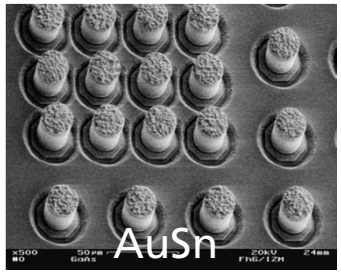
Goal: Stable process parameters using industry standard process equipment

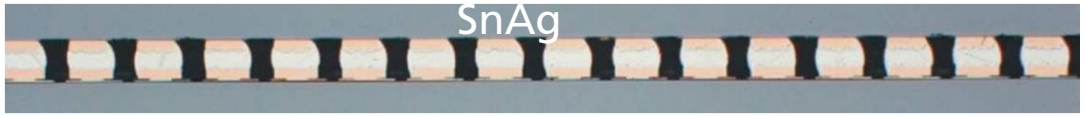
thomas.fritzsch@izm.fraunhofer.de

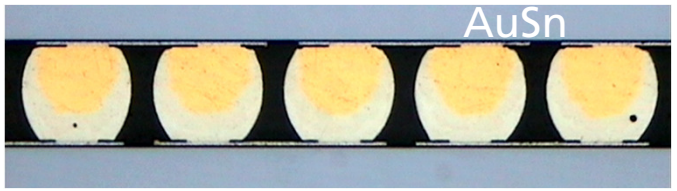
System Integration & Interconnection Technologies - Flip Chip Assembly

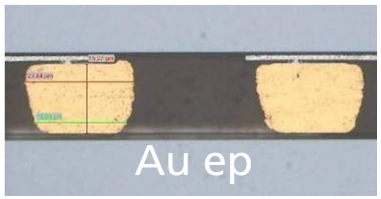


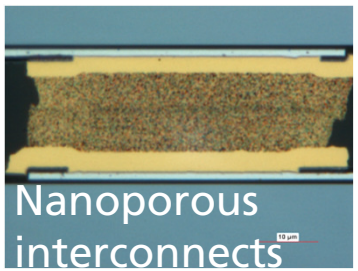


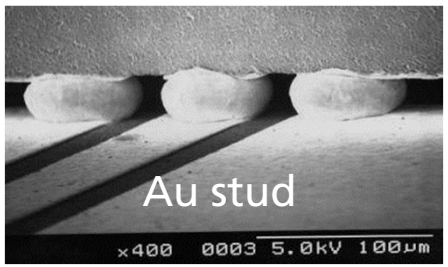












- **Flip Chip**
  - Sn, SnAg(Cu), CuSn
  - Au/Sn fluxless
  - Gold
  - Indium
- **Thermode Bonding**
  - Thermocompression
  - Thermosonic
- **Reflow soldering**
- **Flip Chip Assembly Tools**
  - Suess FC150
  - Panasonic FCB3
  - Datacon
- **Substrates**
  - Chip to Chip
  - Chip To Wafer
  - Wafer to Wafer

thomas.fritzsch@izm.fraunhofer.de

Flip Chip Assembly

Karl Suss FC150

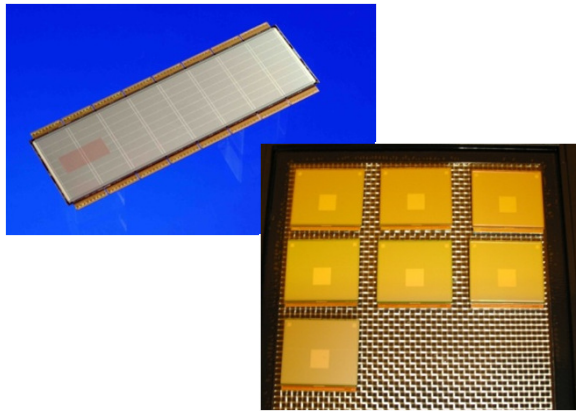
- Accuracy: ± 1 µm at 3σ
- cycle time: ~2 min. per die
- maximum die size: 2” x 2”
- maximum substrate size: 6” x 6”
- heating profiles from top and bottom
- minimum alignment mark size: 20 µm

Panasonic FCB3

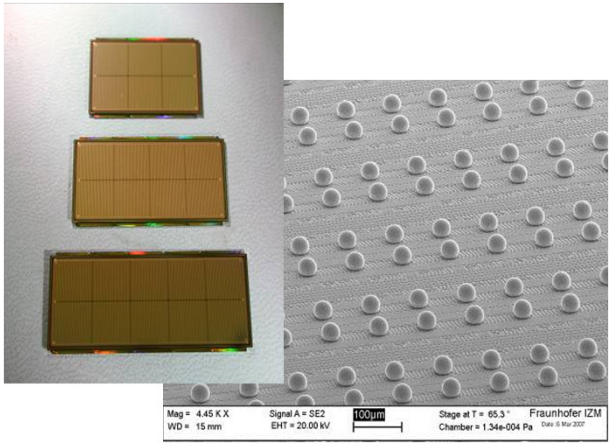
- accuracy: 3.5 µm at 3σ
- full automatic FC bonder with feeder unit
- pick & place cycle time: <2 s
- maximum substrate size: 300 mm wafer
- TC and TS bonding head

thomas.fritzsch@izm.fraunhofer.de

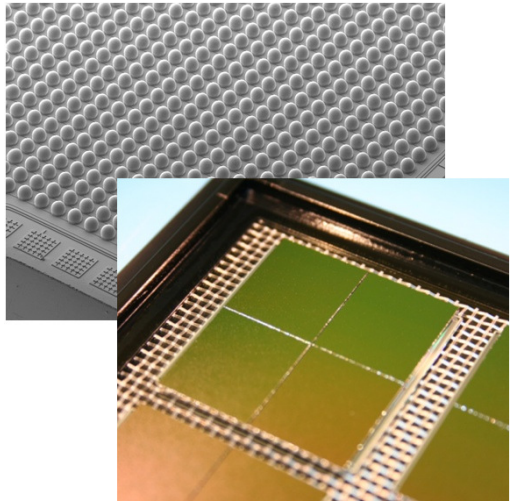
Hybrid Pixel Detector Projects at Fraunhofer IZM



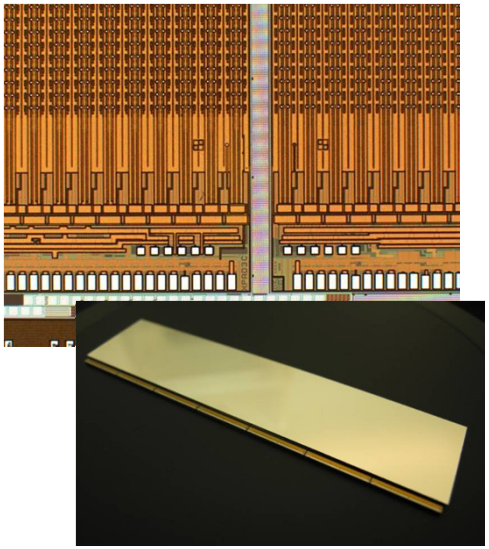
ATLAS FE-I3/FE-I4 Pixel Modules



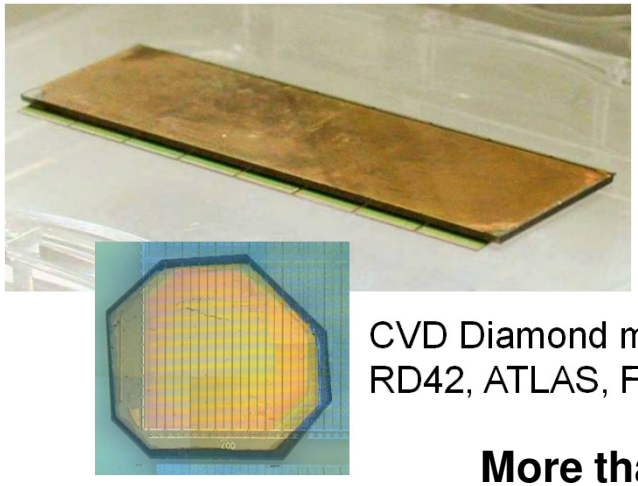
CMSFPIX – Pixel Detector



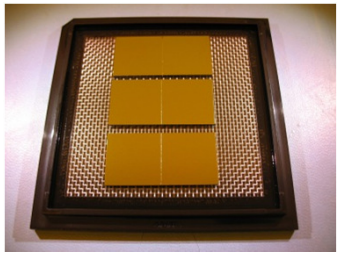
MEDIPIX/TIMEPIX
X-Ray Detector



XPAD3 for CNRS



CVD Diamond modules
RD42, ATLAS, FERMILAB



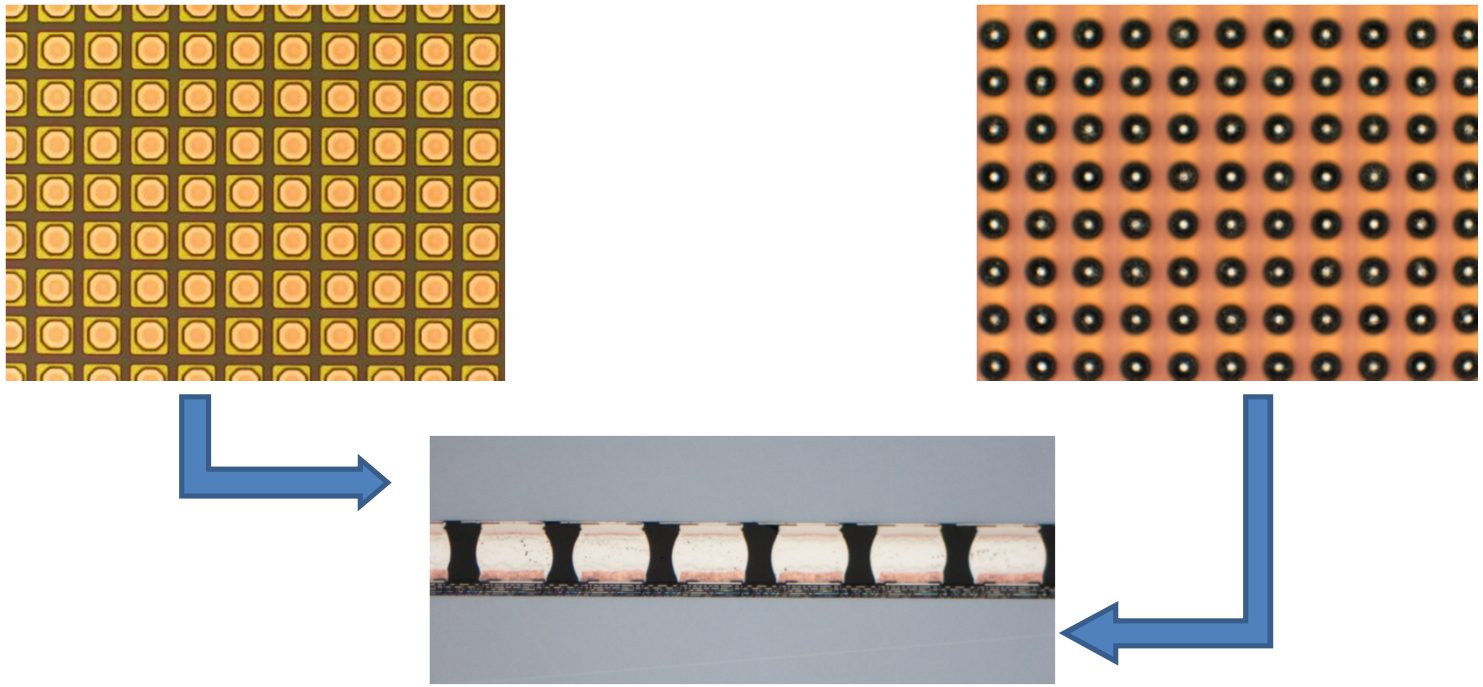
SLAC Stanford

More than 10 years experience in pixel detector hybridization

thomas.fritzsch@izm.fraunhofer.de

Hybrid Module Manufacturing – Wafer Level Technologies

- Step 1: Sensor wafer processing
- Step 2: FE Readout wafer bumping
- Step 3: Flip Chip Assembly

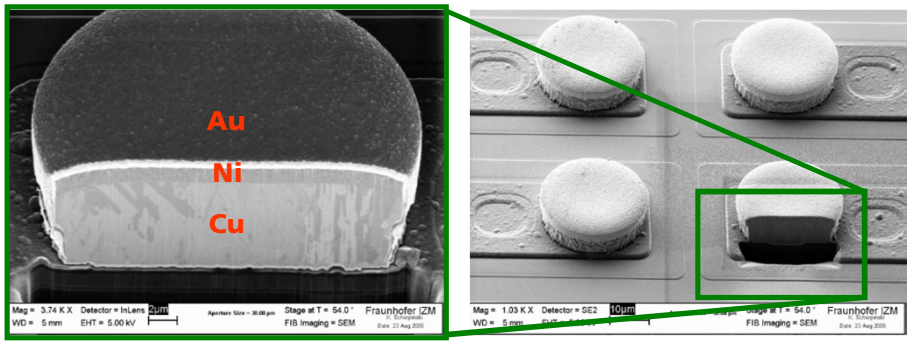


thomas.fritzsch@izm.fraunhofer.de

Wafer Level Packaging for Hybrid Pixel Detectors

Deposition of solderable pixel pads on sensor wafer

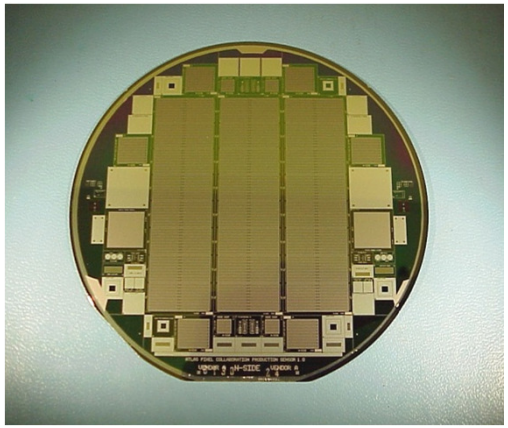
Bump metal	Pad metallization
SnPb37	Cu-Ni-Au
SnAg3.5	Cu, Ni-Cu, Ni-Au
Au80Sn20	Au



FIB cross section of electroplated Cu-Ni-Au pixel pad

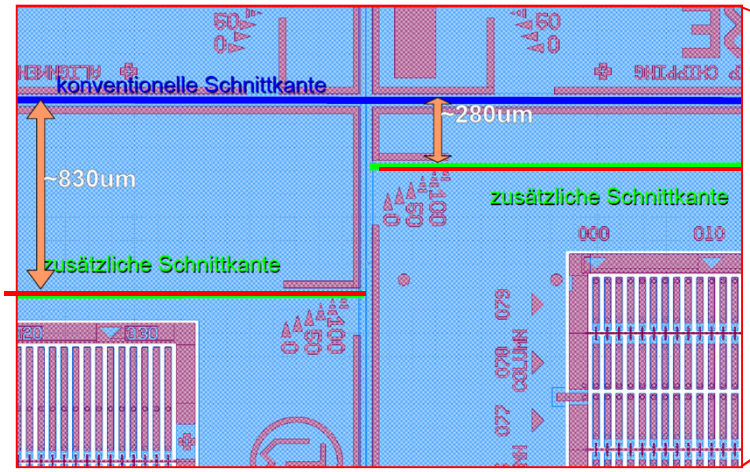
Formation of Interconnects on Sensor Side:

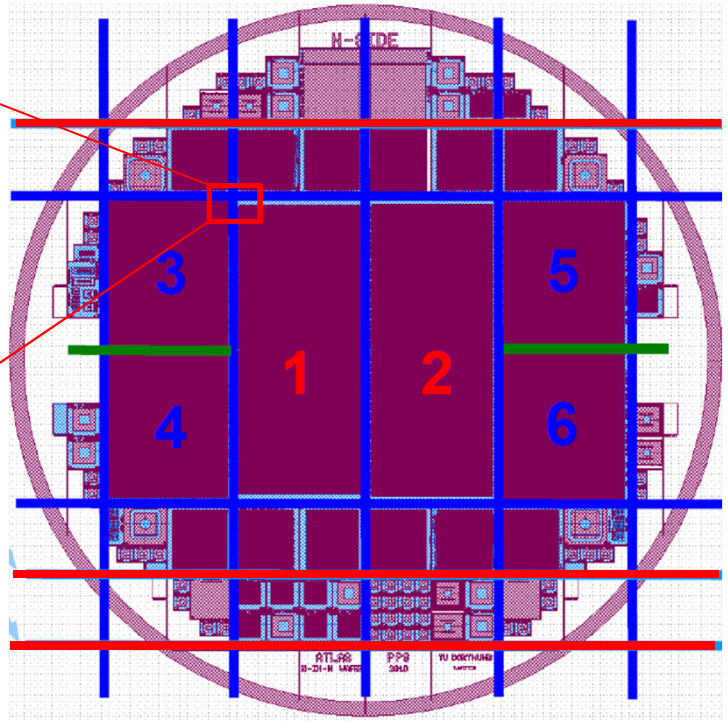
- Sputtering of adhesion layer / diffusion barrier (Ti:W)
- Sputtering of plating base (Cu, Au, Ni, …)
- Resist patterning by mask lithography
- UBM deposition (electroplating)
- Resist stripping / Plating base etching
- Dicing



thomas.fritzsch@izm.fraunhofer.de

Sensor Wafer Design – recommendations for future detectors





ATLAS FE-I4 prototype design

Saw dicing adapted design means:

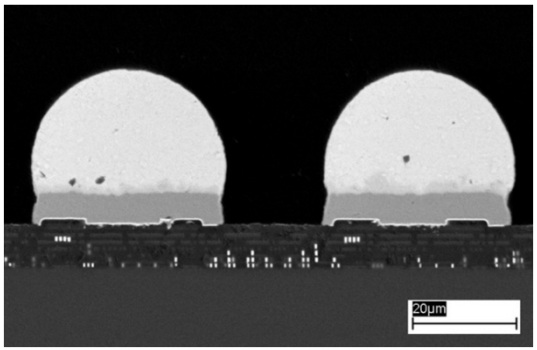
- Avoid different dicing step distances (blue/red)
- Edge-to-edge dicing streets (blue OK / green BAD)
- Avoid single part dicing (singulation of sensor 3,4,5,6)
- Tolerance calculation adapted to mechanical dicing process (+/- 10…20µm)
- Dicing cut is located in the center of the dicing street

thomas.fritzsch@izm.fraunhofer.de

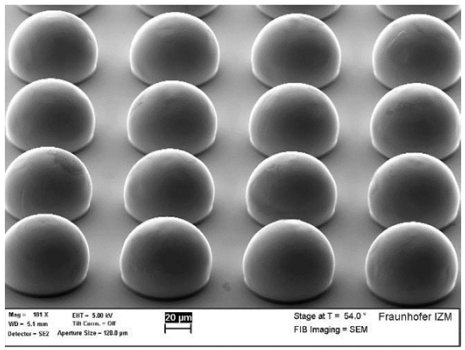
Wafer Level Packaging for Hybrid Pixel Detectors

Solder Deposition on Readout Chipwafer

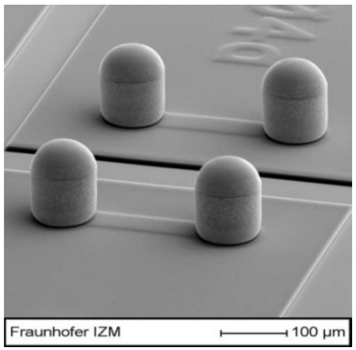
SnAg3.5



Indium



Cu-Sn Pillar

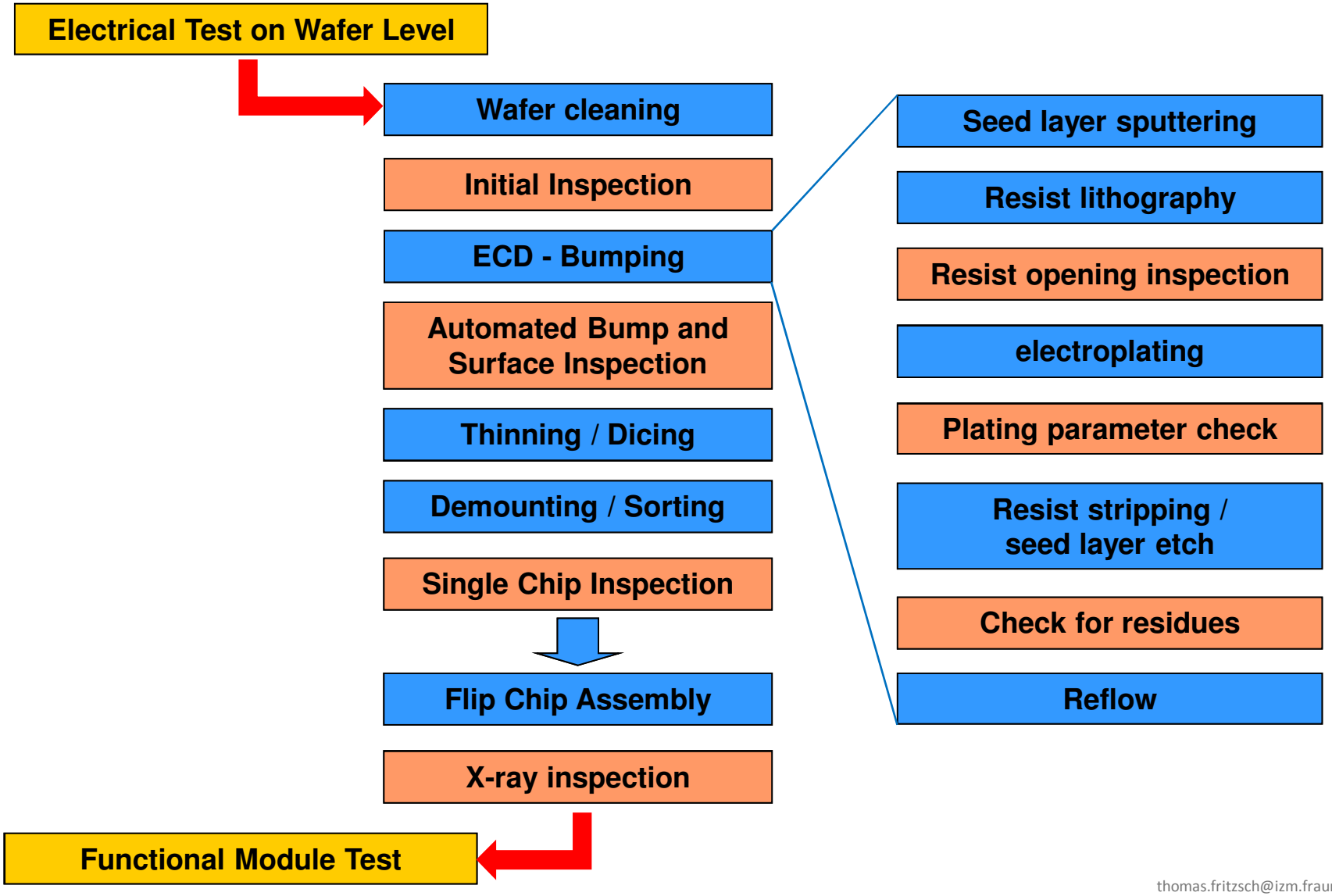


Formation of interconnects on readout chip side:

- Sputtering of adhesion layer / diffusion barrier (Ti:W, Ti, Cr, …)
- Sputtering of plating base (Cu, Au, Ni, …)
- Resist patterning by mask lithography
- UBM deposition (electroplating): Cu, Ni,
- Solder material deposition (SnPb, SnAg, In, AuSn, CuSn, …)
- Resist Stripping / Plating Base Etch
- Reflow (optional)

thomas.fritzsch@izm.fraunhofer.de

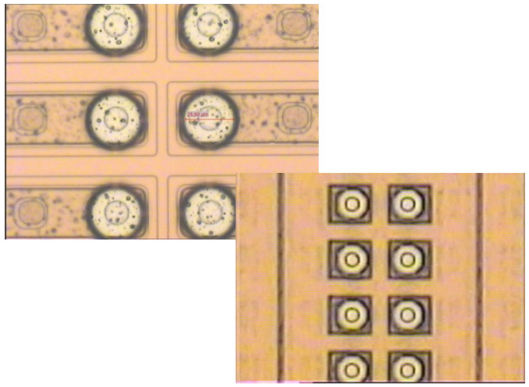
Readout Chipwafer – Prozess Flow

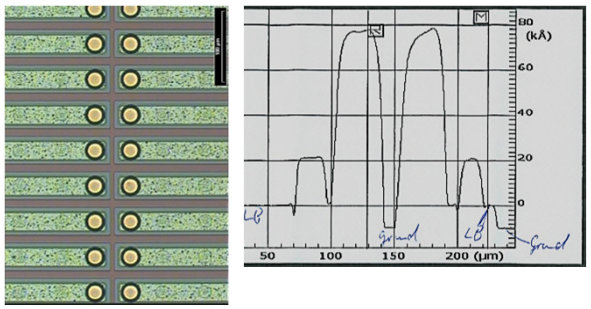


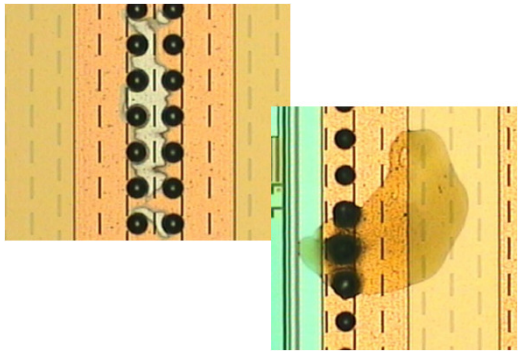
thomas.fritzsch@izm.fraunhofer.de

Process Control – Readout Wafer Bumping

Lithography: Resist opening inspection	Electroplating: Plating parameter check	Plating Base Etch: Check for residues
▪ Optical microscope ▪ via dimensions ▪ Resist defects (bubbles, closed vias)	▪ 3D Surface Profiler ▪ Structure height measurement	▪ Optical microscope ▪ Resist and plating base residues
➢ Avoid plating defects ➢ Rework possible	➢ Check defined structure height ➢ Adjust plating parameters	➢ Avoid isolating residues ➢ Avoid pixel shorts



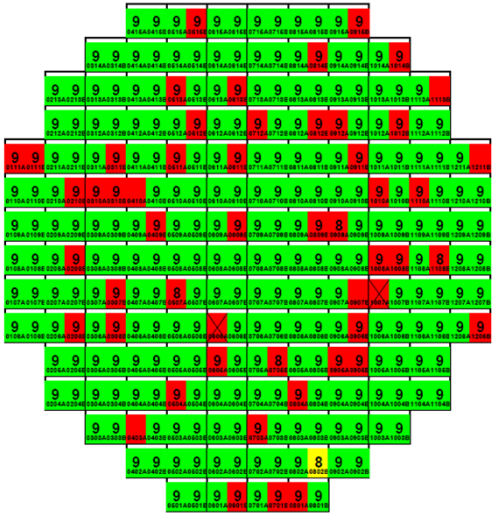




thomas.fritzsch@izm.fraunhofer.de

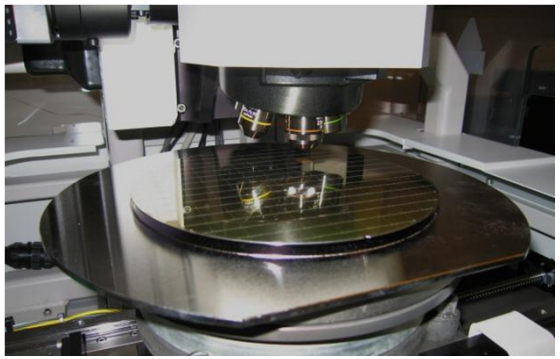
Quality Assurance – Readout Chip Wafer

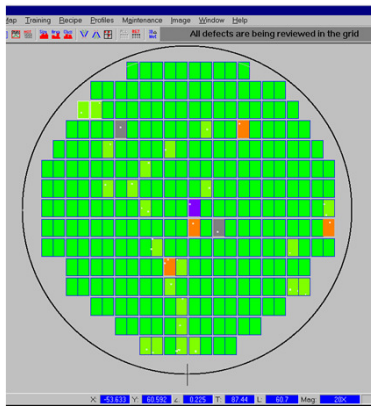
Electrical test on wafer level

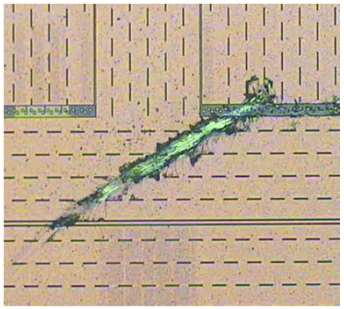


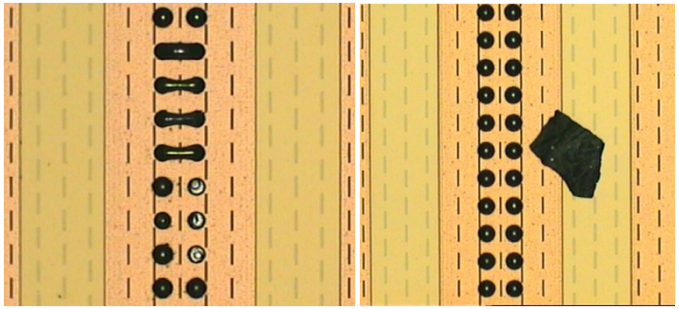
good | class 2 | bad

Automated bump and surface inspection





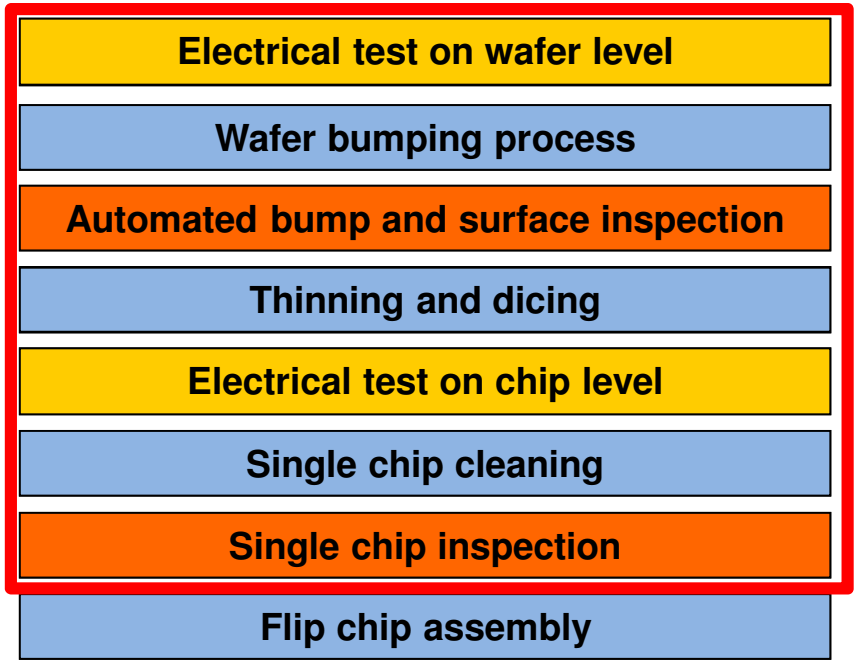




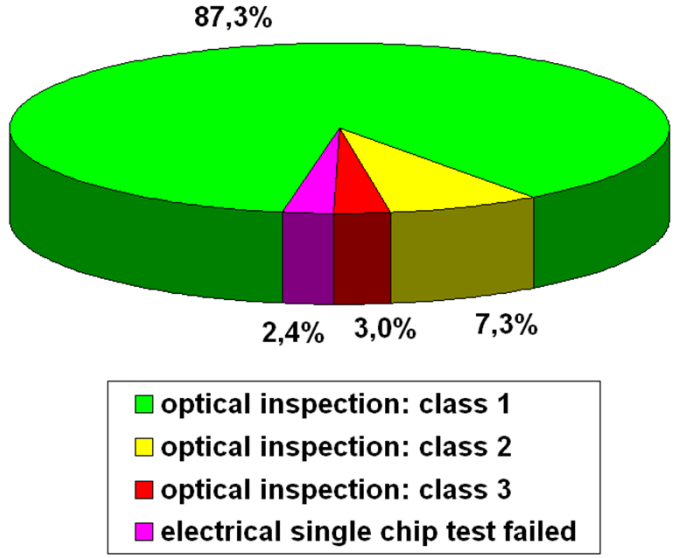
Only electrically good tested chips without bump defects are used for module assembly

thomas.fritzsch@izm.fraunhofer.de

ATLAS Bare Module Production – Readout Chip Yield



20.720 processed Readout Chips
functional good tested on wafer level



Conclusions:

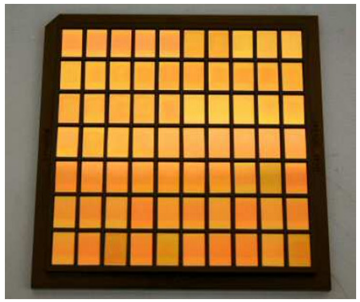
- 94,6% of readout chips can be used for flip chip assembly
- Only 2,4% electrically BAD after bumping process
- Number of single chip process steps (test – cleaning – inspection) can be reduced (reduction of manual single chip handling steps!)
- Development of reliable module rework process instead of functional single chip test

thomas.fritzsch@izm.fraunhofer.de

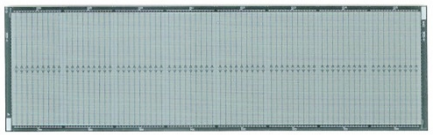
Flip Chip Assembly

- Sensor placement in flip chip tool
- Pick&Place of readout chip
- Reflow
- X-ray inspection

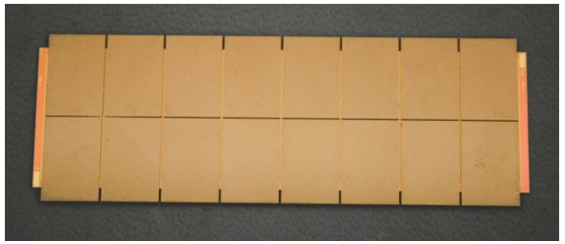
Readout chip:



Sensor tile:



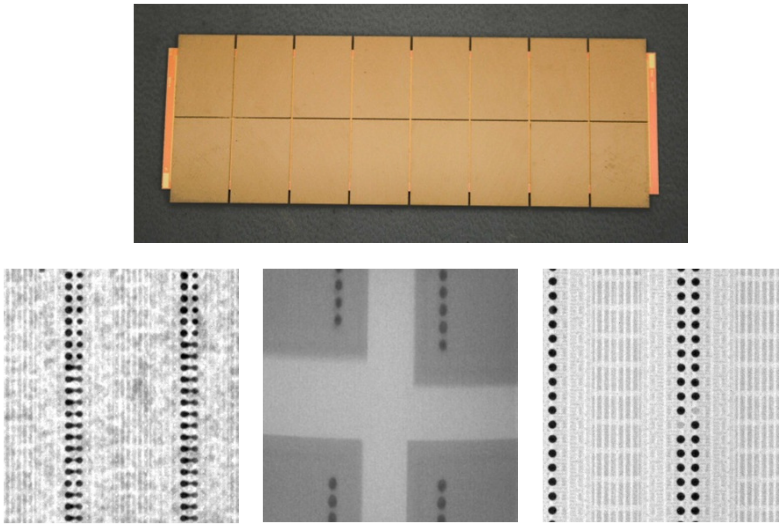
Bare Module



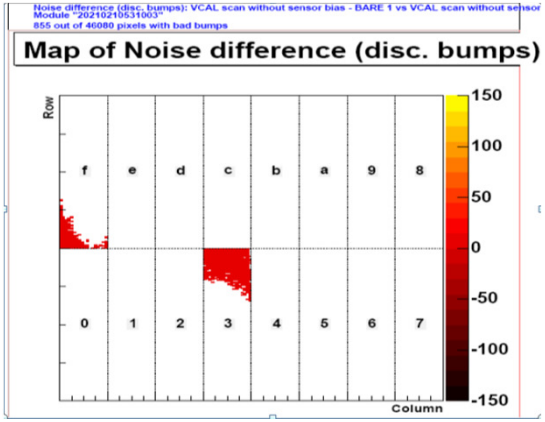
thomas.fritzsch@izm.fraunhofer.de

Quality assurance after flip chip assembly

X-ray inspection



Functional module test



Detection:

- Bridged bumps
- Missing bumps
- Misplaced chips
- But no open contacts detectable

- Disconnected bumps detectable
- chip test using probe needles necessary
- Chip rework after board assembly possible?

➢ reliable rework process for chip exchange even after functional module test

thomas.fritzsch@izm.fraunhofer.de

Outline

Wafer Level Packaging and Flip Chip Assembly for Hybrid Module Manufacturing

- Wafer Level Packaging Equipment
- Processes on Wafer Level
- Flip Chip Assembly
- Additional technologies for future detector modules:
  - Single chip processing for prototypes
  - Thinned readout chip – flip chip assembly

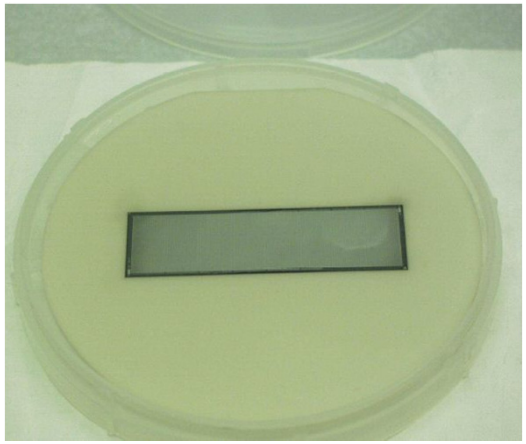
thomas.fritzsch@izm.fraunhofer.de

Single Chip Processing for Hybrid Module Prototypes

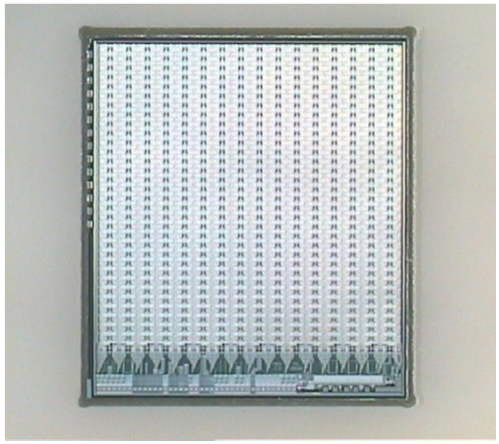
Situation:

- Readout-Chip or Sensor-Prototypes → only a few chips from MPW Batches are available
- Need for functional hybrid test modules
- But bumping processes only available on wafer level

Solution: Single chip embedding into carrier wafer



ATLAS 16-chip poly-crystal diamond sensor embedded into 100mm ceramic wafer



Readout chip after single chip bumping

thomas.fritzsch@izm.fraunhofer.de

Single Readout Chip Bumping

Single chip process	Wafer process
Measurement of chip dimensions	
Design of embedding wafer	
Ceramic wafer laser cutting	
Ceramic wafer cleaning	
Chip embedding	
Plating base sputtering	Plating base sputtering
Lithography resist	Lithography resist
Electroplating Bump metal	Electroplating Bump metal
Stripping resist	Stripping resist
Resist stripping/Plating base etch	Resist stripping/Plating base etch
Dicing and detaping	Dicing and detaping
Single Chip Cleaning	
Flip chip assembly	Flip chip assembly

thomas.fritzsch@izm.fraunhofer.de

Single Chip Processing on Wafer Level

Individual chip embedding

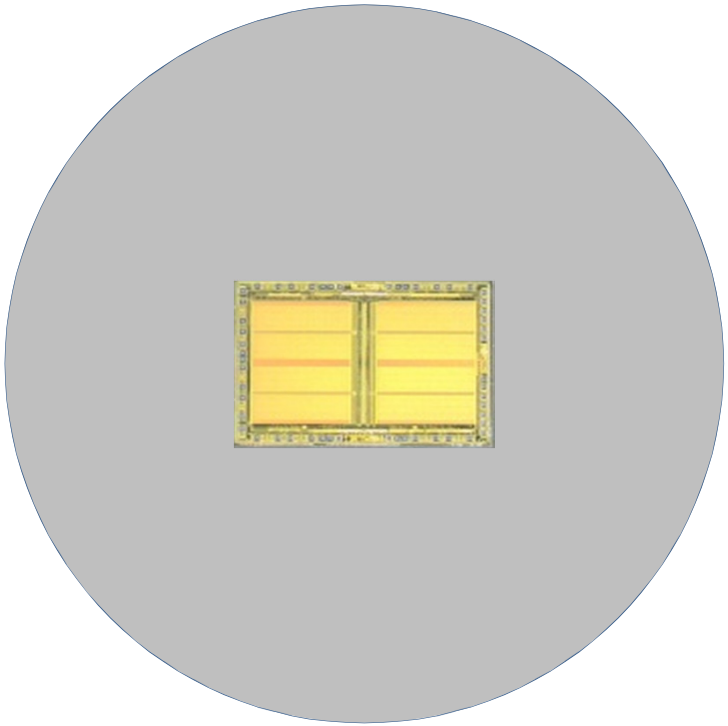
- Small structure size
- Narrow tolerances

Example:

- Passivation opening Ø 14µm
- Bumping 24µm size/ pitch 50µm
- Circumferential bump-passivation overlap of 5µm

Approach:

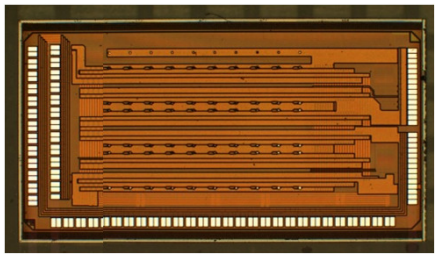
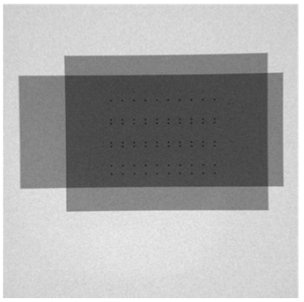
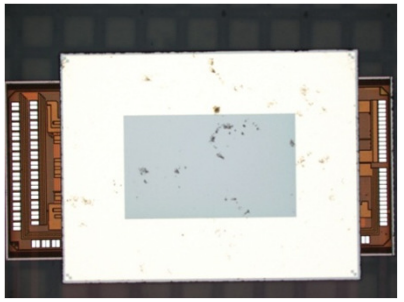
- One chip embedded per wafer
- Mask alignment on chip features (i.e. pads)



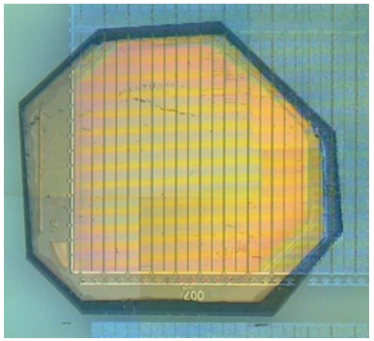
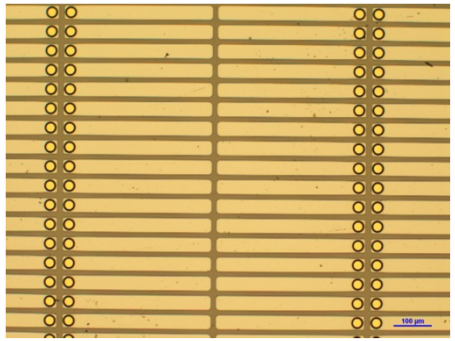
thomas.fritzsch@izm.fraunhofer.de

Single Readout Chip Bumping / Diamond Sensor Chip Processing

Examples:

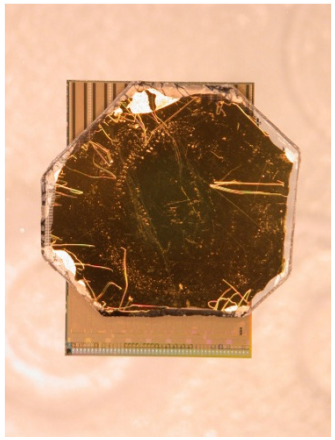
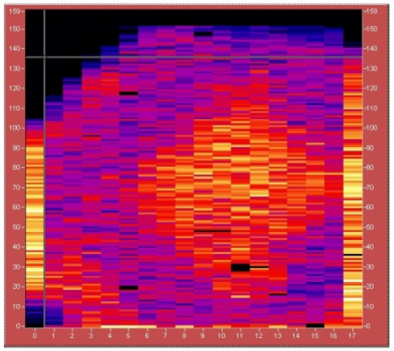





CERN NA62 Readout Chip - single chip bumping

ATLAS Diamond single crystal sensor chip:

Single chip pixel patterning and pad metallization

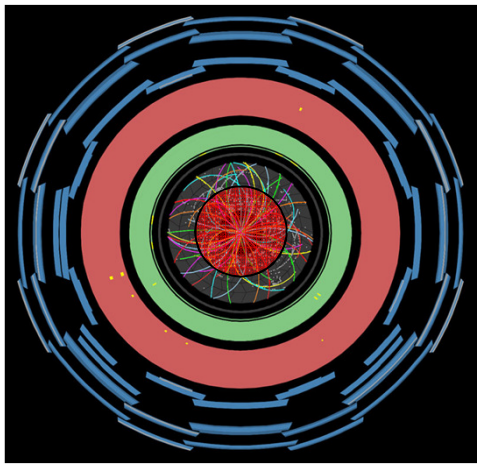
After flip chip assembly / functional test

Courtecy of Bonn University

thomas.fritzsch@izm.fraunhofer.de

Thinned Readout Chip – Flip Chip Assembly

Motivation: Reduction of material budget in future detectors



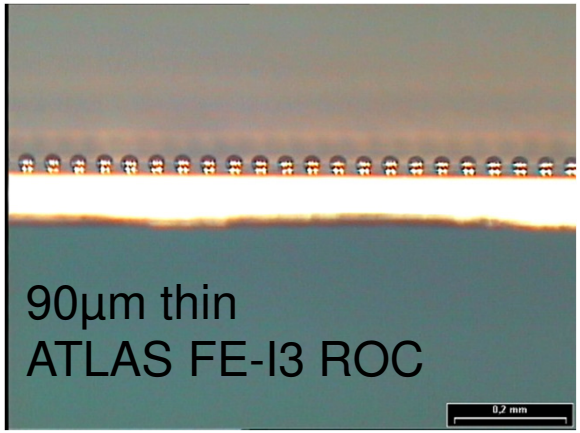
ATLAS Pixel Tracking Detector

	% X_0
Old BL @ R=5 cm	2.7
New BL @ R=3.2 cm	1.5

(F. Huegging, PIXEL 2010)

Established thinning process:

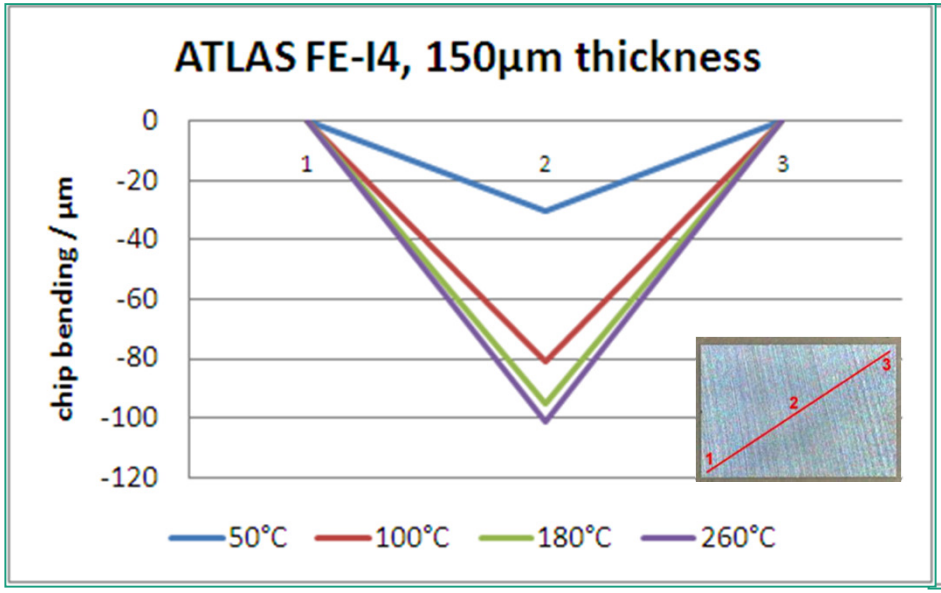
1. Mechanical wafer grinding
2. Stress relief:
   - Polishing
   - Wet chemical etching
   - Plasma etching



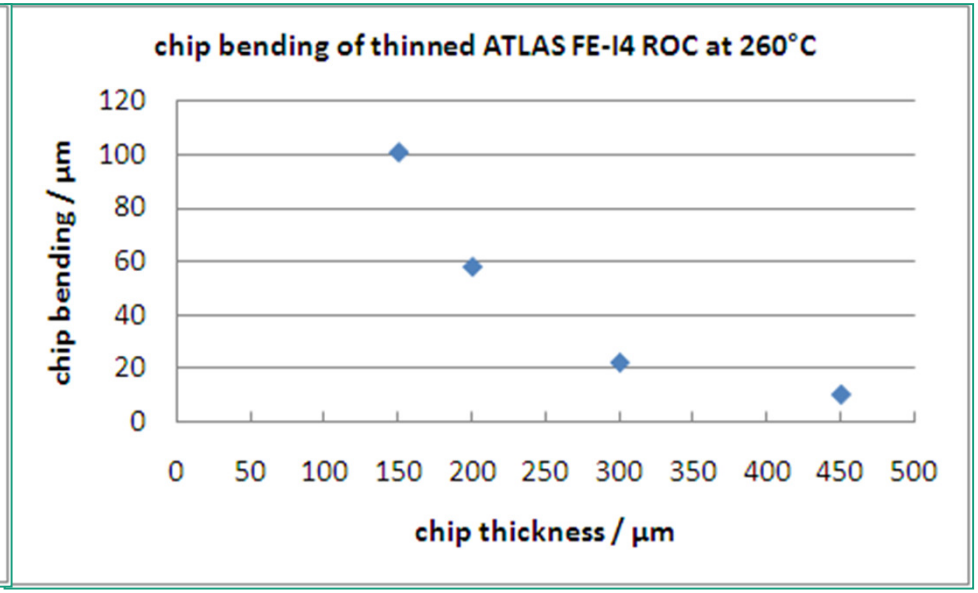
thomas.fritzsch@izm.fraunhofer.de

Thinned Readout Chip – Flip Chip Assembly

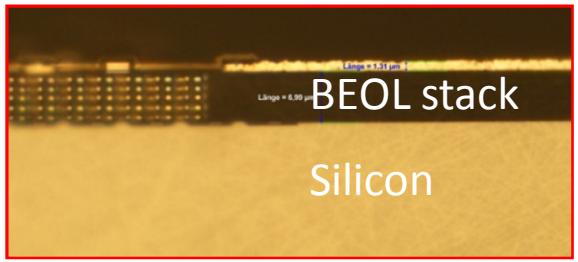
Chip Bending – ATLAS FE-I4 ROC



100µm chip bending @ 260°C



Chip bending measured on FE-I4 ROCs
Single chips thinned to several thicknesses

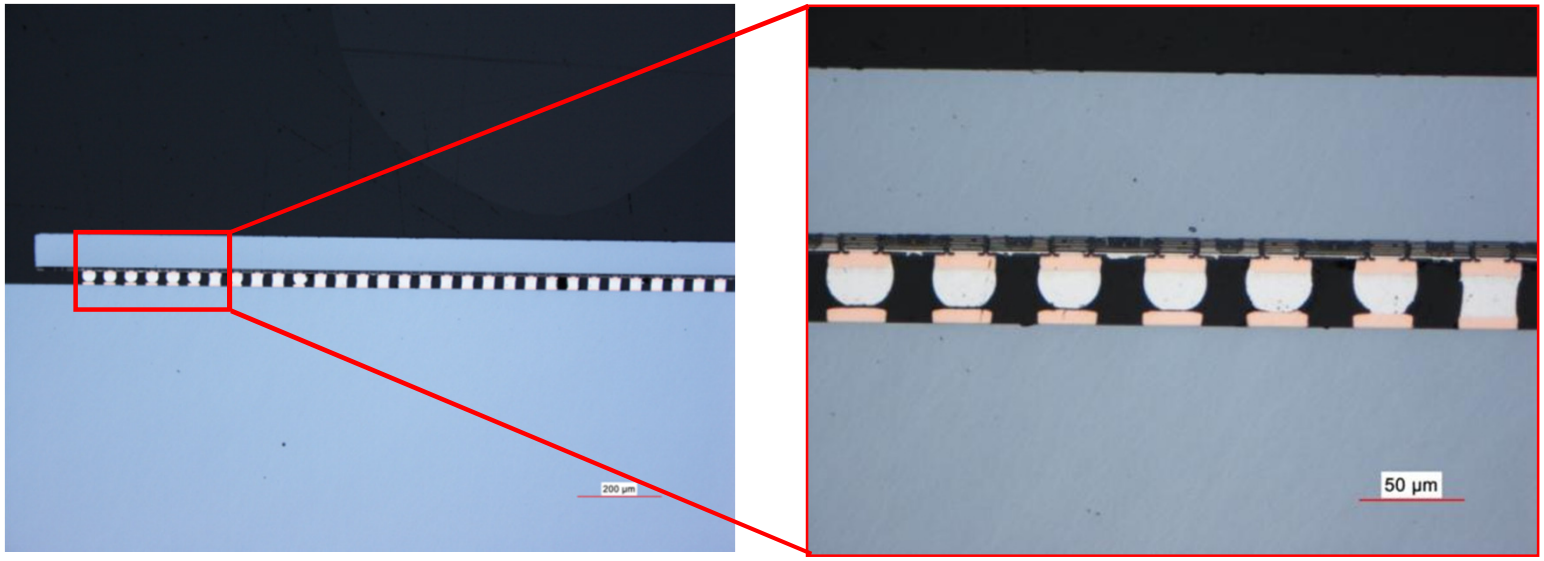


Chip bending as a result of thermal bi-layer effect (Al/oxid stack – silicon) and internal stress after processing

thomas.fritzsch@izm.fraunhofer.de

Thinned Readout Chip – Flip Chip Assembly

Chip Bending at Reflow Temperature – Cross Section



Avoid chip bending during bonding process:

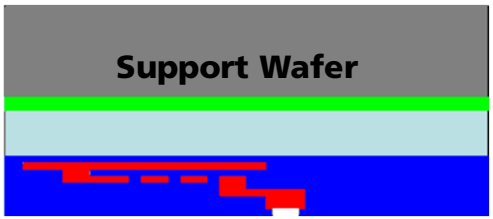
increase chip stiffness during bonding → support carrier approach

thomas.fritzsch@izm.fraunhofer.de

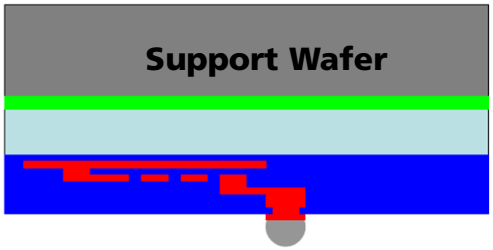
Thinned Readout Chip – Flip Chip Assembly

Flip Chip Assembly using Temporary Support

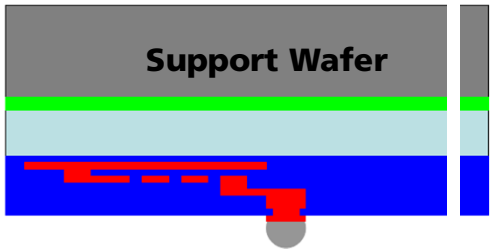
ROC Wafer Thinning



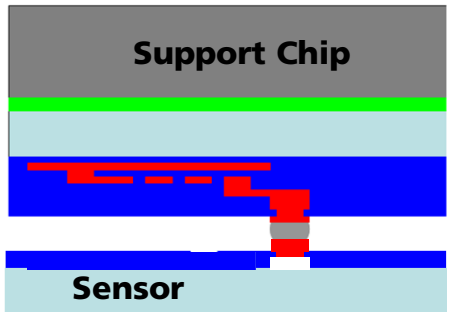
Temporary Wafer Bonding to support wafer



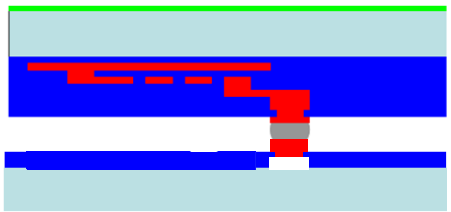
Contact formation (Micro-Bumping)



Dicing of Wafer Stack



Bump Bonding



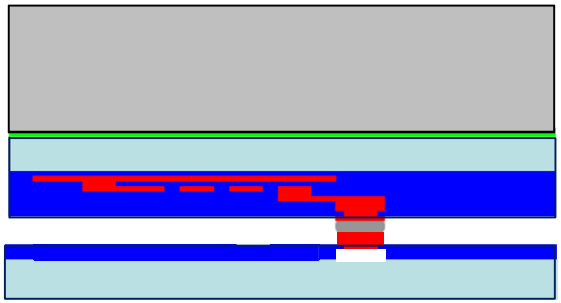
Support Chip Release

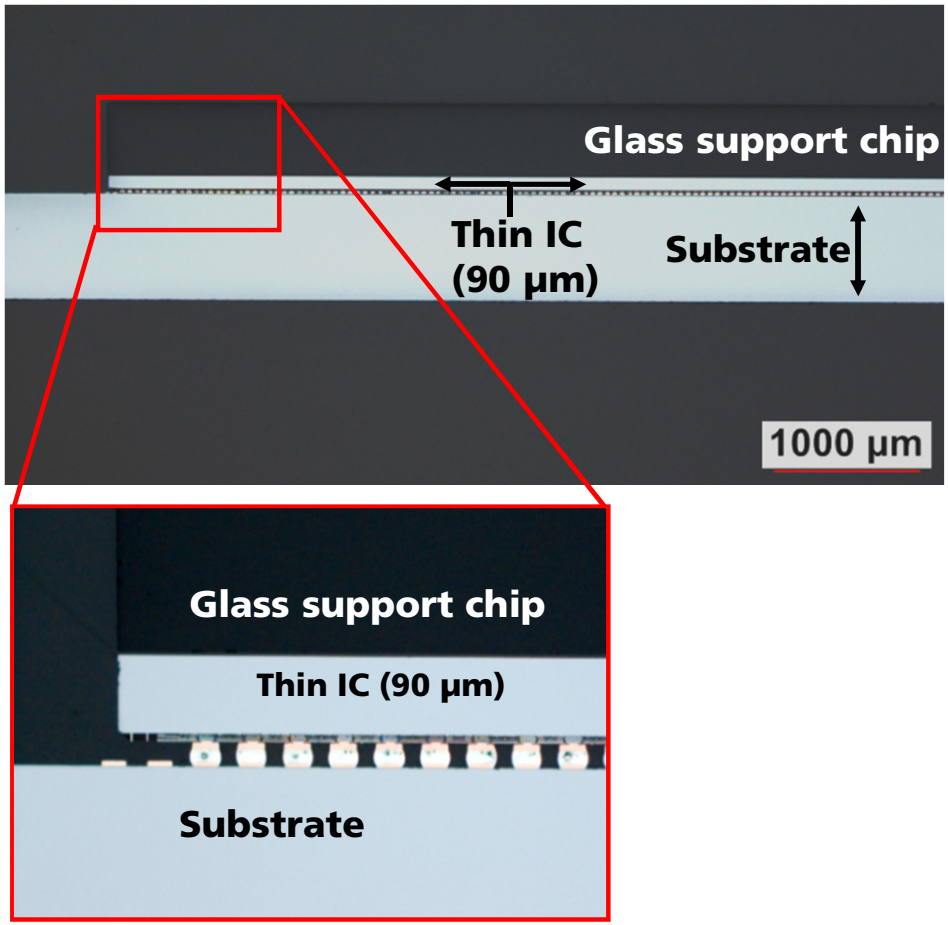
thomas.fritzsch@izm.fraunhofer.de

Thinned Readout Chip – Flip Chip Assembly

1. Step: Flip Chip Assembly

ATLAS FE-I3: 90µm thickness



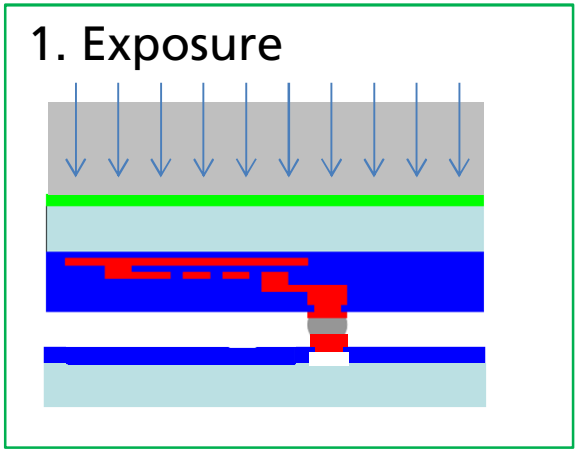


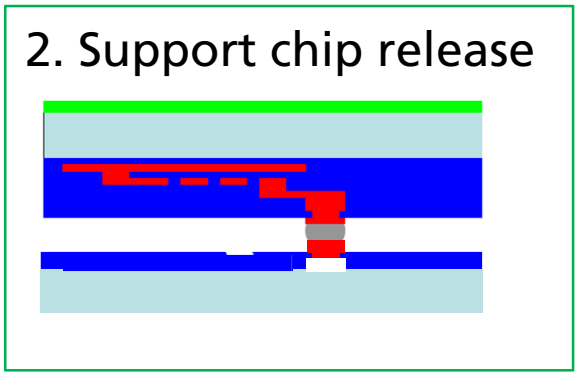
Cross section of the first bump row:
No open interconnects can be found

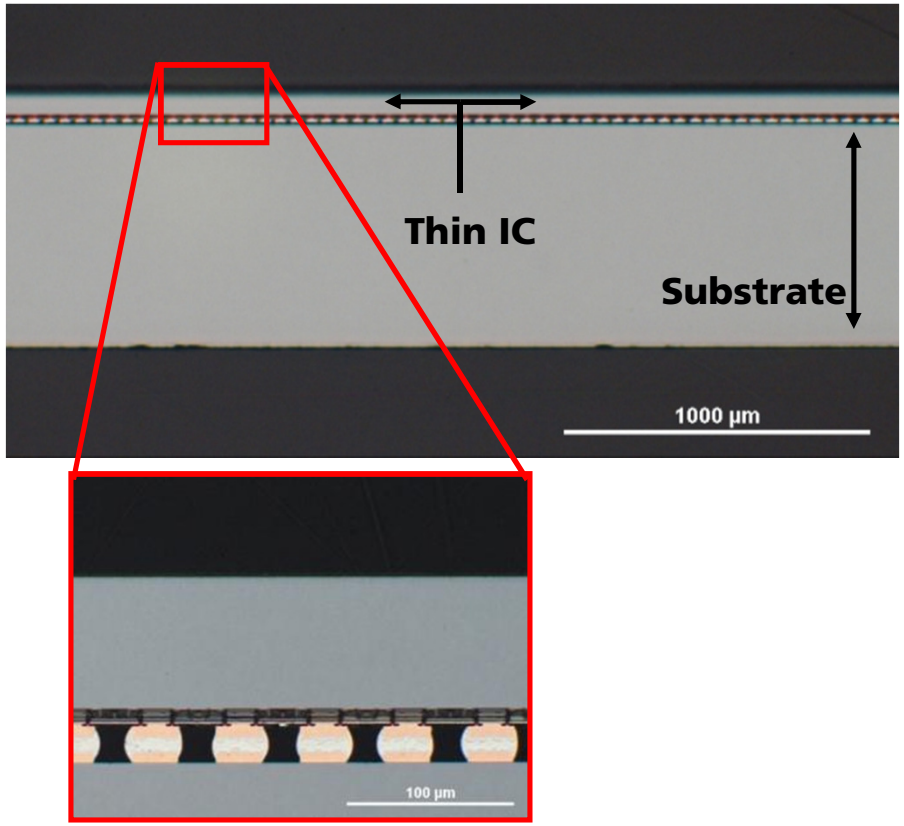
thomas.fritzsch@izm.fraunhofer.de

Thinned Readout Chip – Flip Chip Assembly

2. Step: Carrier Release





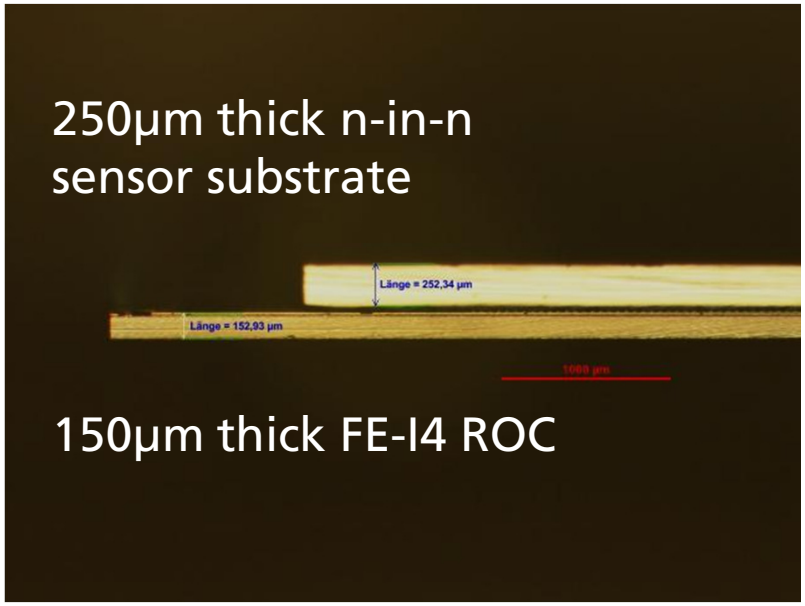


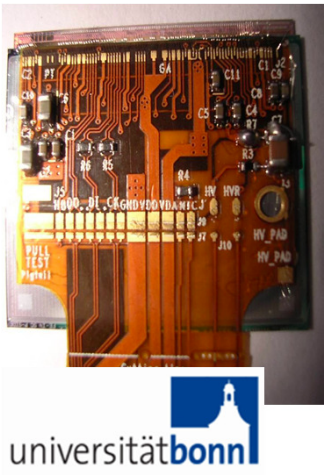
thomas.fritzsch@izm.fraunhofer.de

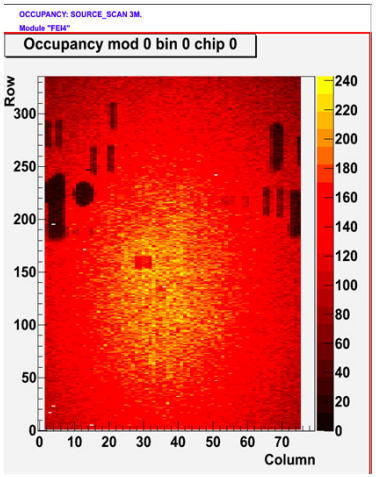
Thinned Readout Chip – Flip Chip Assembly

Thin Chip Assembly using ATLAS FE-I4 ROCs

- FE-I4 ROC, thickness 150µm/100µm assembled on functional sensor tiles
- Release of carrier chip successful
- First functional module tests successful







^{241}Am source scan with 3 million triggers done at modules assembled and tested at Genova

thomas.fritzsch@izm.fraunhofer.de

Summary

Wafer Level Packaging and Flip Chip Assembly for Hybrid Module Manufacturing - Quality Issues -

- Industry standard wafer level packaging equipment for stable processes (sputtering, resist deposition, lithography, electroplating, thinning, dicing)
- Several inspection and measurement steps during bumping process flow (electrical test, inspection after individual process steps, bump inspection)
- Inspection after flip chip assembly using x-ray (merged and missing bumps but no open interconnects detectable)
- Additional technologies for future detector modules:
  - Single chip processing for prototypes (sensors and readout chips)
  - Thin chip assembly using 150µm/100µm ROCs successfully tested
  - going further to reduced thickness (ALICE/NA62 test batch with silicon thickness down to 50µm)

thomas.fritzsch@izm.fraunhofer.de