

Workshop on Quality Issues in
Present and Future Silicon Detectors
CERN, 3-4 November 2011

Experience with the Test and Qualification of ALICE Double-Sided Microstrip Sensors

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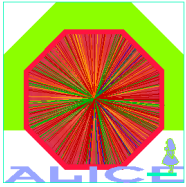
OUTLINE

1. Sensor Description
2. Acceptance Tests
3. Surface Effects
4. Noise Measurements



1. Sensor Description

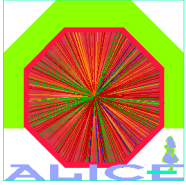




Sensor Type and Geometry

- Double-sided strip detector
- AC-coupled strips
- **Punch-Through biasing** on both sides
- Overall size: 75mm X 42mm
- 300 μ m thickness
- 768 strips on each side
 - 40mm long
 - 95 μ m pitch
 - **35 mrad stereo angle**
 - + 7.5 mrad strip angle on p-side
 - 27.5 mrad strip angle on n-side
- ‘DC’ pads contacting the implanted strips at each end
- ‘AC’ pads contacting the metal strips close to each end





ALICE Silicon Microstrip Sensors: Numbers

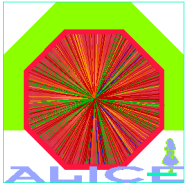
- 2095 sensors supplied by three manufacturers:
 - 1126 Canberra
 - 336 Sintef
 - 633 FBK-Irst
- Pre-series sensors (20 from each supplier) delivered in July 2002
- Series production:
 - started early 2003
 - completed April 2006
- ~ **2400** sensors tested (including pre-series and rejects)
at one testing location (INFN Trieste)

The largest supply of this kind of sensors so far



2. Acceptance Tests





Sensor testing in Trieste



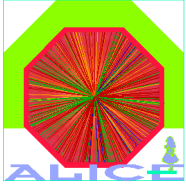
Hardware:

- Alessi REL55 **semi**-automatic prober
- I - V and C - V testing instruments + scanner

Software:

- “M-Shell” set of LabView programs for control, data acquisition and analysis (developed by R.Wheadon, INFN Torino)



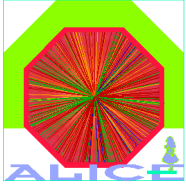


Set-up for sensor testing

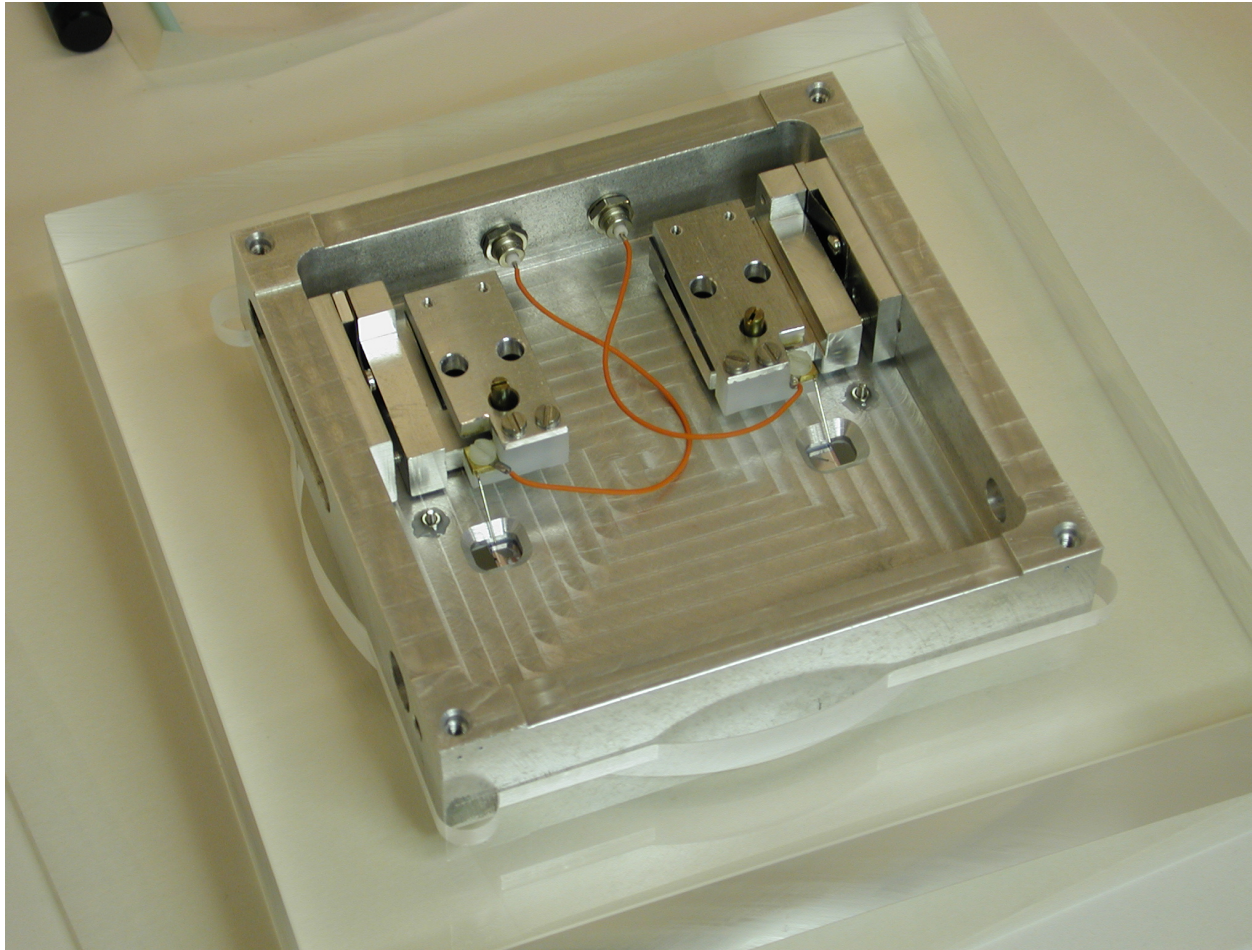


Sensor held on
dedicated support

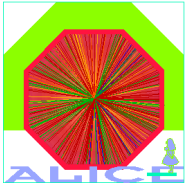
- teflon-clad mounting surface
- plastic clamps (delrin)



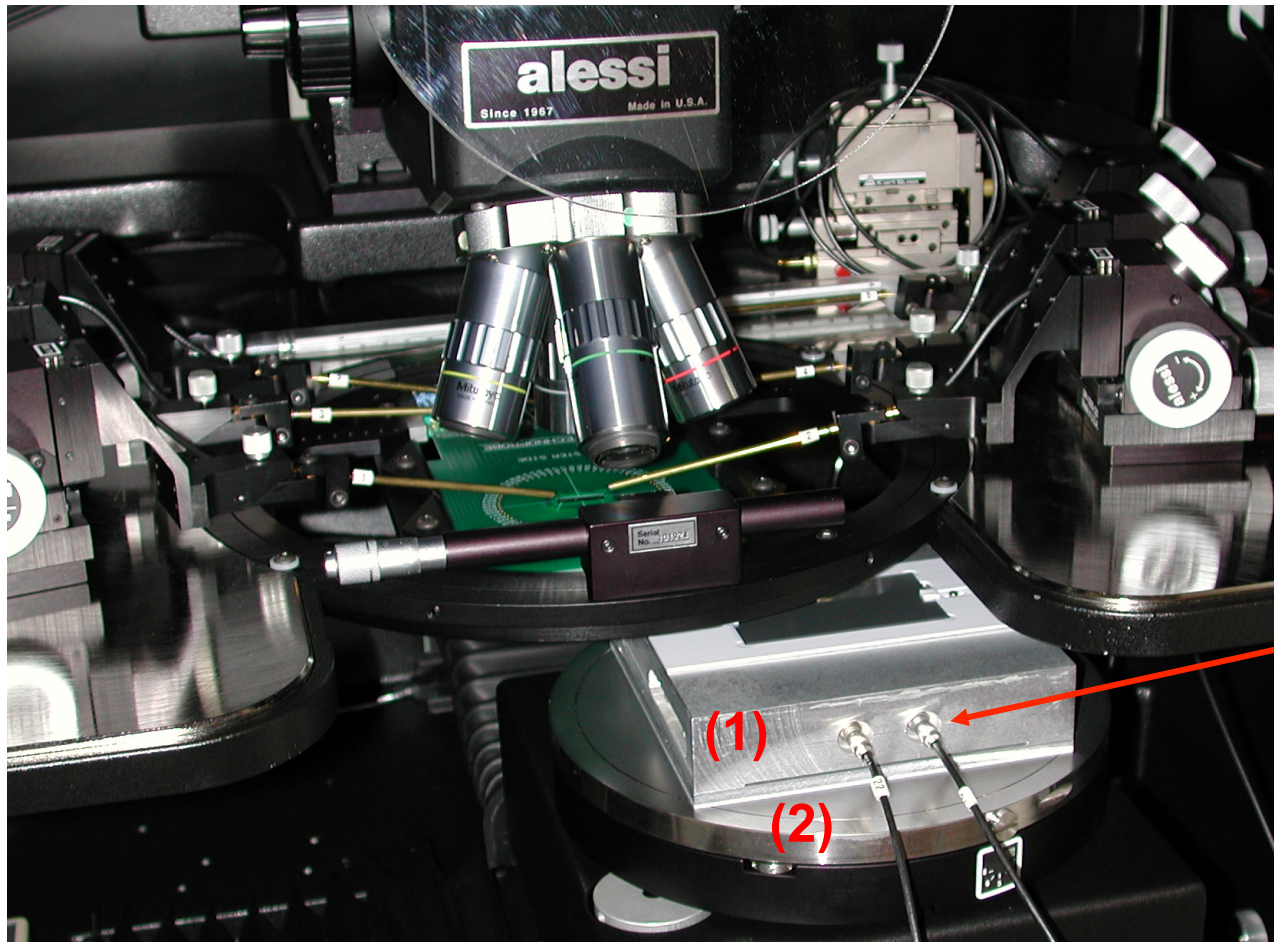
Set-up for sensor testing



Contacting
back-side
Guard Ring
and Bias Ring
by two small
manipulators
inside the
detector support

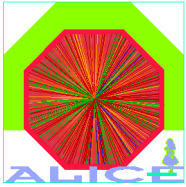


Set-up for sensor testing

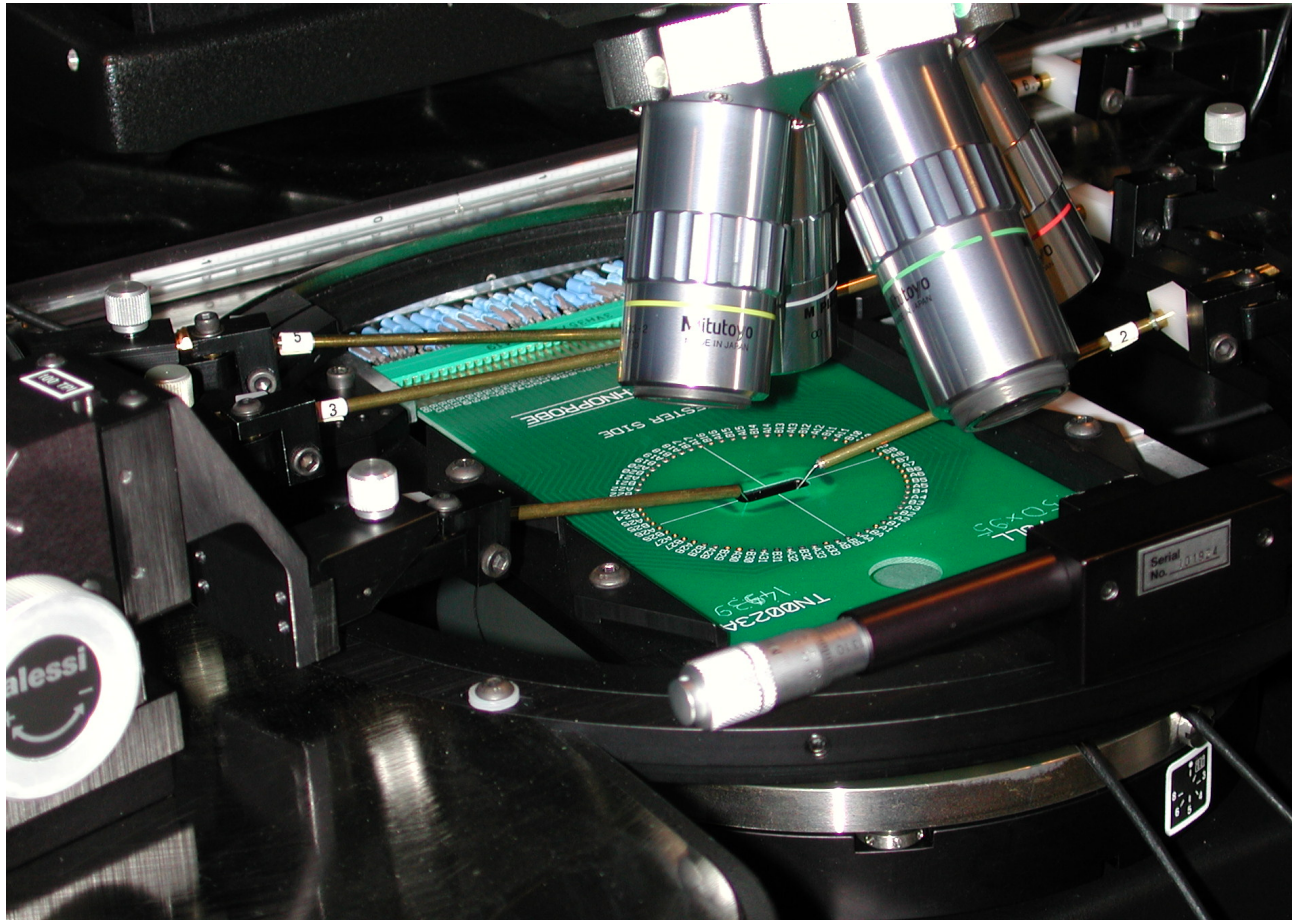


The detector support (1) is mounted on the probe station chuck (2)

- held by vacuum
- contacts to backside Bias and Guard Rings available through two coaxial connectors

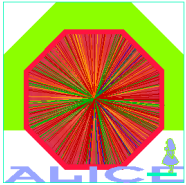


Set-up for sensor testing

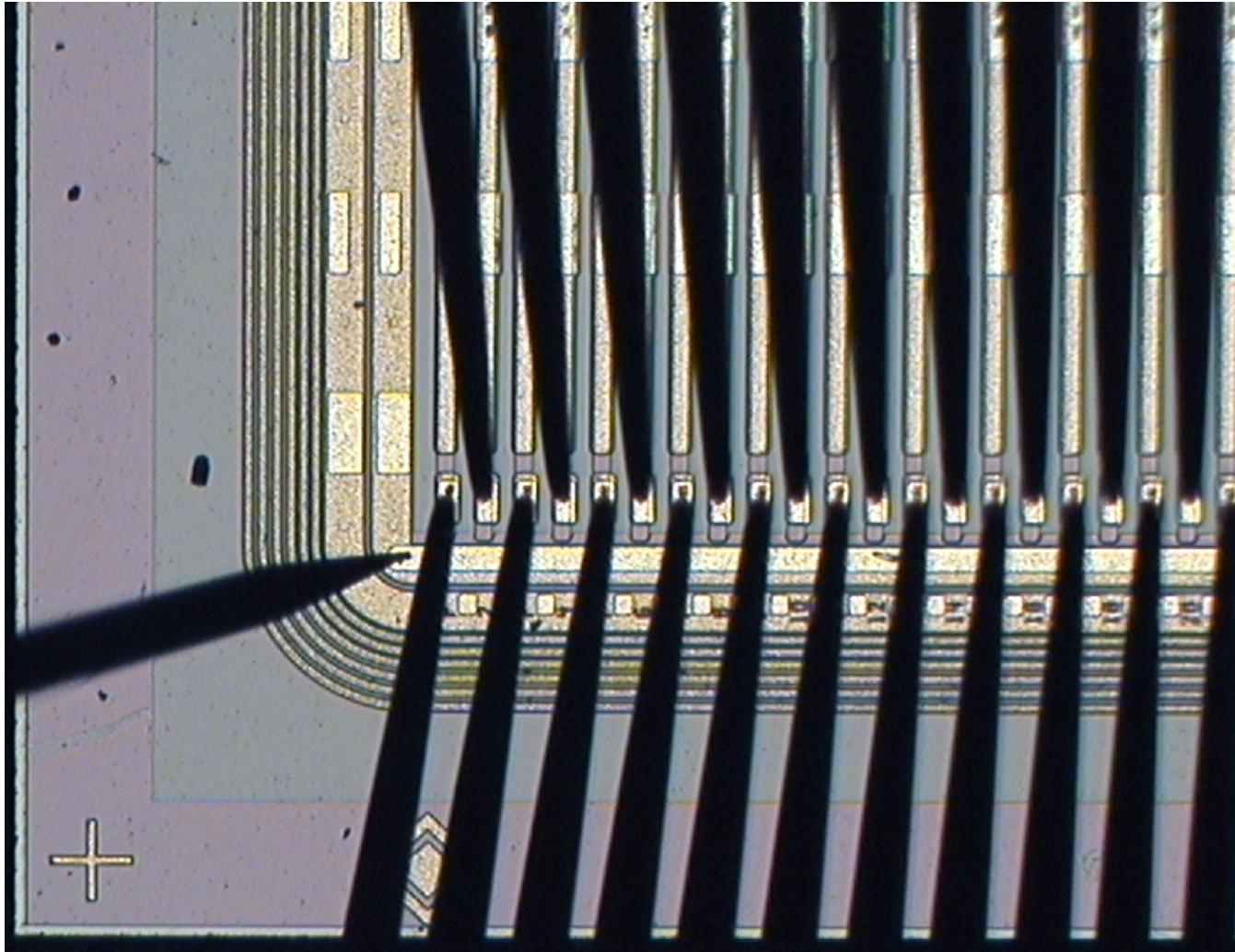


Probing the detector top side with:

- a probe card to contact 50 strip pads
- two manipulators for Bias Ring and Guard Ring

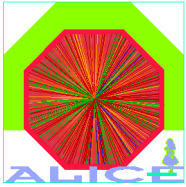


Set-up for sensor testing



Measuring the 'DC' pads of a detector





Test Sequence (1)

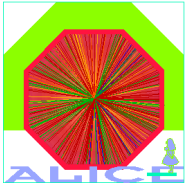
n - side

- 1) AC strip test on n-side (768 pads).
20V across capacitors, light on. Measure:
 - Capacitance to bulk (1 kHz)
 - Dissipation factor
 - Leakage current through capacitor

- 2) I-V Measure (0-100V) on
 - Guard Ring-p, Bias Ring-p
 - Bias Ring-n
 - one n-side Strip (→ insulation voltage)

- 3) Measure of Punch-Through voltage drop between Bias Ring and two different strips, versus bias voltage.





Test Sequence (2)

- 4) DC strip test on n-side (768 pads).
40-70V bias (chosen depending on results of 2.)

Measure:

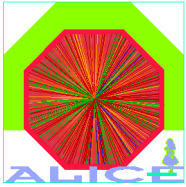
- Leakage current of every strip
- Insulation resistance of every strip at bias voltage: $(\Delta I / \Delta V)^{-1}$, with $\Delta V = 0.2$ V
- Bias Ring and Backside current once every probe card position (16 points)
- Insulation bias voltage for one strip in every probe card position (16 points)

p-side

Repeat Measurements 1), 3), 4) on p-side (except no strip insulation voltage is measured during DC scan on p-side)

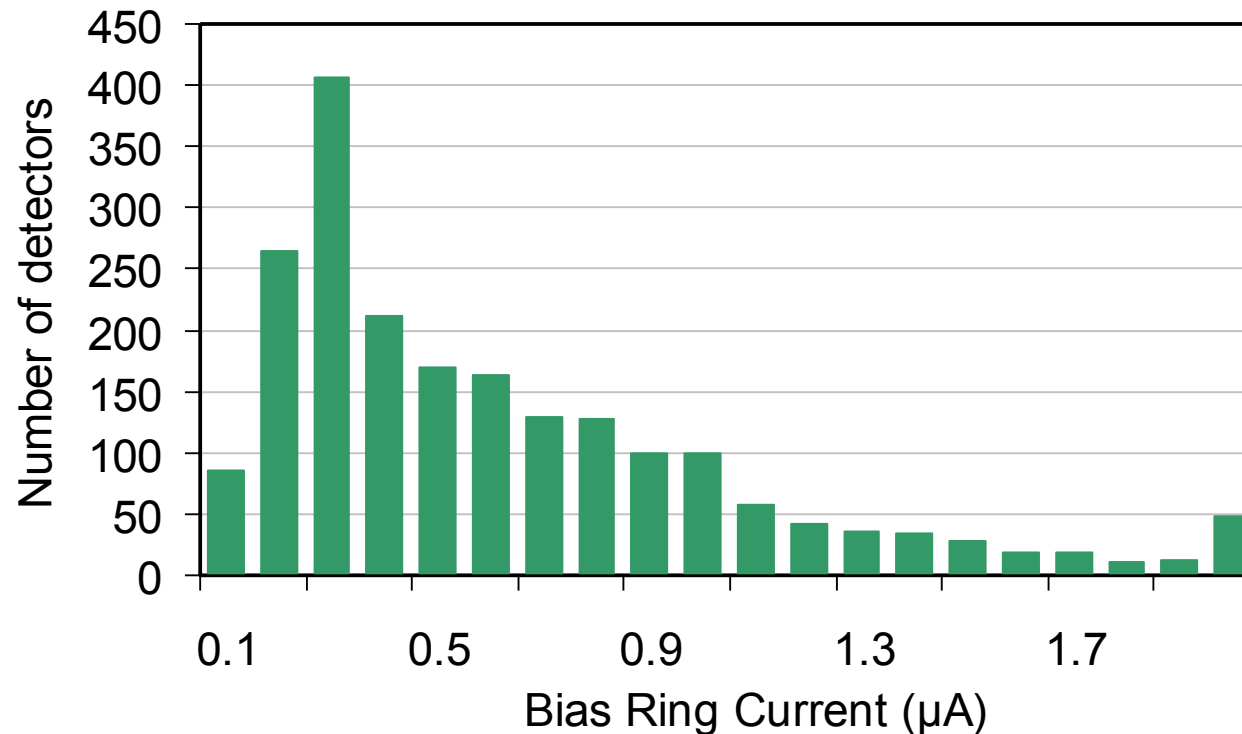
Total time required: ~ 2 hours/detector
⇒ 4 detectors / day (if no problems arise...)





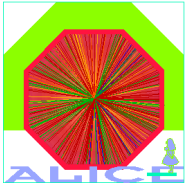
Test Results: Leakage Current

Bias Ring leakage current distribution



Specifications:

- Bias ring current $< 2 \mu\text{A}$ (Measured average $0.61 \mu\text{A}$)
- Guard ring current $< 5 \mu\text{A}$ (Measured average 41 nA)

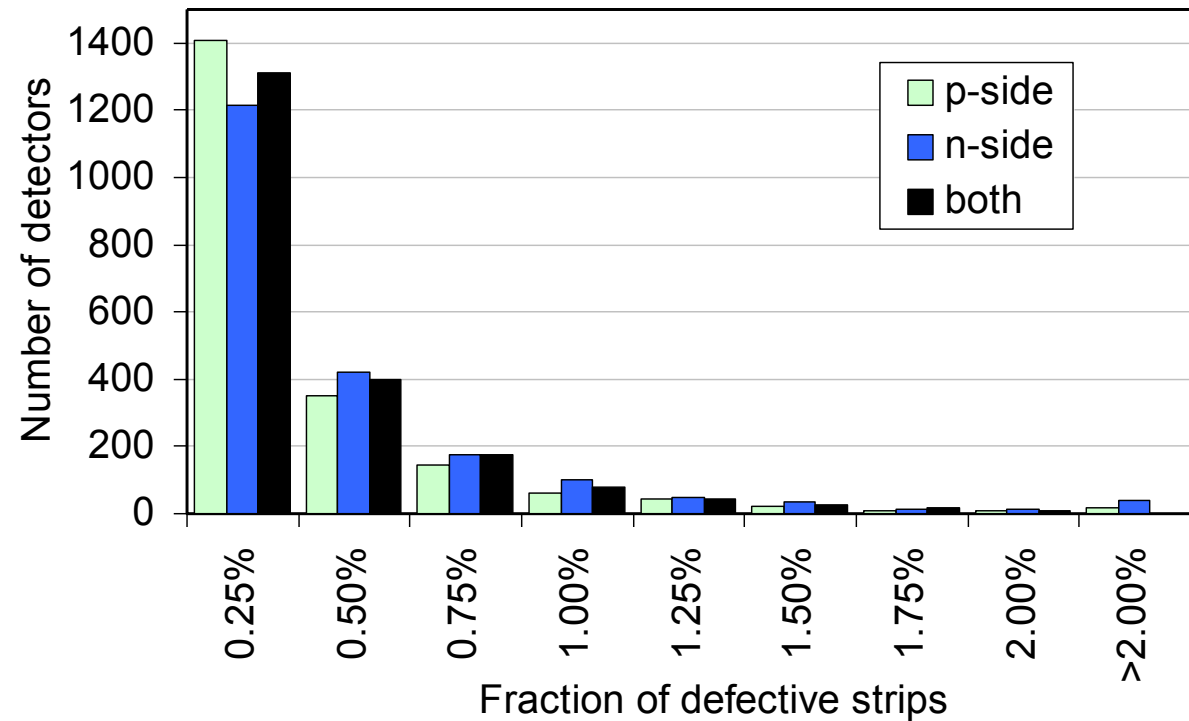


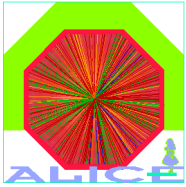
Distribution of defective strips

Defective strips are strips with either:

- Leakage current > 20 nA
- Insulation resistance < 50 M Ω
- Broken AC capacitor
- Metal electrode shorted to adjacent ones
- Open metal electrode

The specification on defective strips is:
total number
(sum of both sides) < 30
($\Rightarrow \sim 2\%$ of all strips).

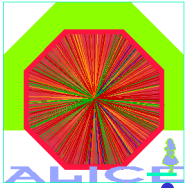




Average number of the various defect types

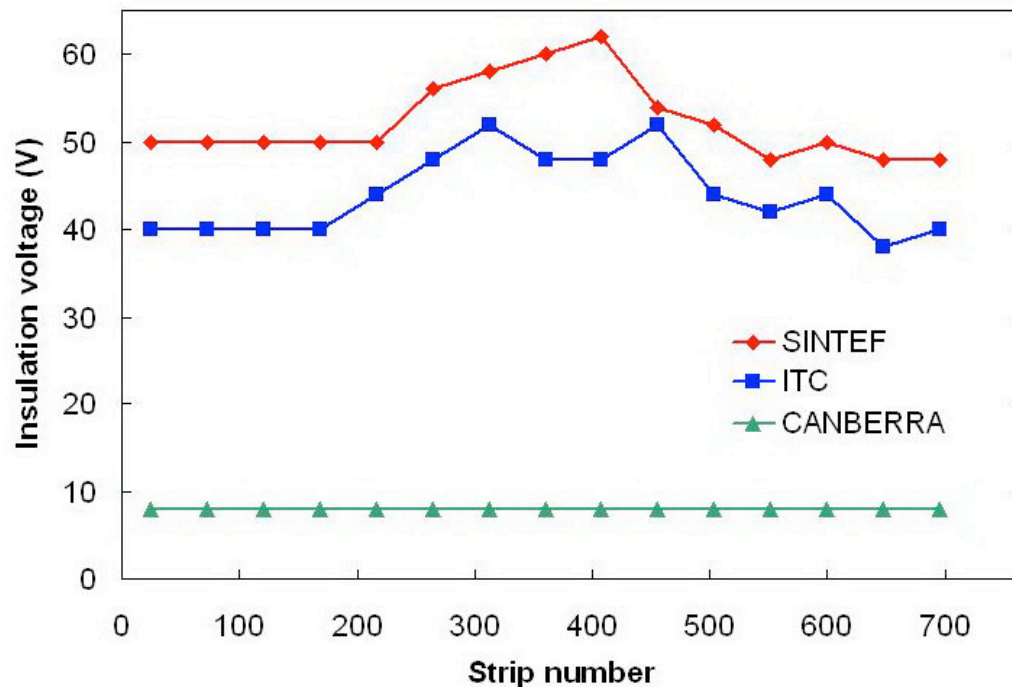
Defect type	<i>p</i> -side	<i>n</i> -side
$I_{leak_strip} > 20 \text{ nA}$	0.60 (0.08%)	0.37 (0.05%)
$R_{insulation} < 50 \text{ M}\Omega$	0.16 (0.02%)	0.71 (0.09%)
Broken Capacitor	0.40 (0.05%)	0.78 (0.10%)
Metal Short	0.12 (0.02%)	0.09 (0.01%)
Metal Open	0.37 (0.05%)	0.31 (0.04%)
Total	1.65 (0.21%)	2.26 (0.30%)

The total defect number is well within specification (2%).

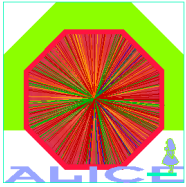


Doping Variation in the Substrate

- We can profile the depletion voltage across the sensor by measuring the voltage at which n -side strips become insulated (routinely done at 15 points on every sensor)
- On FBK and SINTEF sensors there is an increase of 10-20 V from edge to center, reflecting the characteristic doping variations of FZ Si



- Canberra sensors show exceptionally low depletion voltage ($\Rightarrow \rho \approx 30 \text{ k}\Omega \text{ cm}$) and even more surprising uniformity across the sensor ($\approx 70 \text{ mm}$ on a 100 mm wafer)
- Exceptional quality of the substrate \Rightarrow lower electric fields at junction edges \Rightarrow less susceptible to high currents associated with small defects



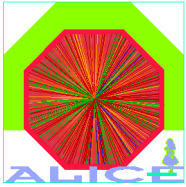
Additional tests

- Measurement of strip capacitance performed on a sampling basis.
- Parametric measurements made on test structures (diodes, gated diodes, MOS capacitors, Van der Pauw structures)
- Stability of leakage current (BR-p and GR-p) for long times (≥ 24 h), under varying humidity conditions (up to 80-90%) performed on a fraction of the sensors.
- Bonding test, to verify the integrity of coupling capacitors after bonding.
 - Performed on the small test detectors (SINTEF), or on dedicated test structures (ITC)
 - Fraction of capacitors damaged by bonding:
 - p-side: $15/17408 = 0.09\%$
 - n-side: $8/17408 = 0.05\%$



3. Surface Effects



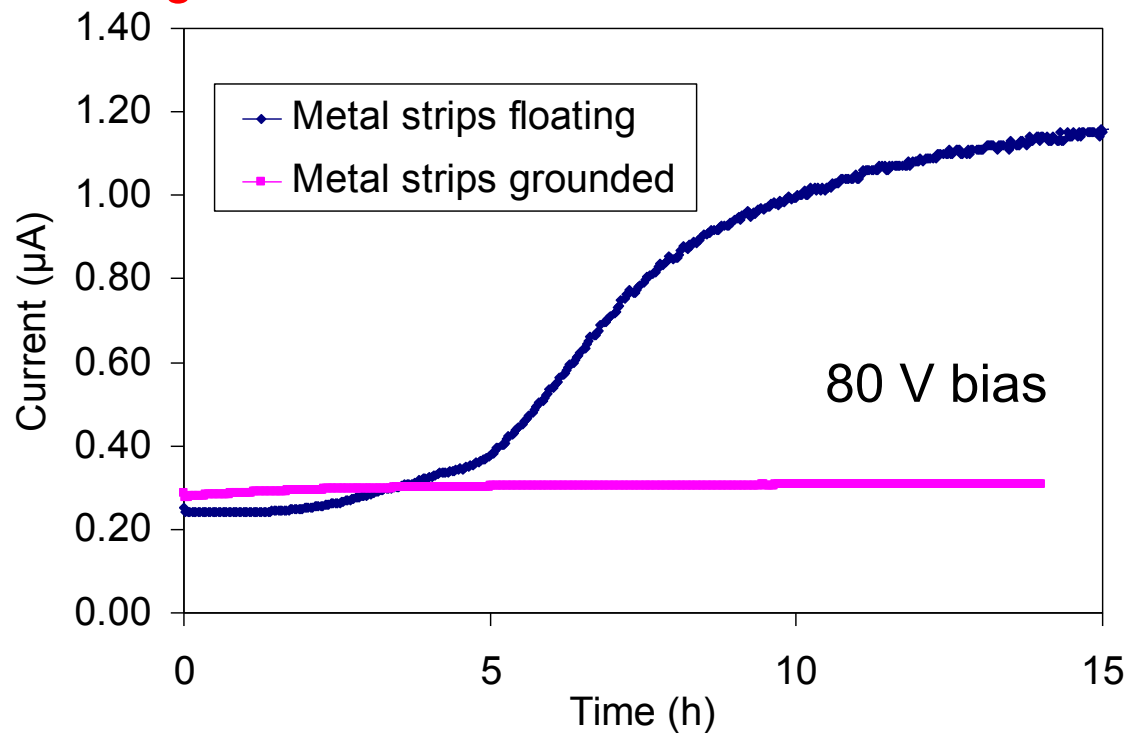


Effects of Surface Potential - 1

On some FBK sensors the current did increase after a few hours under bias, when the **metal strips were left floating**.

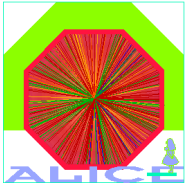
The high current originated from a single *p*-side strip, often showing a small visual defect at the implant edge.

The current was low and stable when the metal strips were grounded.



It has been found that the metal strips tend to charge at slightly positive potential w.r.t. the implanted strips, thus increasing the E field at strip edges. In the presence of defects this can lead to avalanche.

Grounded metal strips are a few V negative w.r.t. the implant (sitting at punch-through voltage) thus decreasing the edge fields.



Effects of Surface Potential - 2

In the long run, ions migrating on the outer surface of the sensor tend to make the surface equipotential with the metal strips. On p -side, this acts as a negative gate w.r.t. the implanted strips.

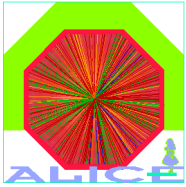
When N_f is high ($2-4 \times 10^{11} \text{ cm}^{-2}$ for FBK sensors, fabricated on (111) wafers), this has the beneficial effect of decreasing the peak electric fields, thus rising the breakdown voltage and decreasing the leakage current.

But when N_f is low ($\approx 10^{10} \text{ cm}^{-2}$ for SINTEF sensors), this negative 'gate' may turn on the parasitic MOSFET between p -strips, thus shorting them together.

A solution is to bias the Bias Ring a few V negative w.r.t. the local ground of the front-end electronics. But it was too late to implement this change in the readout chain!!

In order to gain a margin of safety against this problem, independently of the biasing conditions, Sintef sensors have been pre-irradiated on p -side with low energy X-rays (20 keV, 450 Gy).

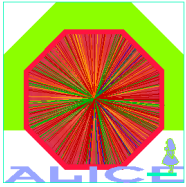




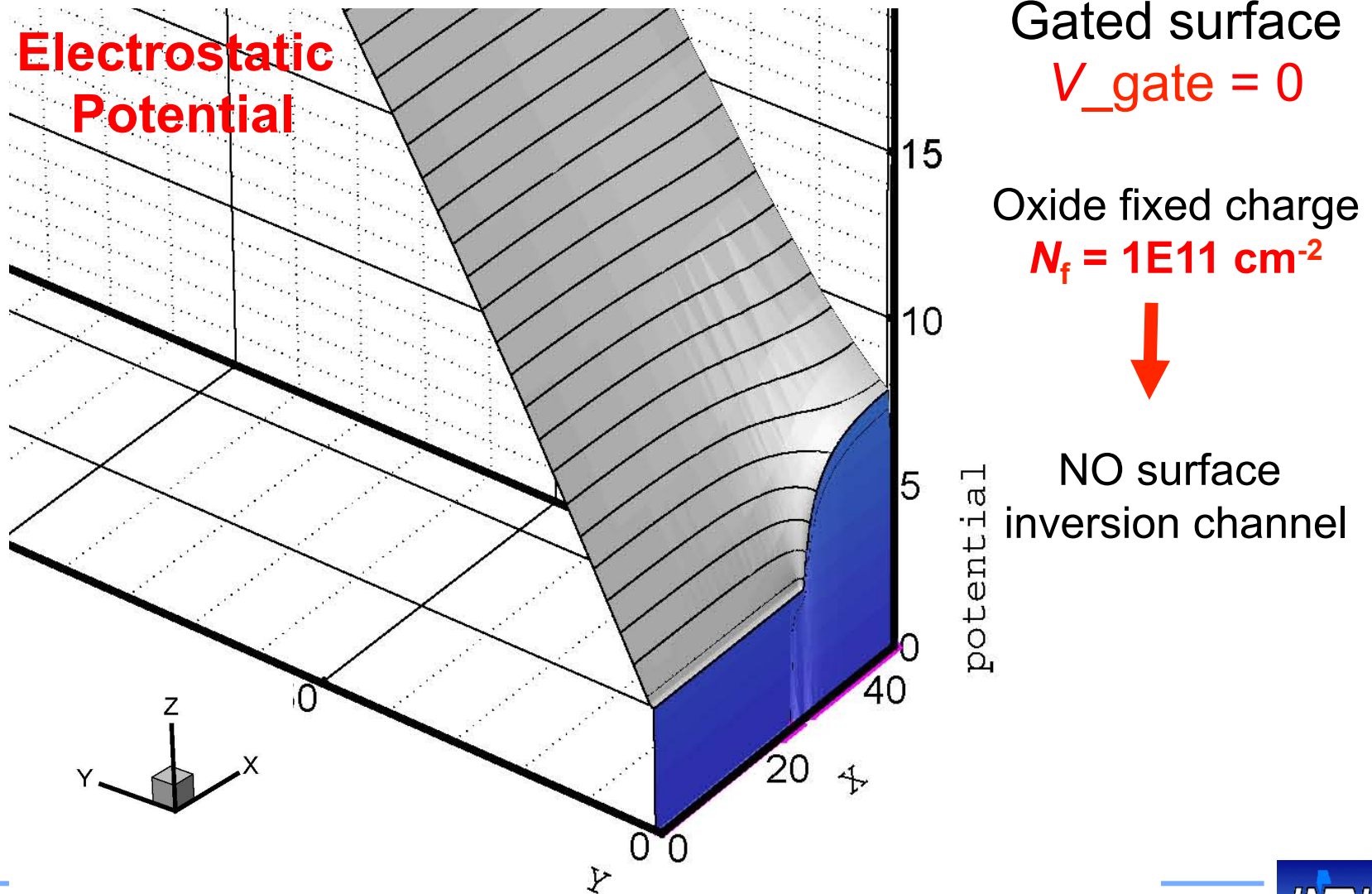
Surface Inversion on SINTEF sensors

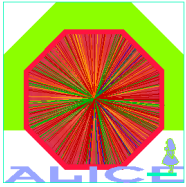
- Low insulation between p -side strips observed after:
 - some time (\sim hour) under bias with AC strips grounded
followed by
 - a few more hours under bias with AC strips floating,
or a long time (several days) of storage without bias
- Interpretation
 - negative ions drift on the surface from the grounded AC pads to the positive interstrip region
 - eventually the interstrip region becomes \sim equipotential with the AC pads, acting as a negative gate w.r.t the positively biased DC strips (sitting at punch-through voltage)
 - this negative gate voltage ($\sim -V_{pt}$), given the very low oxide fixed charge of the SINTEF process, is sufficient to invert the silicon surface, turning on the parasitic MOSFET between the DC strips
however...
- The effect has NOT been seen when AC strips were permanently connected by wire bonding (on a few test sensors)
 \Rightarrow No problem in the real operating conditions ???
The reasons for this behavior are not understood.



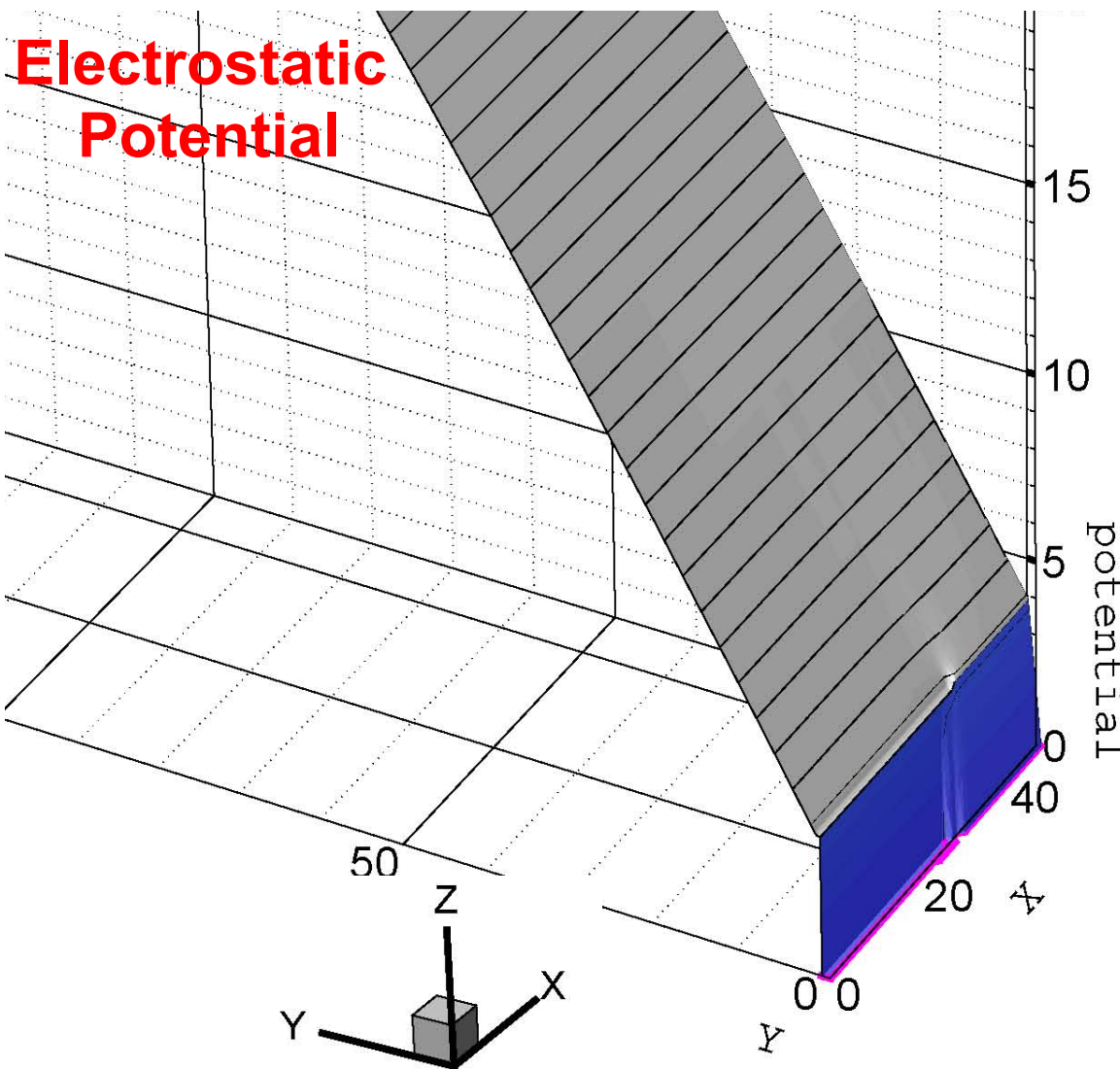


Simulation of interstrip region – High N_f





Simulation of interstrip region – Low N_f

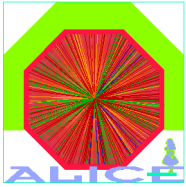


Gated surface
 $V_{\text{gate}} = 0$

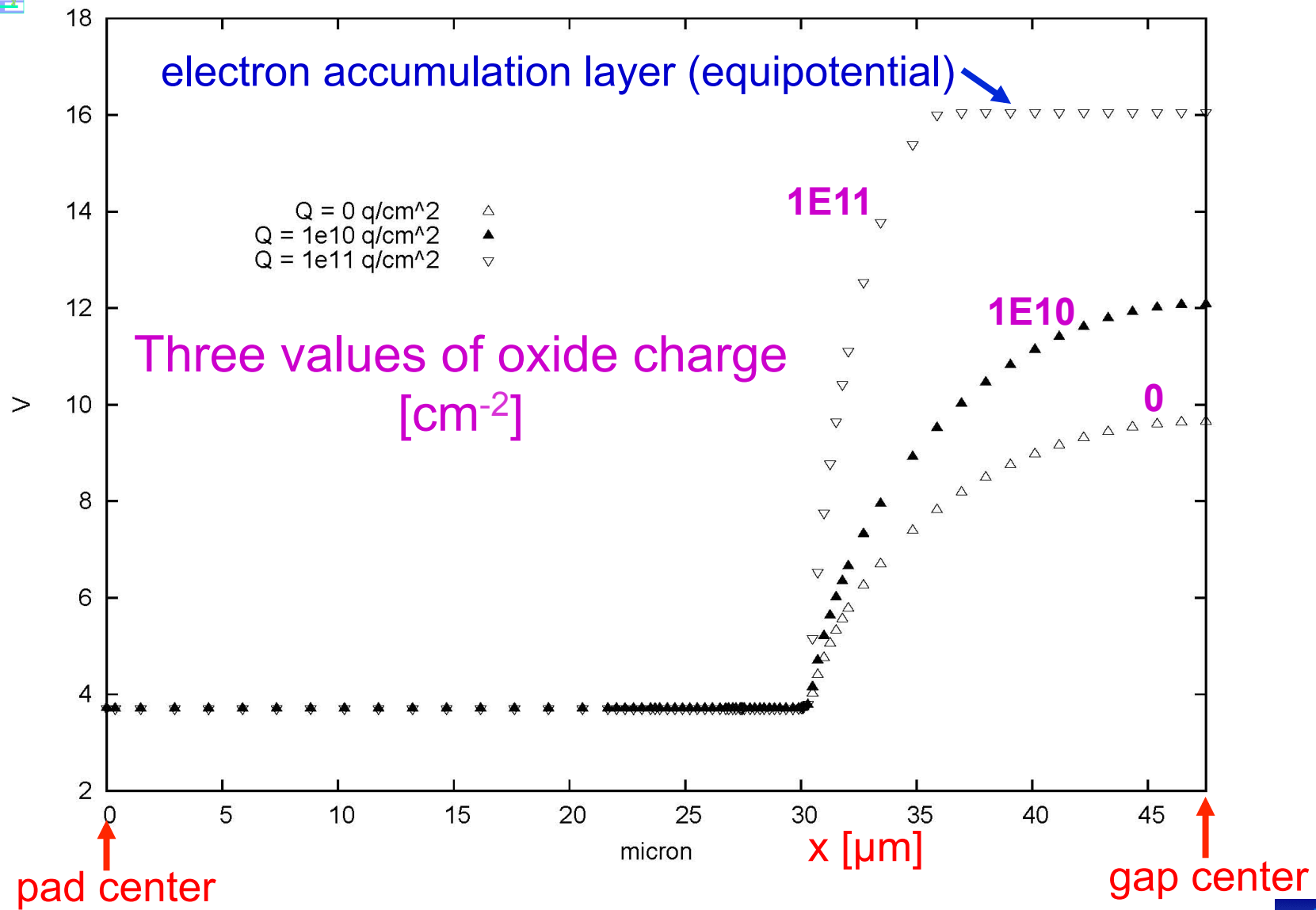
Oxide fixed charge
 $N_f = 1\text{E}10 \text{ cm}^{-2}$

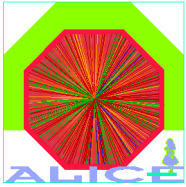


Surface inversion
channel is formed

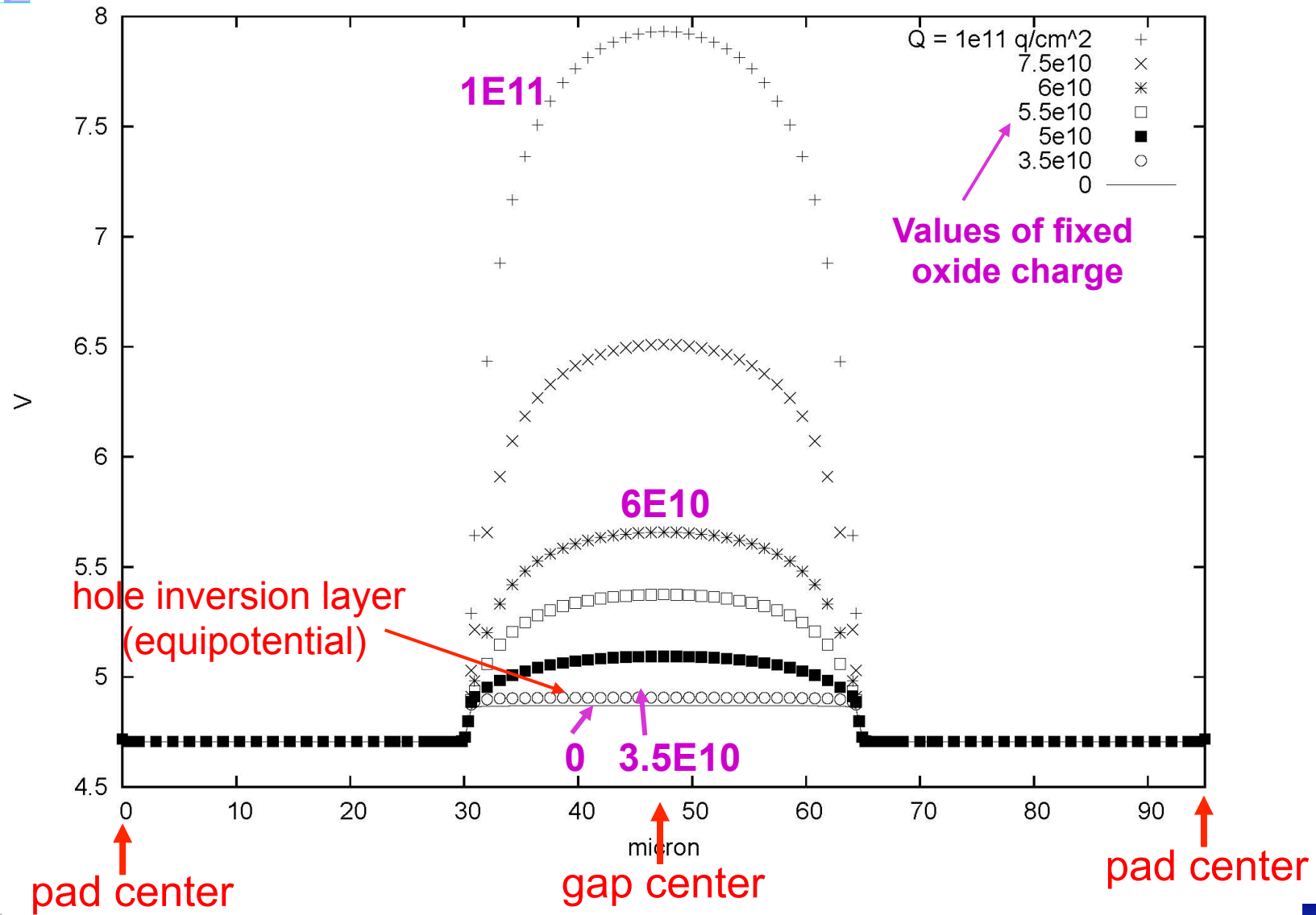


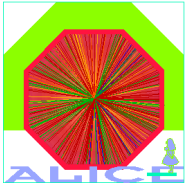
Electrostatic potential along the surface - No Gate



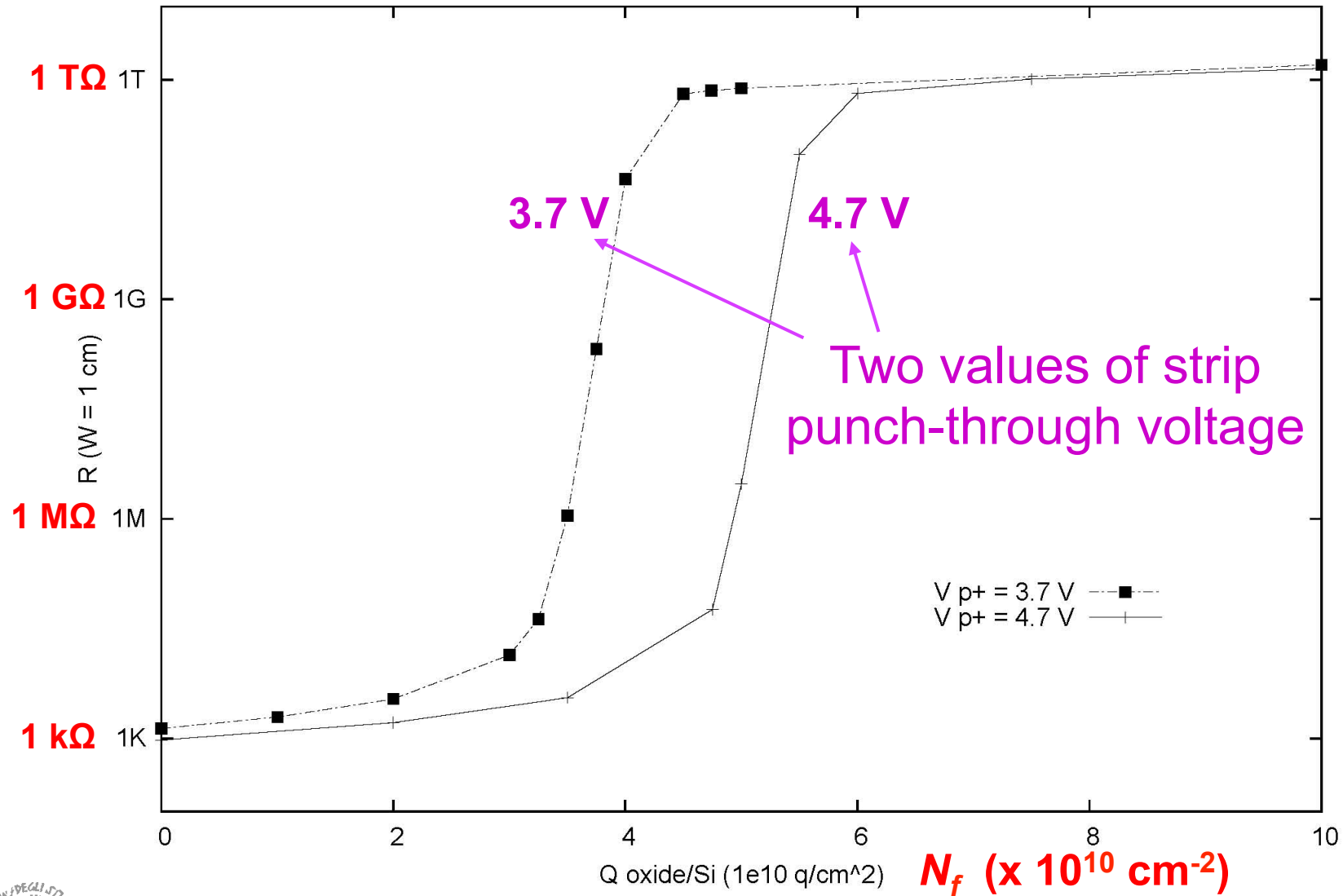


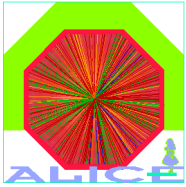
Electrostatic potential along the surface $V_{\text{gate}} = 0$





Interstrip resistance vs. oxide fixed charge $V_{\text{gate}}=0$





Strip Insulation on SINTEF Sensor

Scan of P-side DC pads on non-irradiated test sensor

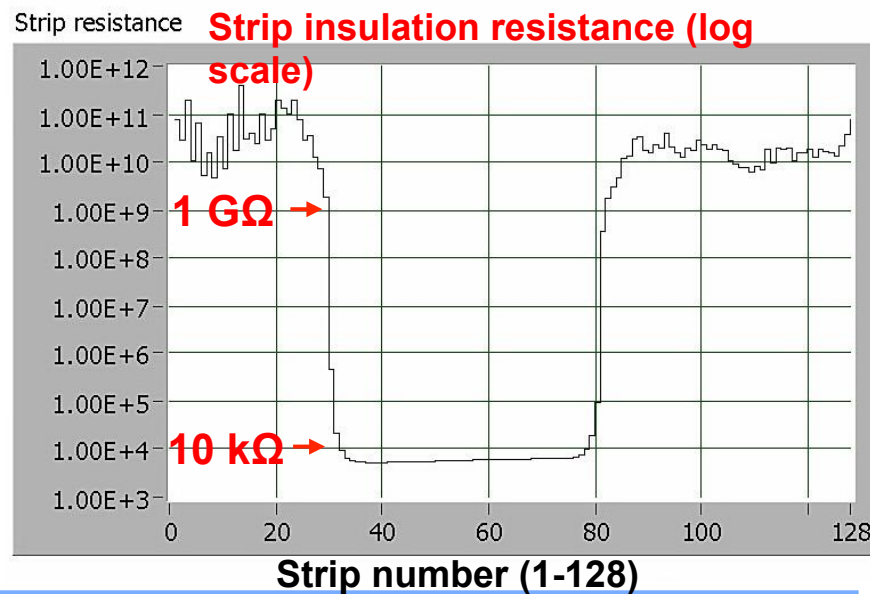
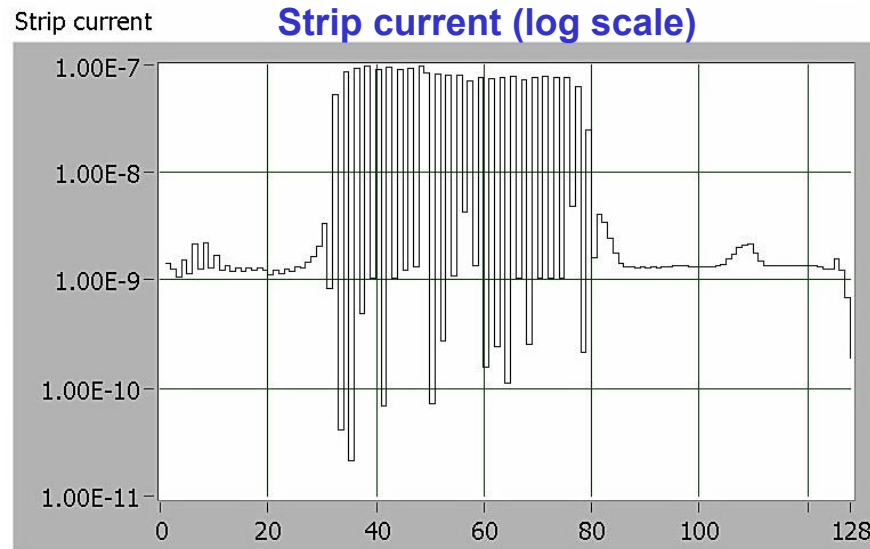
- Metal strips # 31-80 grounded with probe card for ~1 h with sensor under bias

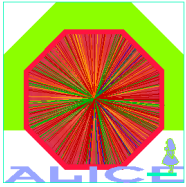
followed by

- 12 h under bias with AC strips floating before making the scan



Low resistance between DC strips #31-80





Strip Insulation on SINTEF Sensor

Scan of P-side DC pads on irradiated test sensor

- Metal strips # 31-80 grounded with probe card for ~1 h with sensor under bias

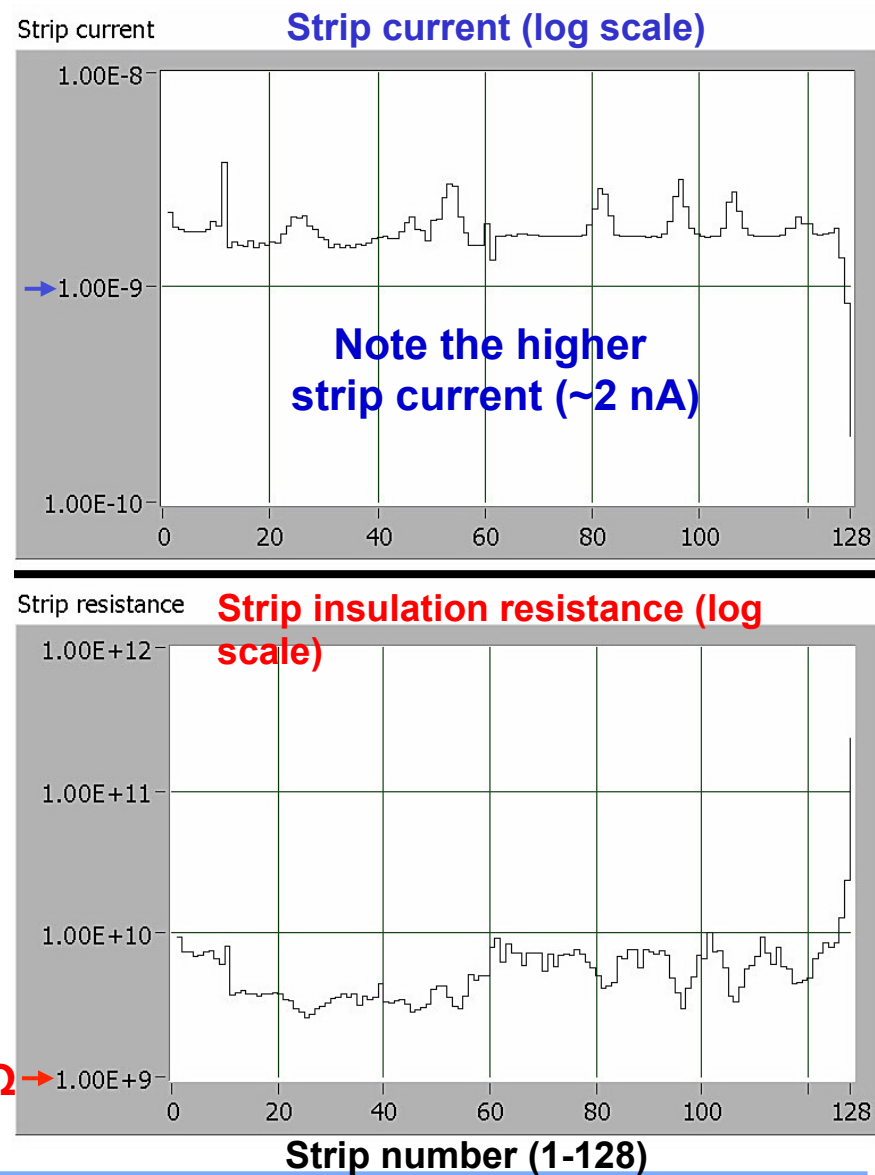
followed by

- 12 h under bias with AC strips floating before making the scan



No low-resistance strips

1 G Ω →

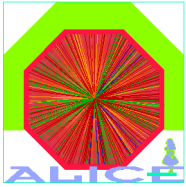


4. Noise Measurements

References:

- G. Giacomini et al.,
“Noise Characterization of Double-Sided Silicon Microstrip Detectors with Punch-Through Biasing”
IEEE Trans. Nucl. Sci. NS-58 (2011) 569-576
- G. Giacomini et al.,
“Study of frequency-dependent strip admittance in silicon microstrip detectors”
Nucl. Instr. and Methods A 624 (2010) 344-349





Noise Measurements

Purpose:

- Investigate the noise contribution of punch-through biasing. Check our understanding of the noise dependence on sensor parameters.
- Compare irradiated with non-irradiated SINTEF sensors, investigating the possible presence of extra noise sources beyond the increased shot noise due to the higher leakage current

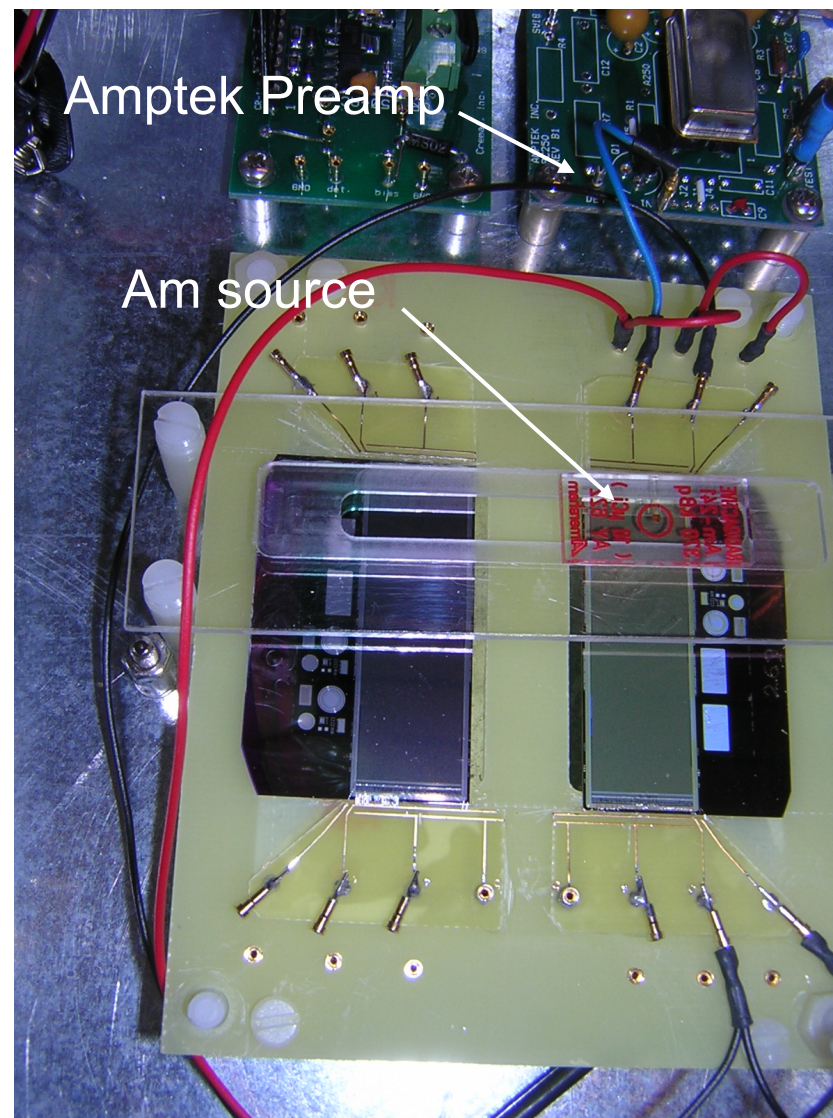
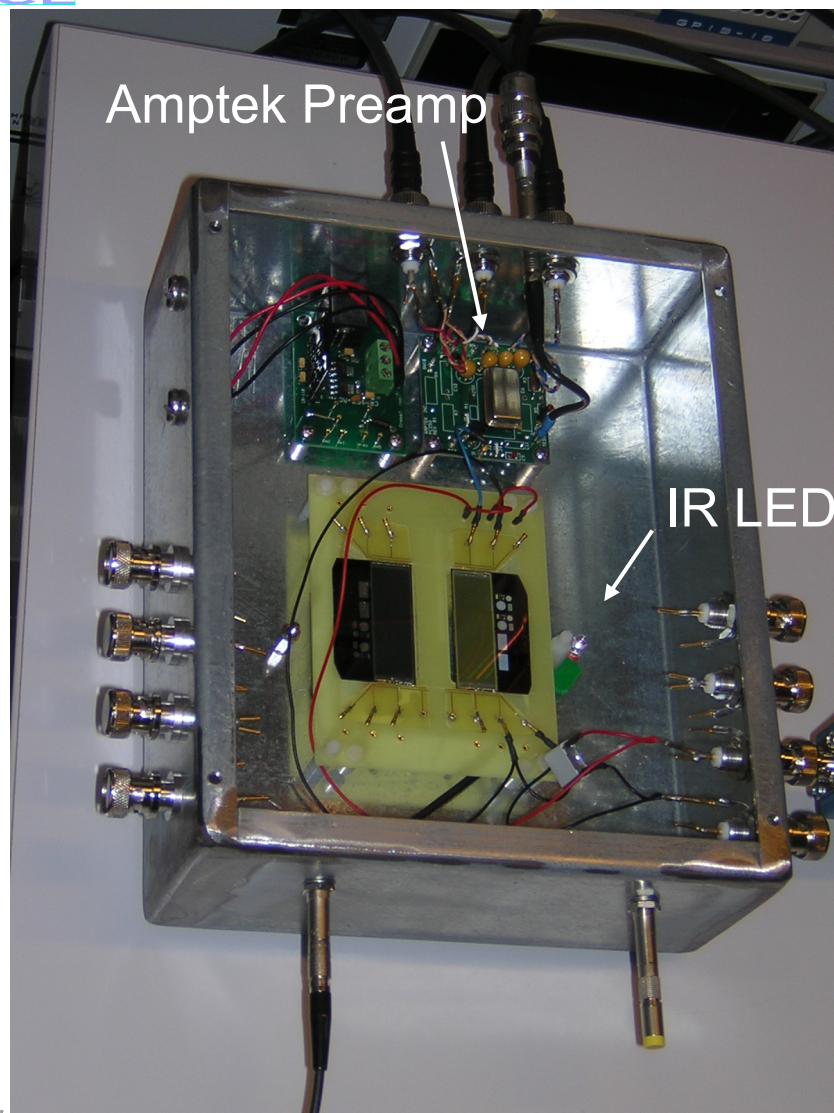
Setup:

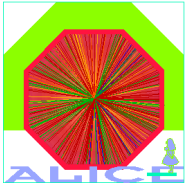
- Test sensors glued and bonded to PCB board
 - AC and DC pads of one strip per side bonded to external terminals
 - all other AC strips bonded to a common bus
- Amptek A250 preamplifier with 2SK152 external input JFET
- Amptek PX4 pulse processor with digital filter
- ^{241}Am 60 keV X-ray source for calibration (~2/3 of a m.i.p.)
- IR LED to increase the leakage current by photogeneration
- Single-channel measurement \Rightarrow no C.M. subtraction possible
 \Rightarrow very sensitive to pick-up \Rightarrow good shielding and filtering needed





Noise Measurements: Setup





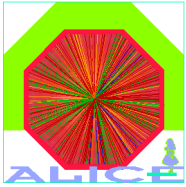
Noise Measurements

- For both p -side and n -side strips, the ENC was measured versus
 - *peaking time* of triangular shaper ($\tau_p = 0.8 - 26 \mu s$)
 - *leakage current* (in the dark and photogenerated)

Note: *Equivalent Gaussian shaping time* $\approx \frac{1}{2} \tau_p$

- Several variants explored, including:
 - strip biasing by a high value external resistor vs. punch-through bias
 - injecting current through the DC pad vs. photogeneration by an IR LED
 - taking the signal from the DC pad





Noise Contribution of Punch-Through Biasing

- Punch-through current = carriers emitted over a potential barrier
⇒ affected by Poisson fluctuations ⇒ shot noise contribution
- If fluctuations in I_{PT} and in I_{Leak} are uncorrelated, the two shot noise contributions add in quadrature
- We then expect, for triangular shaping with peaking time τ :

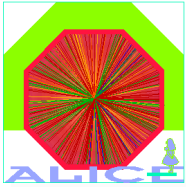
$$q^2 ENC^2 = \frac{\tau}{3} \left(2qI_L + 2qI_{PT} + \frac{4kT}{R_f} \right) + \frac{C^2}{\tau} 4kT \left(\frac{2}{3g_m} + R_S \right) + C^2 A_f \quad (1)$$

where:

- C = total capacitance at amplifier input
- R_S = sum of the series resistances
- R_f = feedback resistance of amplifier
- g_m = transconductance of the input JFET
- A_f = series flicker ($1/f$) noise coefficient

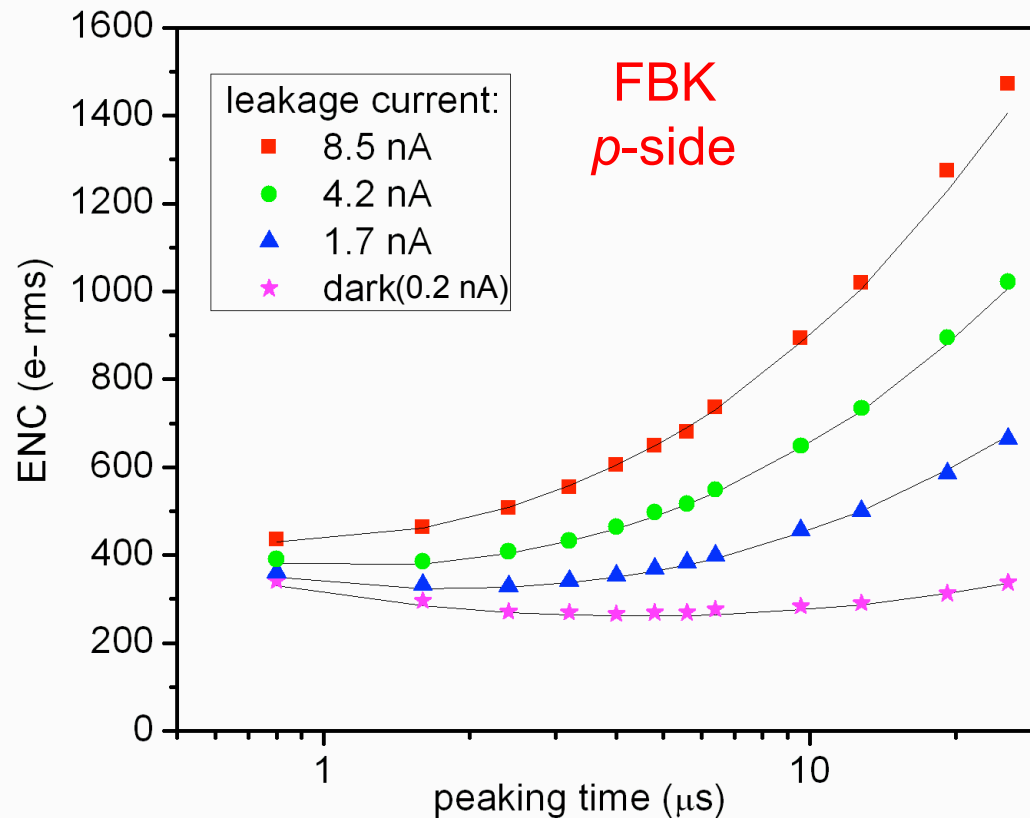
In normal situations $I_{PT} = I_L$ and we get a leakage current contribution $\tau/3(4qI_L)$ to the (squared) noise, instead of just $\tau/3(2qI_L)$





FBK sensor *p*-side

Noise vs. peaking time and leakage current



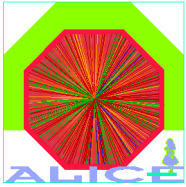
Continuous lines: calculated from Eq.(1)

- Leakage current varied by photogeneration
- The measured noise agrees well with the prediction of Eq.(1), with:

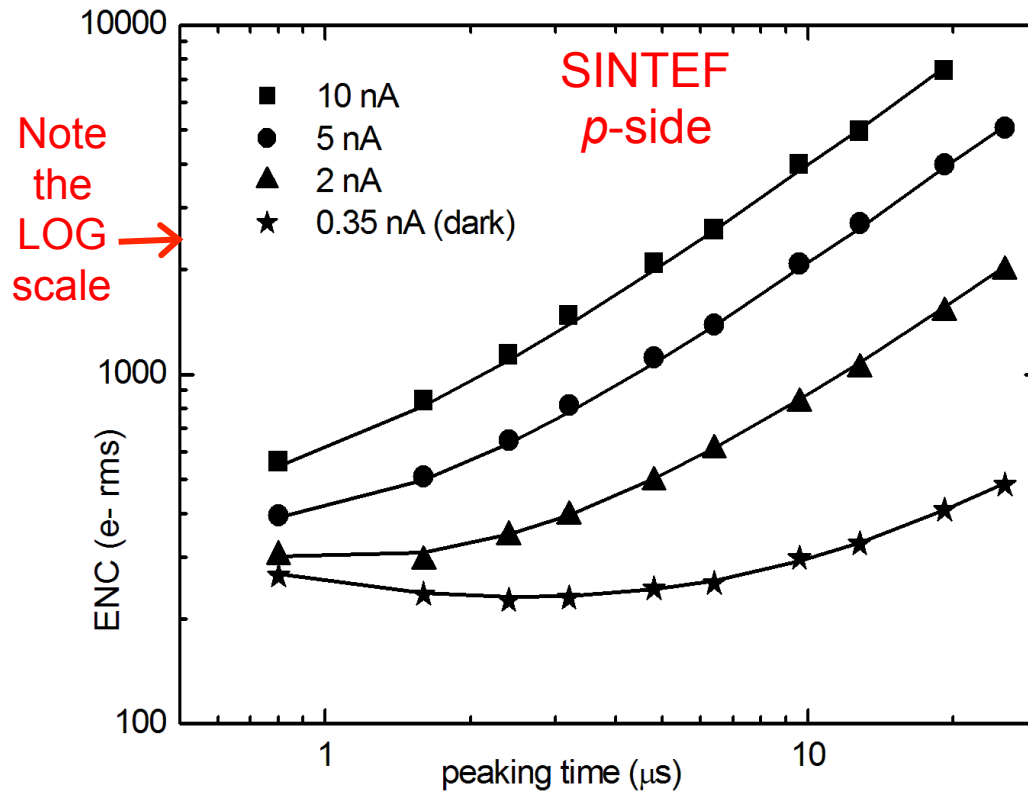
- g_m, R_f, C_{det} determined by direct static measurements
- C_{input}, R_S, A_f evaluated from noise measurements with open amplifier input



- The noise contribution of punch-through is as expected



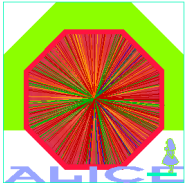
Excess Noise on p -side of SINTEF Sensor



Continuous lines: calculated from Eq.(1) with the extra noise term (2), where the value of A is defined by fitting the data

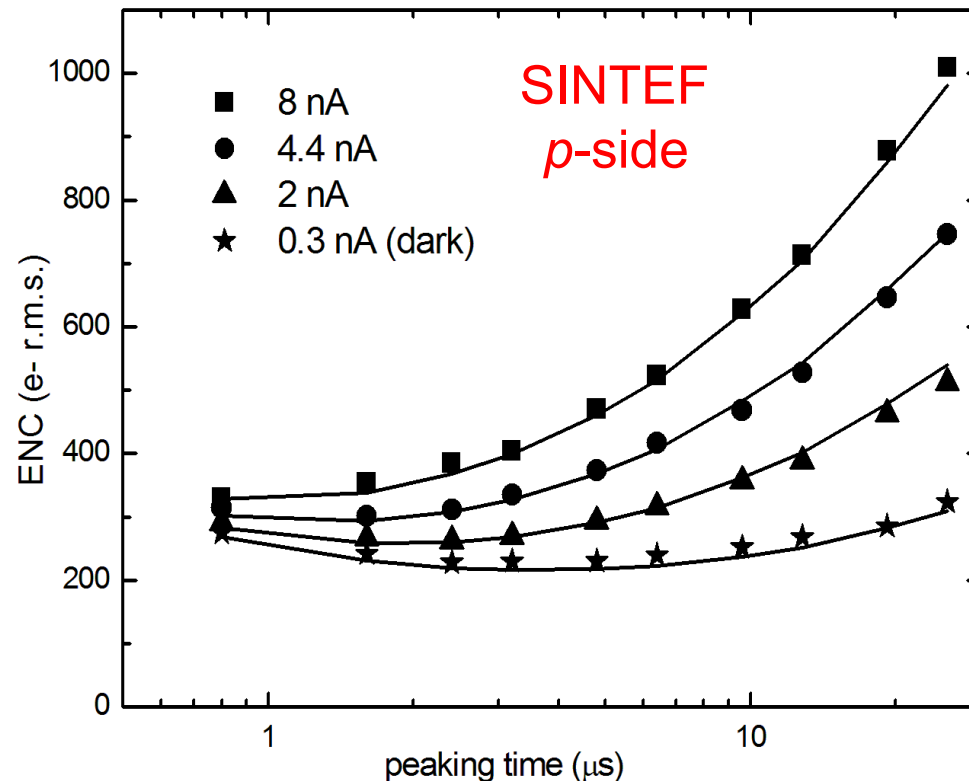
- Photogenerated current
- At high τ and/or I_L values, noise is
 - much higher than expected
 - directly proportional to both τ and I_L
- There is an excess noise term

$$q^2 ENC^2 = A \tau^2 I_{PT}^2 \quad (2)$$
 added in quadrature (A = dimensionless constant)
- Spectral power density of this current noise is $\propto 1/f$: ‘parallel flicker noise’



SINTEF sensor *p*-side

Noise when the P-T current is suppressed

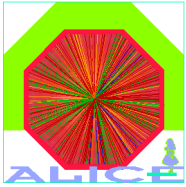


- Photogenerated current
- Strip polarized through an external resistor (470 MΩ) connected to the DC pad
- ⇒ NO Punch-Through current
- ⇒ NO extra noise term
- Confirms that the extra noise is due to the punch-through current

Continuous lines: calculated from Eq.(1)

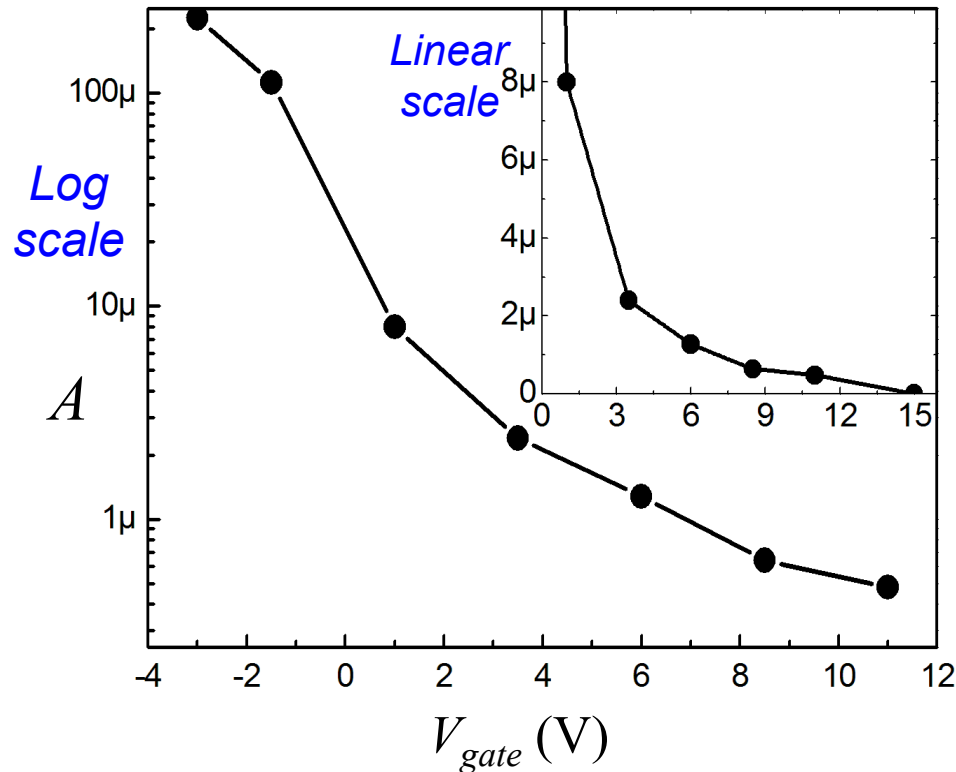
with the added thermal noise of the bias resistor: $q^2 ENC^2 = \frac{\tau}{3} \left(\frac{4kT}{R_{bias}} \right)$





SINTEF sensor *p*-side

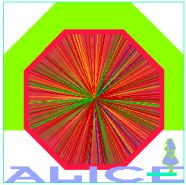
Effect of gate over the Punch-Through region



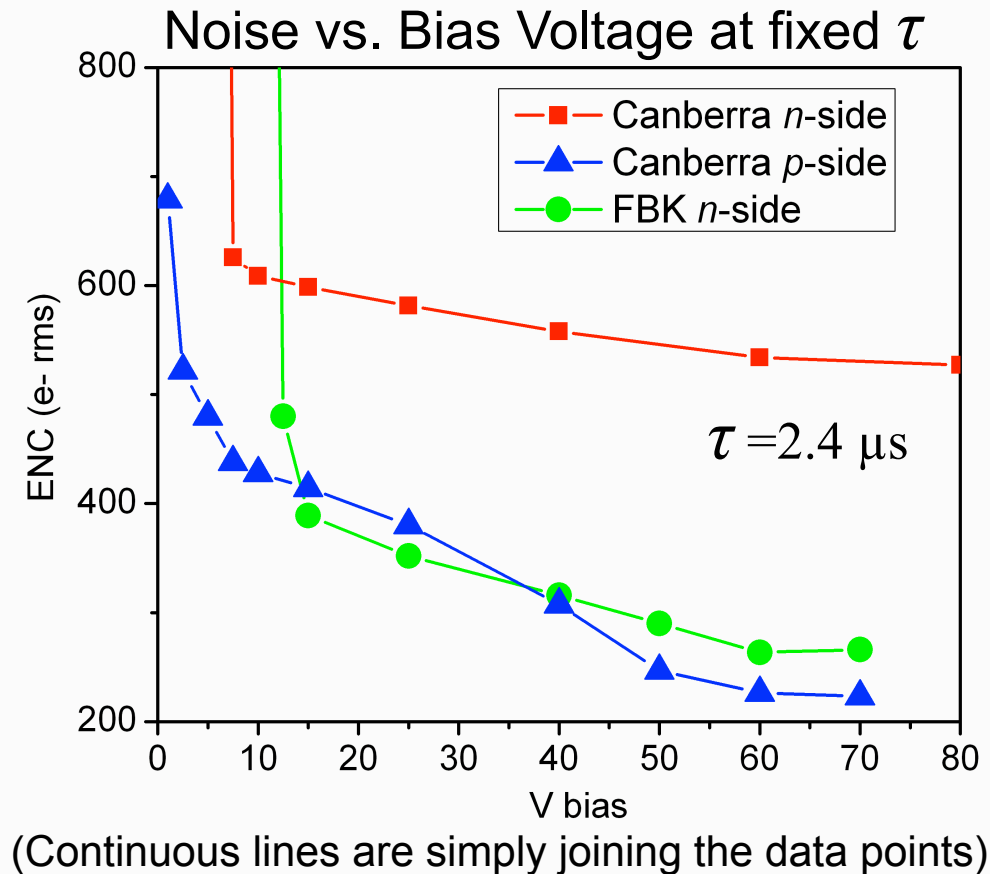
- SINTEF sensors have a (floating) metal gate above the P-T region
- Noise measured versus voltage applied to gate
- Excess noise (Eq.(2)) extracted and dimensionless constant A plotted vs. gate voltage
- Negative V_{gate} suppresses the excess noise, positive V_{gate} enhances it

- Interpretation: Due to the low oxide fixed charge of Sintef sensors, the P-T hole current runs close to surface, where it is affected by $1/f$ noise due to interface traps (as for the channel current in a MOSFET).
- Positive V_{gate} pushes the P-T hole current away from the surface, suppressing the excess noise.

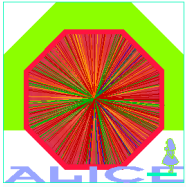




Further Excess Noise Contribution

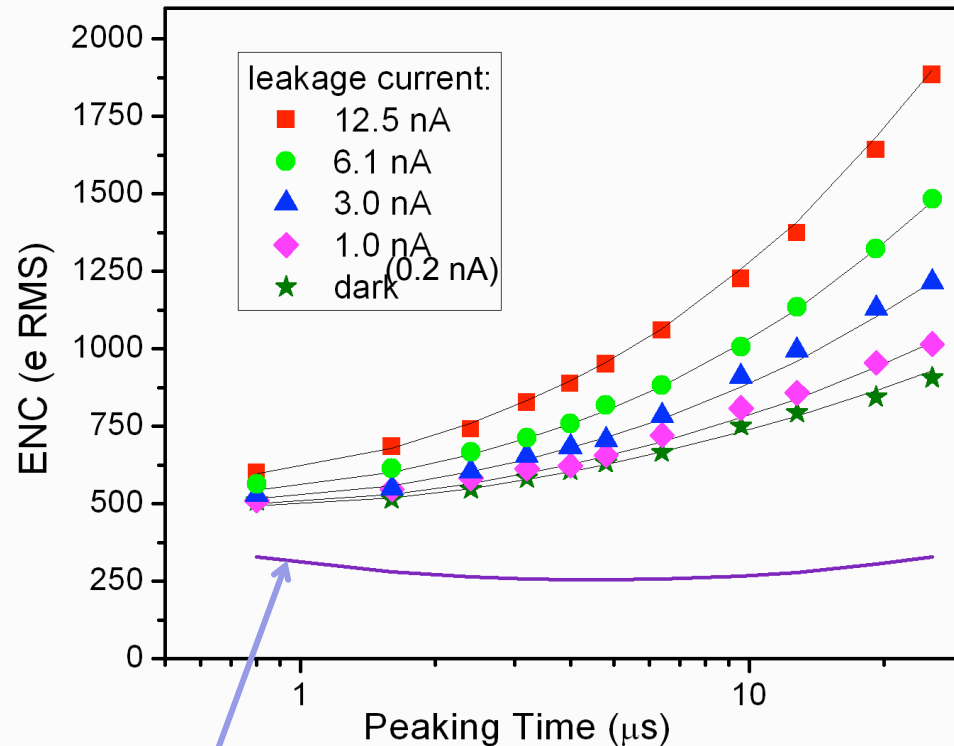


- On **Canberra *n*-side** the noise decreases slowly with bias above total depletion (~ 8 V), but is ~ 2 X higher than expected
- **Canberra *p*-side** and **FBK *n*-side** (total depletion ~ 15 V) show an excess noise between depletion and ~ 60 V.
- The **dependence** of this noise on **peaking time** has been found to be **rather odd**: $q^2 ENC^2 = K\sqrt{\tau}$
where $K \approx 10^{-30} \text{ C}^2 \text{ Hz}^{1/2}$, independent of the current



Noise due to Resistive Layers at the Interface

Canberra *n*-side 80 V bias



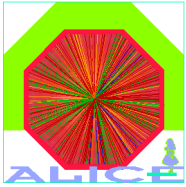
0.2 nA , calculated from the model,
without excess noise

⇒ The excess noise is dominant over other
noise sources

- Comparison with measurements of strip capacitance and dissipation factor vs. frequency and bias voltage suggest that this noise term may be due to continuous resistive layers at the interface, extending over the whole sensor:

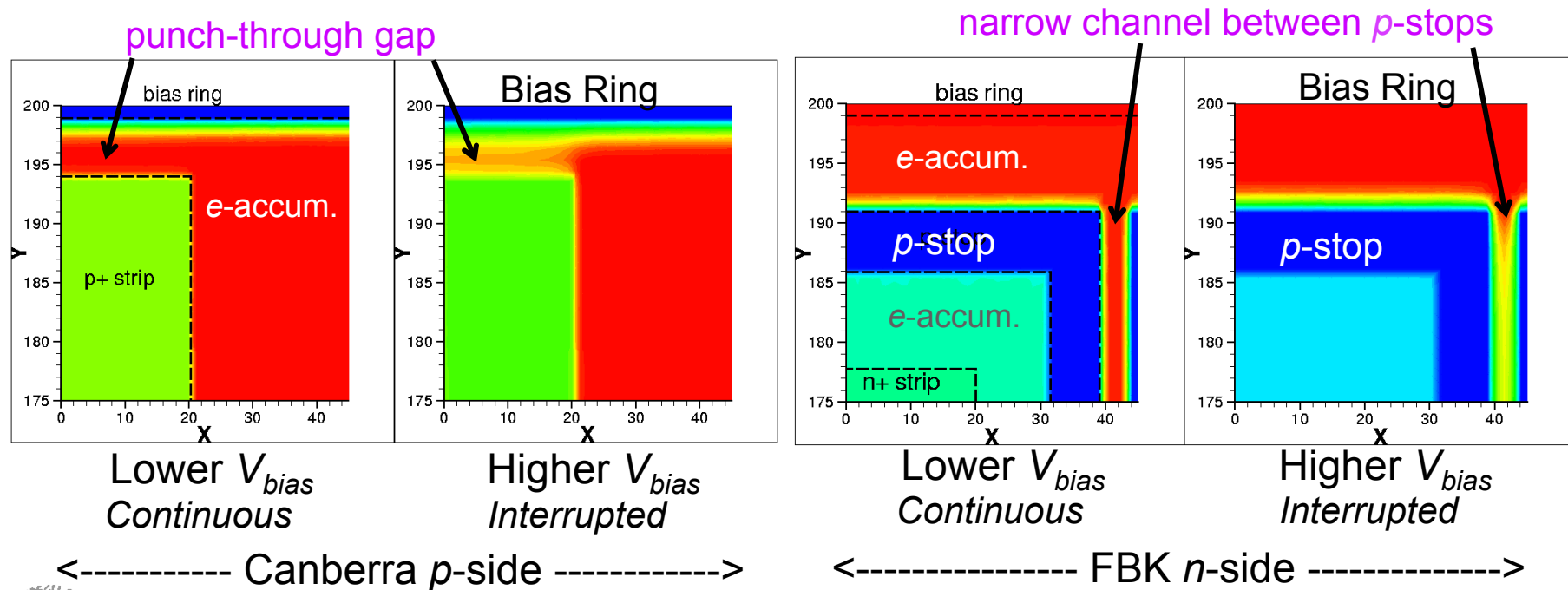
- electron accumulation layer on *p*-sides and on FBK *n*-side
- *p*-spray on Canberra *n*-side

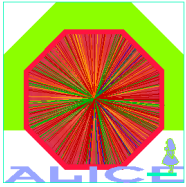
- But it's not just thermal noise capacitively coupled to the strip (different τ dependence)



Noise due to Resistive Layers at the Interface

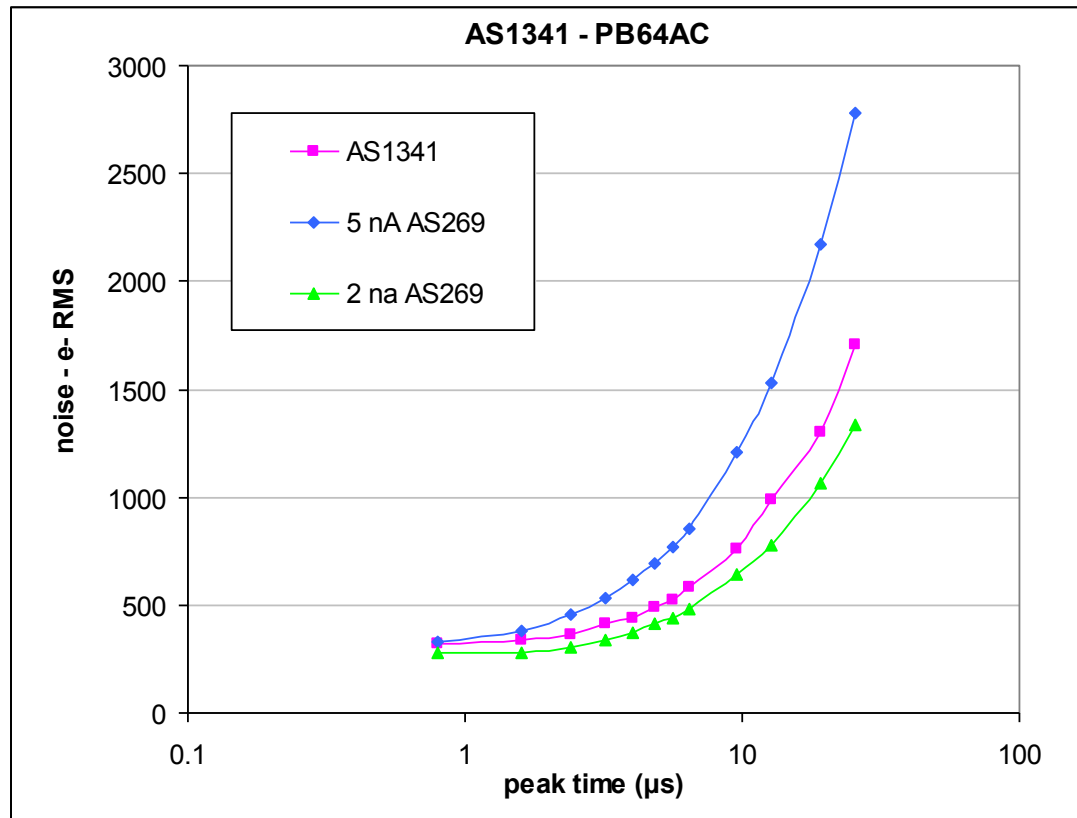
- The suppression of this noise at high bias voltage could be related to the interruption of the electron accumulation layer
 - in the punch-through gap on p -side
 - in the region between p -stops close to strip ends on n -side
- 3-D numerical simulation of electrostatic potential at the interface, (floor view of a small region at strip end)



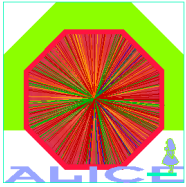


X-ray Irradiated Sintef Sensor: *p*-side strips

Comparison between irradiated (AS1341) and non-irradiated (AS269) sensors, for comparable values of leakage current

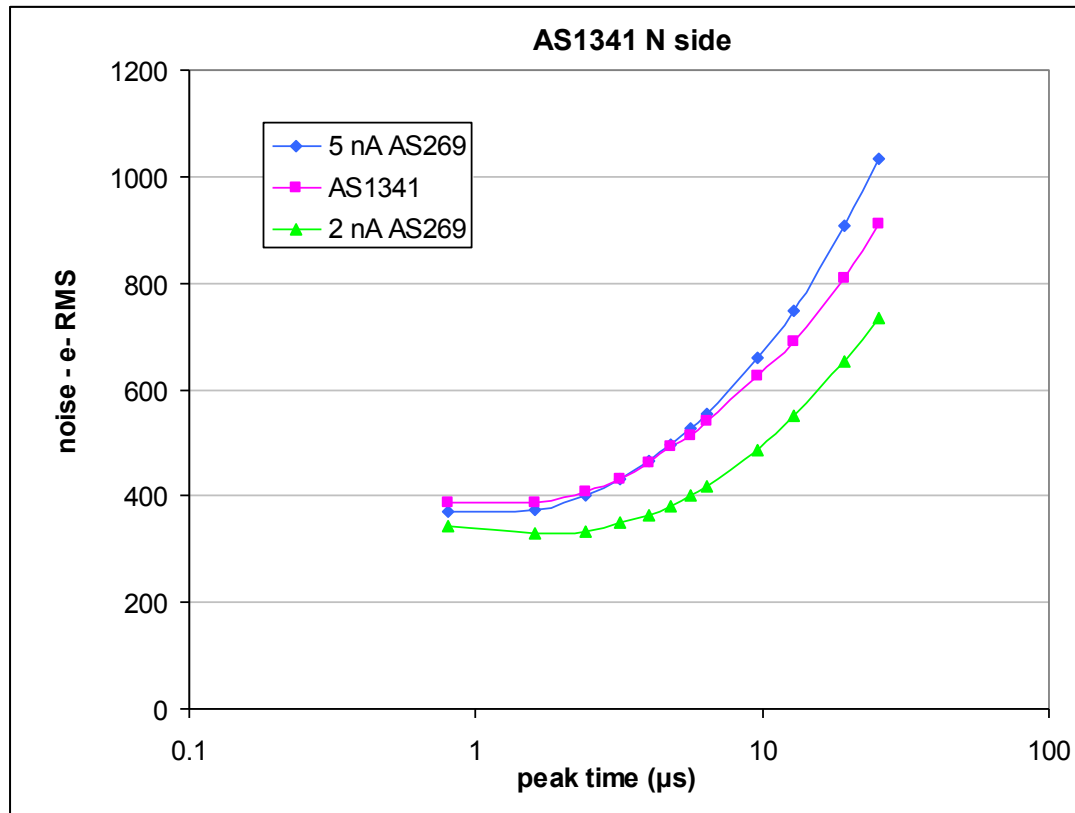


- Noise of irradiated sensor is compatible with its higher leakage current (given the observed contribution of punch-through current)
- No further contribution to noise was found
- ENC < 400 e r.m.s. at shaping times of 1-2 μs

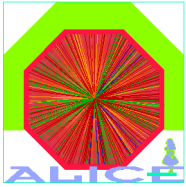


X-ray Irradiated Sintef Sensor: n -side strips

Comparison between irradiated (AS1341) and non-irradiated (AS269) sensors, for comparable values of leakage current



- Noise of irradiated sensor is roughly compatible with its higher leakage current (a few nA)
- ENC is still < 400 r.m.s. at shaping times of 1-2 μ s



Summary of Noise Measurements

- Punch-through biasing contributes by adding in quadrature a further shot noise contribution, i.e. doubling the shot noise contribution to ENC^2



Carrier injection by punch-through from strip to BR undergoes Poisson fluctuations, and these fluctuations are uncorrelated to the fluctuations in carrier generation and collection by the strip.

- On SINTEF sensors, the punch-through mechanism on p-side contributes extra noise, directly proportional to punch-through current and to shaping time. This 'parallel flicker noise' is attributed to the current flowing very close to the interface, where it is affected by interface traps.
- The X-ray irradiation does not appear to add additional noise beyond what expected given the increased current.
- At 2 μs shaping time the noise is well acceptable in all cases ($ENC < 500 e$).

