

# Integration and System Qualification of the ALICE Silicon Pixel Detector



R. Santoro

On behalf of the SPD collaboration in the ALICE experiment at LHC

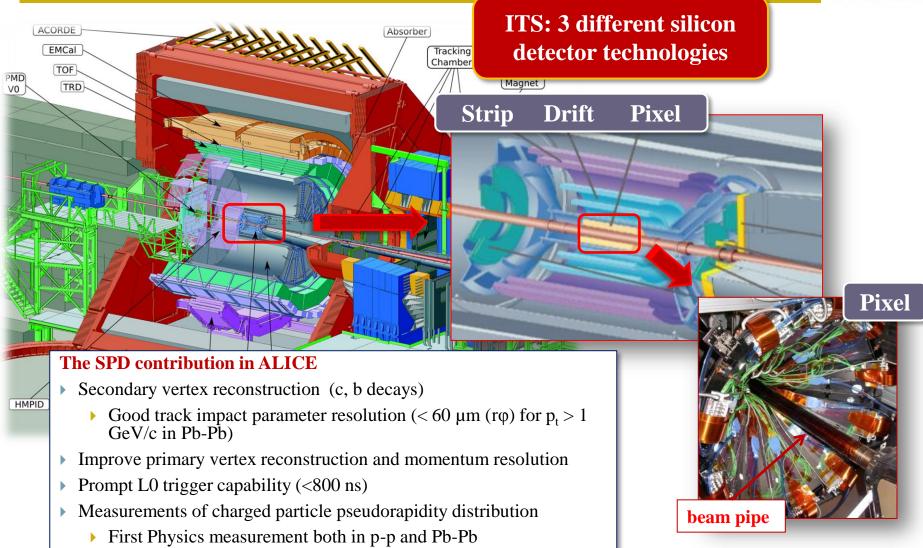
#### Outlook



- Silicon Pixel Detector in the ALICE experiment
- Mechanical accuracy
- Pre-commissioning
- Installation
- Optical link synchronization
- Monitor and debug tools

## SPD in the ALICE experiment







Mechanical accuracy



## Basic module assembly: Half-stave



#### Components

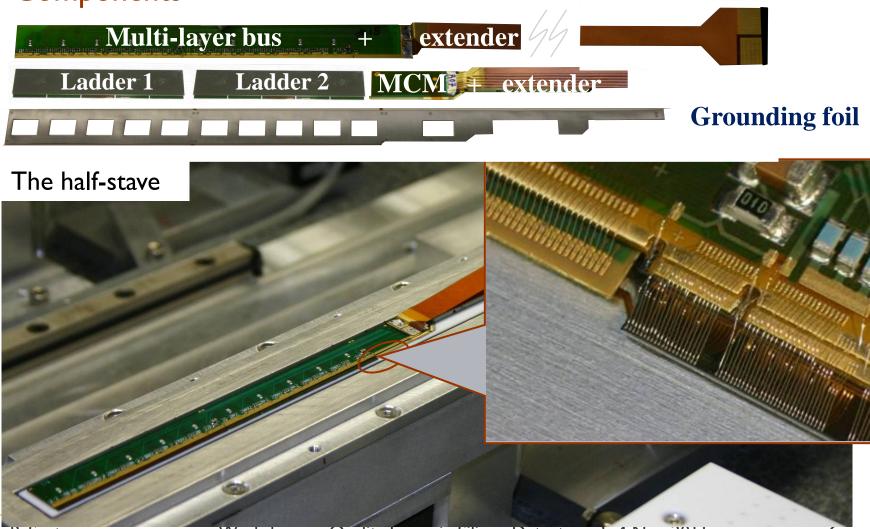


- Grounding foil: aluminum-polyimide foil (25 + 50 µm thick) with 11 windows to improve the thermal coupling between the backside of the FE chips and the cooling tube
- ▶ 2 hybrid pixel modules: ladders
  - A p+n silicon sensor matrix 200 μm thick with 40960 pixels arranged in 256 rows and 160 columns
  - > 5 FE chips Flip-chip bonded to the sensor through Sn-Pb bumps
  - The pixel cell has the dimensions of 50  $\mu$ m (r $\phi$ ) x 425  $\mu$ m (z)
- MCM: Multi Chip Module to configure and read-out the half-stave
- ▶ Pixel Bus: aluminum-polyimide multi-layer bus to connect the MCM and FE chip
  - More than 1,000 wire bonding for each half-stave

## Basic module assembly: Half-stave





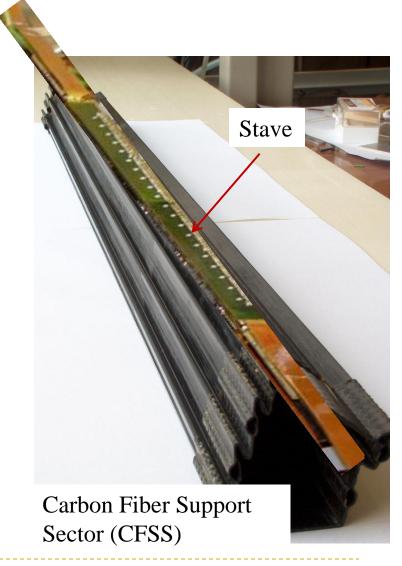


#### Sector



- ▶ 2 half-staves are coupled to form a stave
  - The sensitive area is in the center, while the services at the 2 edges
- The staves are mounted onto the low-mass carbon fiber support (sector) in the upper and bottom part to form the 2 layer-structure



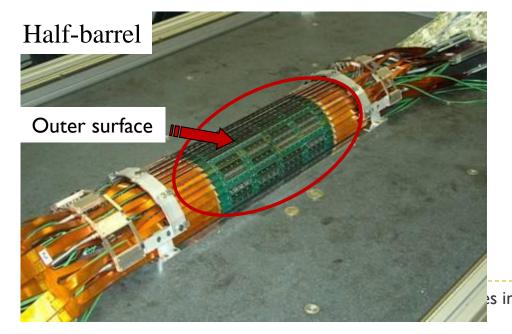


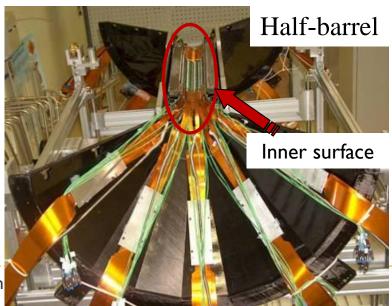
#### Half - barrels



- > 5 sectors are joint one close to the other to form the half-barrel
- The 2 half-barrels are mounted face-to-face around the beam-pipe







#### Mechanical accuracy



- The ladders positioning in the half-stave has the accuracy of the order of few microns
- The stave positioning onto the sector has the accuracy of the order of tenths of microns
- The sectors were joint one close to the other in the half-barrel with the accuracy of the order of hundred microns
- ▶ The SPD positioning around the beam pipe is of the order of few hundred of microns
- No survey was done at the end

#### Is this enough for the physics?

- Alignment:
  - The survey measurement is an important input for the alignment algorithm
  - Although, using the estimated mechanical accuracy as input, we aligned the detector within the expectation
- Simulation:
  - The description and the alignment of the passive components has to be very accurate. The transport code is unpredictable if you superimpose two materials in the same region
  - We experienced this problem which still has to be solved
    - Temporary solution adopted in ALICE: simulate collision with a perfectly aligned geometry and reconstruct the events with the residual misalignment geometry



System pre-commissioning

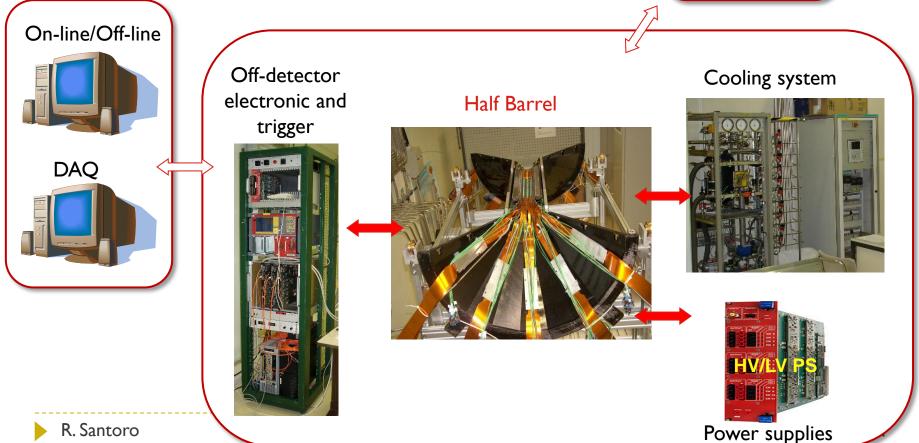


## Pre-commissioning (I)



Test performed using the final readout chain, power supplies, DCS system, cooling system, cables, interlock ...





## Pre-commissioning (II)



## This is the first opportunity to commissioning the full system

- It is a crucial task:
  - You have to run the system by remote as in the experiment
  - You have to be sure that all the safety procedures (i.e. interlock) behave properly
  - The system has to be characterized and the informations stored in the construction DB
  - Everybody in the collaboration wants prompt feedback!!!

# Off-detector electronic and trigger Half Barrel Power supplies

#### ... but it is still better than the experiment because you have access to the hardware

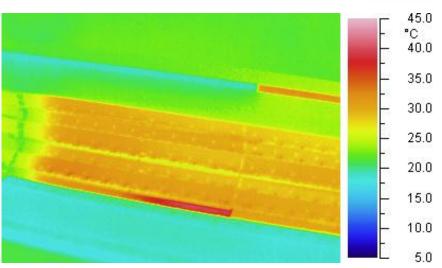
- ... and this is extremely useful to:
  - Debug the software and the integration
  - Tune the monitoring and archival tools (voltages, current and temperature measurements)
  - Fix the number convention (i.e. software-hardware module correspondence)
  - ... and in case of small accident ... there is still something that can be done!!!



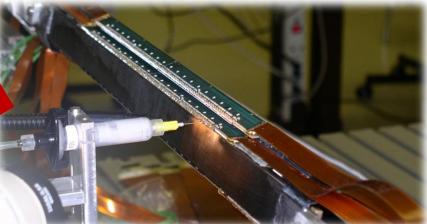
#### ... one example



- We measured a poor thermal contact which caused higher temperature in one half-stave ...
- We decided to operate surgically the stave instead of rework the full sector









Mechanical integration



## Integration in the Department Silicon Facility













#### The travel inside the heart of ALICE



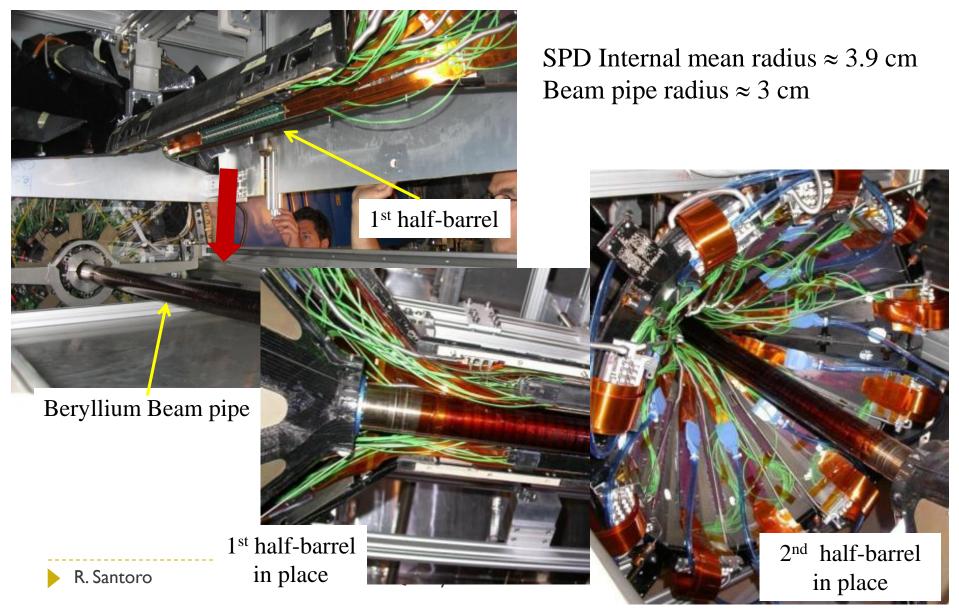






## Installation: ...for the press (I)

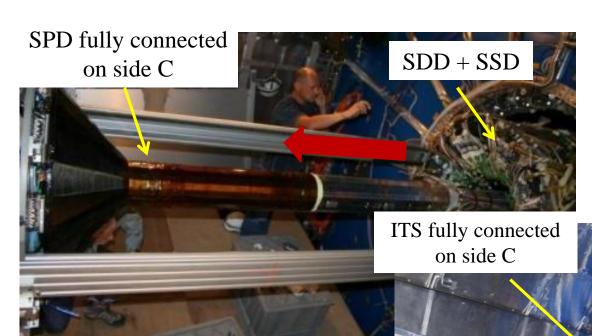




#### Installation: ...for the press (II)



**TPC** 

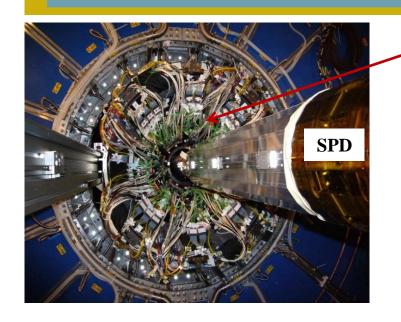


SDD+SSD moved over the SPD to form the ITS

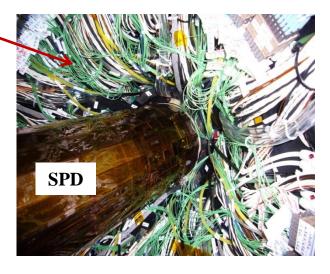
TPC moved over the ITS

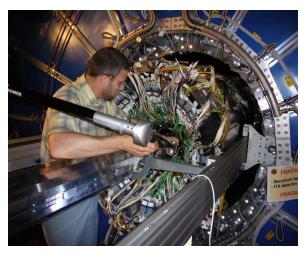
## Installation: ...what really happened



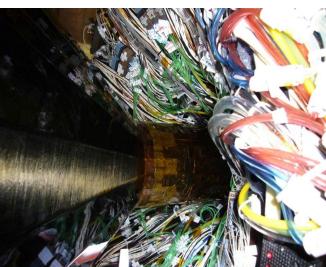


SDD + SSD services







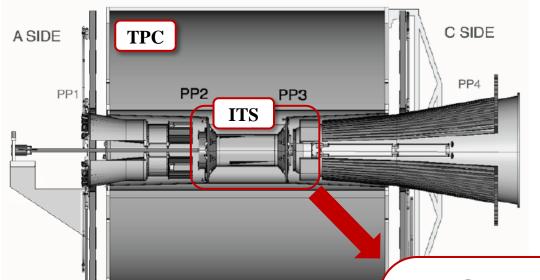


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Workshop on Quality Issues in Silicon Det

#### ITS + TPC: section view

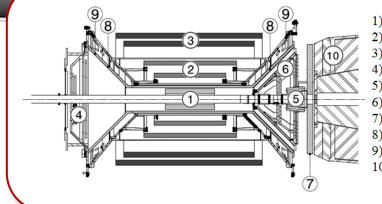




Once the TPC is moved in the final position, there is no more access to the ITS and to the Forward detectors. In addition, two of the 4 patch panels (PP2 and PP3) used for services connections are not accessible anymore

Any access to the detectors or to the services needs a very long and risky procedure:

The time estimate to access the ITS has been recently estimated to be of the order of 7 months



- 1) SPD
- 2) SDD
- 3) SSD
- 4) FMD-2
- 5) T0
- 6) FMD-3
- 7) V0
- 8) SPD services cones
- 9) SDD + SSD services cones
- 10) Front Absorber

#### What we experienced?



#### Mechanical integration

- In such a complex and extremely packed detector the good communication between teams or, even better, to have a unique team for the integration could help during the installation
- Integration tests are also preferable although are not always easy
- Services: better accessibility has to be a must
  - See SPD cooling experience (Rosario Turrisi)
  - Cabling failure (1/120 HS in the SPD)



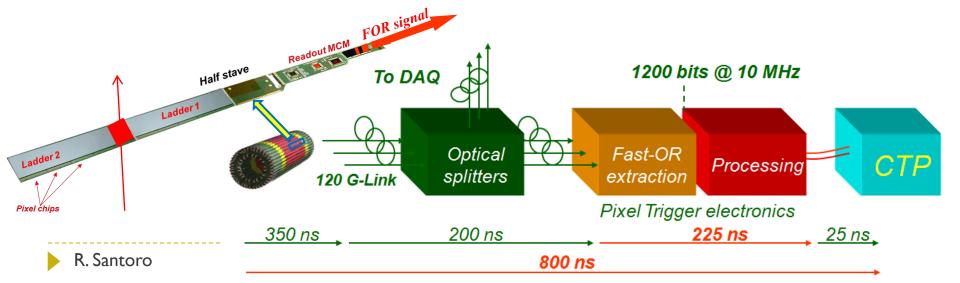
Optical link synchronization



## L0 trigger capability

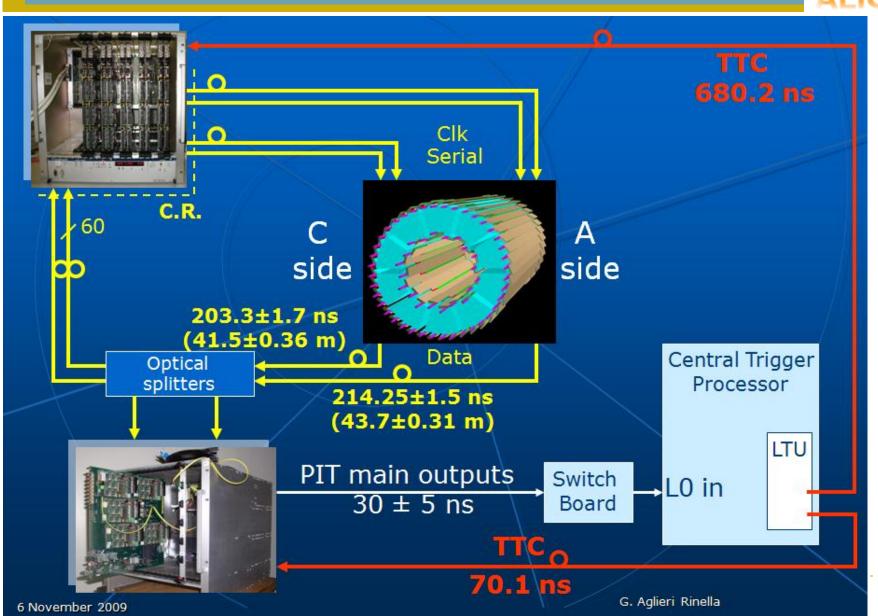


- Pixel chip prompt Fast-OR
  - Active if at least one pixel hit in the chip matrix
  - ▶ 10 signals in each half-stave (1200 signals in total)
  - Transmitted every 100 ns
- Overall latency constrain 800 ns (CTP)
- Key timing processes are data deserialization and Fast-OR extraction
  - ▶ Algorithm processing time < 25 ns
- ▶ 10 Algorithms provided in parallel: useful for detectors commissioning, p-p and Pb-Pb physic
  - Cosmic, minimum bias and multiplicity algorithms
- FPGA remote programmable to guarantee maximum flexibility



## Electronic layout



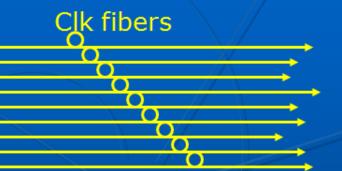


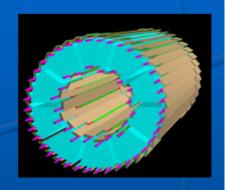
## Detector clock phases alignment











Clk outputs

Relative phases of 120 clocks of CR electronics:  $\sigma = 0.63$  ns Propagation delays due to 120 fibers measured:  $\sigma = 0.9$  ns

Clock phases at SPD inputs without correction:  $\sigma = 1.1 \text{ ns}$ 

Delays added to the clock transmitters to compensate for differences Clock phases at SPD inputs with correction:  $\sigma = 0.08$  ns

5 November 2009

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#### What we learned?



- Use optical fibers with the same length is an important requirement but ...
- A flexible system is also better
  - Settings to equalize the delays in each channel
  - Settings to adjust the overall time w.r.t. the LHC clock



Tools to monitor the data output



#### Motivation

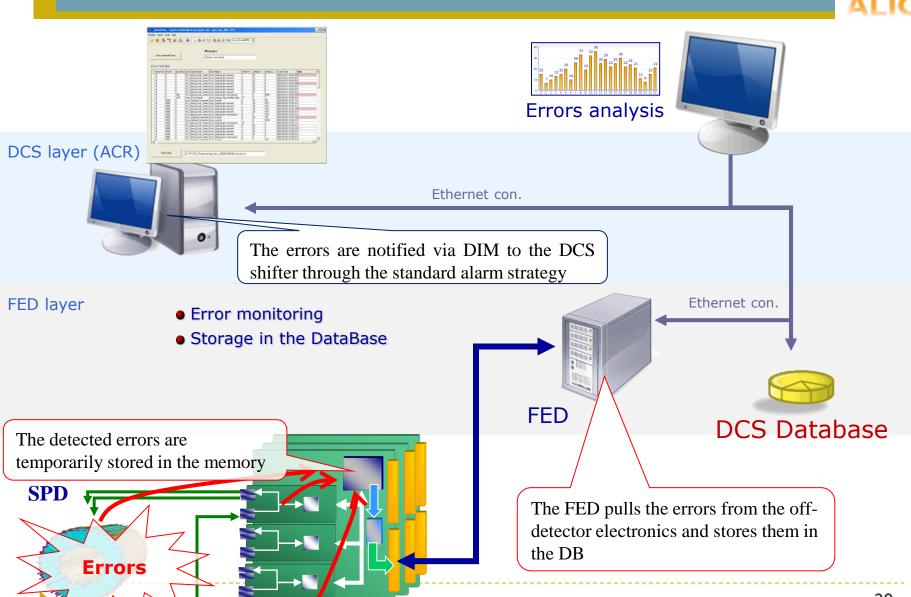


- Identify the source of problems and fix the failures in complex systems it is always a very hard tasks
  - ▶ FEE-electronics, Off-detector electronics, Link communication ...
- It is often hard and extremely time consuming to reproduce the problem and to correlate it with external condition
  - ▶ Trigger schema, partition schema, beam dependence ...
- This is the reason why a system capable to monitor the data output, to flag errors and to store the hardware conditions without disturbing the acquisition would help the expert... but, is that feasible?
- If the system would also be able to suggest the proper action and even to fix the problem by himself... it would be a dream!!!!
  - but don't be so excited... we don't have it!!!
  - Although, the "Error handler" tool is extremely useful

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## "Error handler" strategy





Off-detector electronics

#### What we learned?



- The tool is extremely powerful and makes track of the low level information when the errors occur
- It is important to group errors in categories which can be masked accordingly to the expert needs
  - Useful to avoid that warnings fulfill the DB
- Statistic studies could be useful to monitor the electronics stability or to identify frequent failures



Thanks for your attention



## Spares



## Fast-OR Algorithms



1	Minimum Bias	(I+O)≥th <sub>IO,mb</sub> and I≥th <sub>I,mb</sub> and O≥th <sub>O,mb</sub>
2	High Multiplicity 1	l≥th <sub>I,hm1</sub> and O≥th <sub>O,hm1</sub>
3	High Multiplicity 2	l≥th <sub>I,hm2</sub> and O≥th <sub>O,hm2</sub>
4	High Multiplicity 3	l≥th <sub>I,hm3</sub> and O≥th <sub>O,hm3</sub>
5	High Multiplicity 4	l≥th <sub>I,hm4</sub> and O≥th <sub>O,hm4</sub>
6	Past Future Prot	$(I+O)\ge th_{IO,pfp}$ and $I\ge th_{I,pfp}$ and $O\ge th_{O,pfp}$
7	Background(0)	l ≥ O+ offset <sub>O</sub>
8	Background(1)	O ≥ I+ offset <sub>I</sub>
9	Background(2)	$(I+O) \ge th_{(I+O),bnd}$
10	Cosmic	Selectable coincidence, see following list

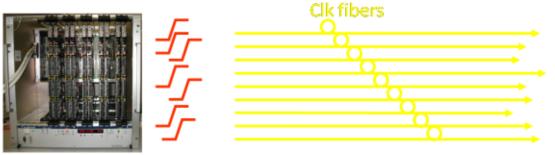
#### **Cosmic algorithms:**

- ▶ TOP\_outer and BOTTOM\_outer
- OR\_OUTER and OR\_INNER
- ▶ DLAYER ( $\geq$  2 FOs in the INNER and  $\geq$  2 FOs in the OUTER)
- TOP\_outer and BOTTOM\_outer and TOP\_inner and BOTTOM\_inner
- ► TOP\_outer and BOTTOM\_outer and OR\_INNER
- GLOBAL\_OR

## Timing optimization

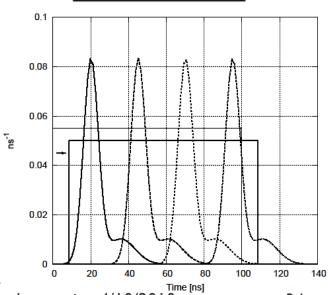


- Fine tuning of the timing for each individual Half-Stave
  - delay added to the clock transmitters to compensate for differences
  - Distribution of clock phases at SPD inputs after correction:  $\sigma = 0.08$  ns

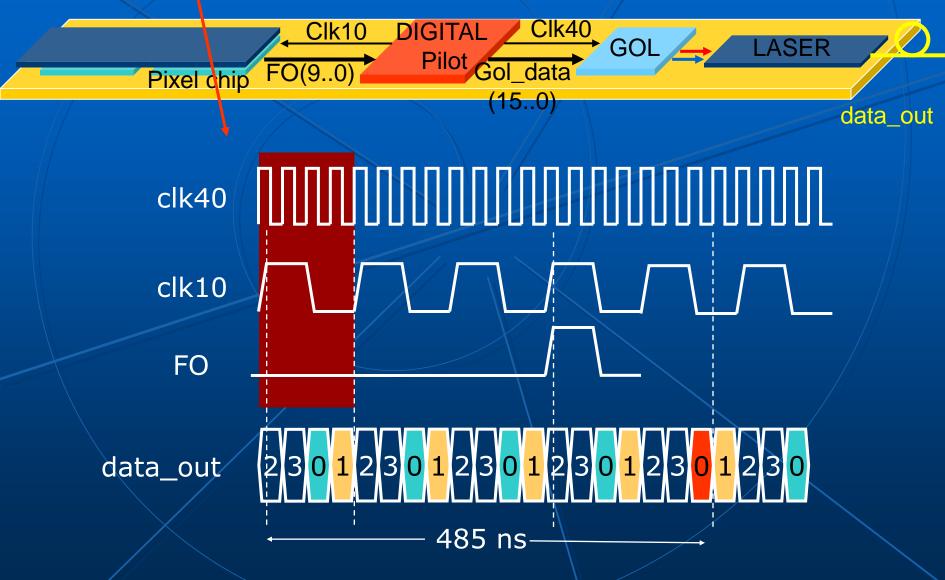


**Clk outputs** 

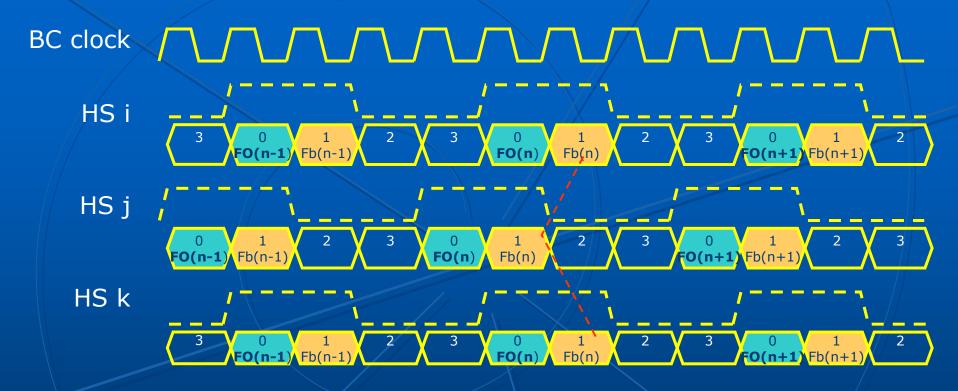
- Fine tuning of the SPD clock phase with respect to the LHC clock (SPD clock 10MHz)
  - Dedicated calibration during collisions has been performed
  - Measure pixel multiplicities versus clock phases
  - Set optimal phase in the clock domain



# Fast OR timing



## Synchronization



- 40 MHz clocks aligned by equalizing fibers length
- 10 MHz clock phases aligned by broadcast signal on TTC
- One clock period uncertainty left
   -> Measure relative phases
  - Measure arrival time of trigger feedback

# Frame alignment

