

Quality issues in bump bonding for HEP – generic observations over 10 years at VTT

Quality Issues in Current and Future Silicon Detectors workshop
3-November-2011

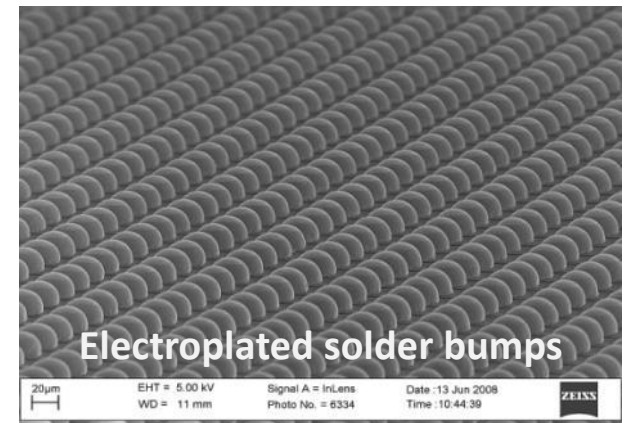
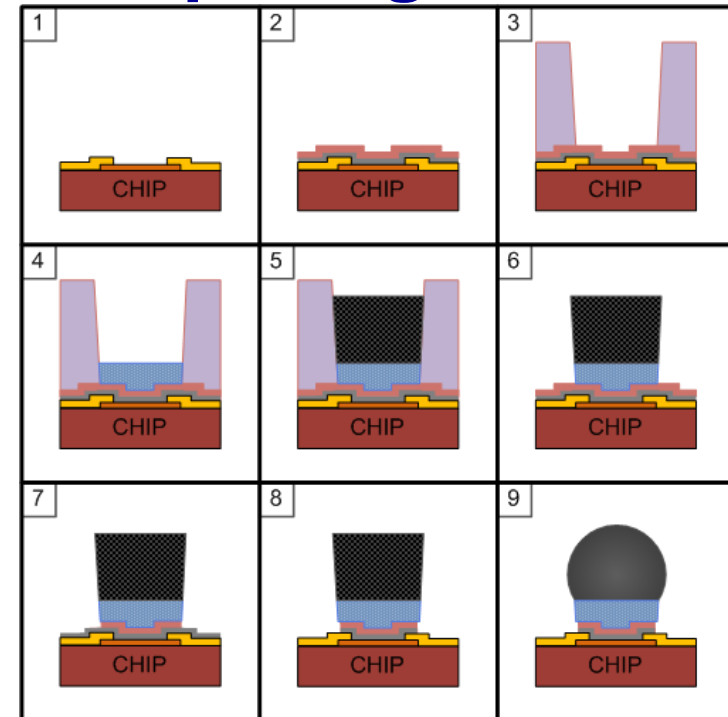
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Outline

- **Introduction to bump bonding**
- **Recorded issues in bump bonding with readout and sensor wafers**
 - **Testing**
 - **Dicing**
 - **Assembly**
- **Shipping - Gelpaks**
- **Yield & actual cost**
- **Technology development**
- **Summary**
- **Backup slides**
 - **Wafer-level alignment marks**
 - **Solder bump design rules**

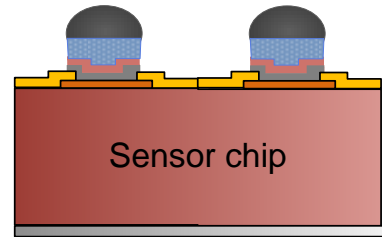
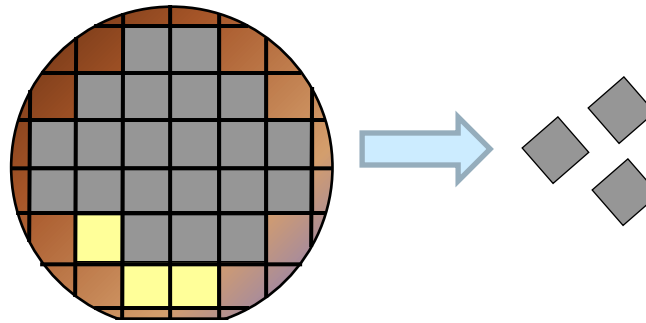
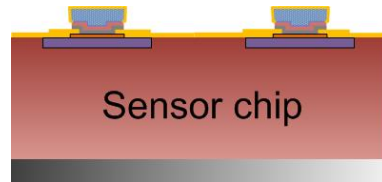
Solder μ -Bumping Using Electroplating

- Solder bumping using electroplating is a single-mask process (sketch on the right)
- TiW/Cu seed layers used for electroplating (step 2)
- Photolithography (step 3)
- Electroplating steps
 - Ni or Cu is typically used as UBM (step 4)
 - Solder is deposited on top of UBM (step 5)
 - Solder alloys: SnAg(<5%), InSn (low MP solder), SnPb (eutectic) & Sn
- Photoresist is stripped and seed layers are wet etched away (steps 6-8)
- Solder reflow – a flux-free process (step 9)
 - Solder reflow done in reducing gas ambient – no flux residues

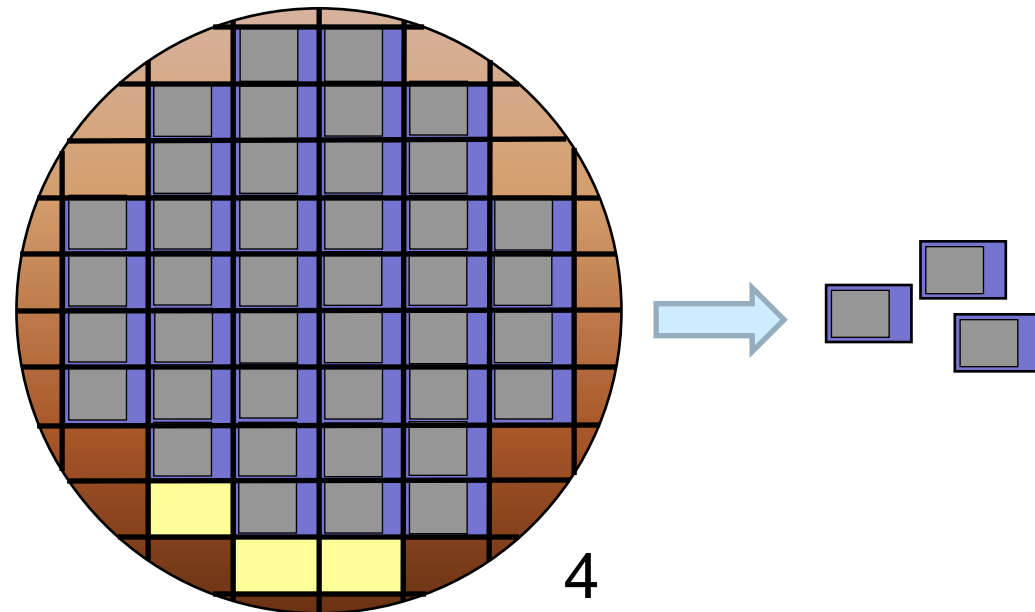
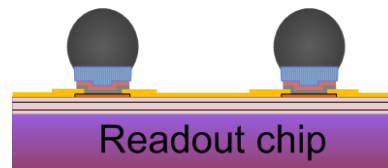


Dicing

4"-6" hi-res Si sensor wafer with solderable pads or with solder bumps



Thinned 8" readout wafer with solder bumps



Flip Chip Bonding

- **High-accuracy bonding equipment:**

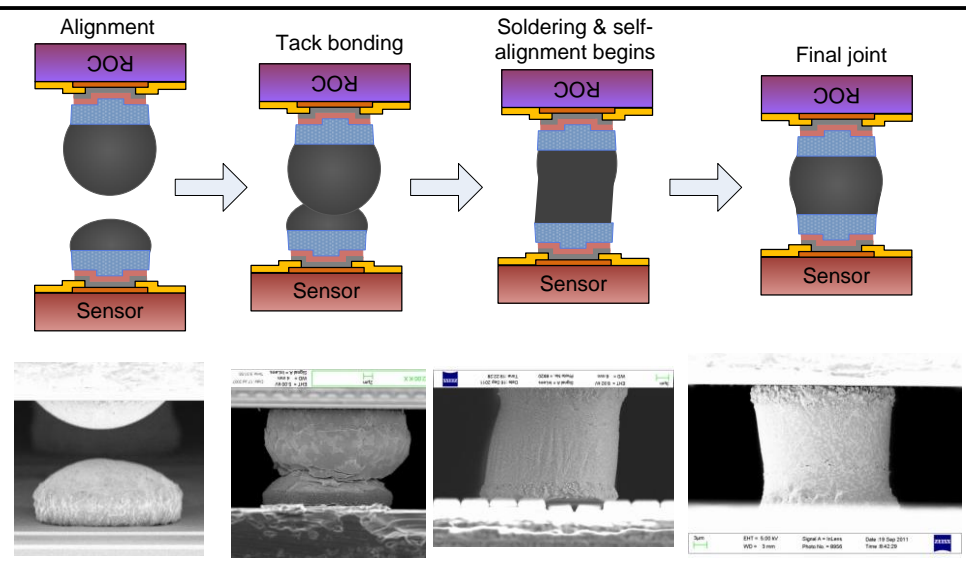
- Assembly have been done on chip-to-chip level
- Accuracy of the bonders are good enough for pixels
- Throughput is a problem

- **Solder bumps are deposited on both chips to be assembled**

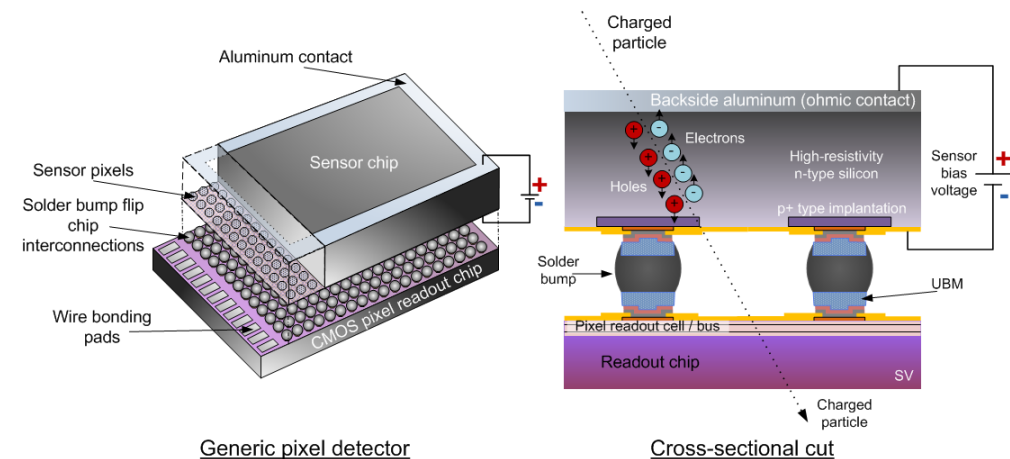
- Beneficial for rework (replacing defective readout chips on sensor)

- **Bonding cycle:**

- Alignment, levelling and tackbonding routine with "assembly reflow" process (solder is not melted in the flip chip bondig phase)



Flip chip bonding routine at VTT

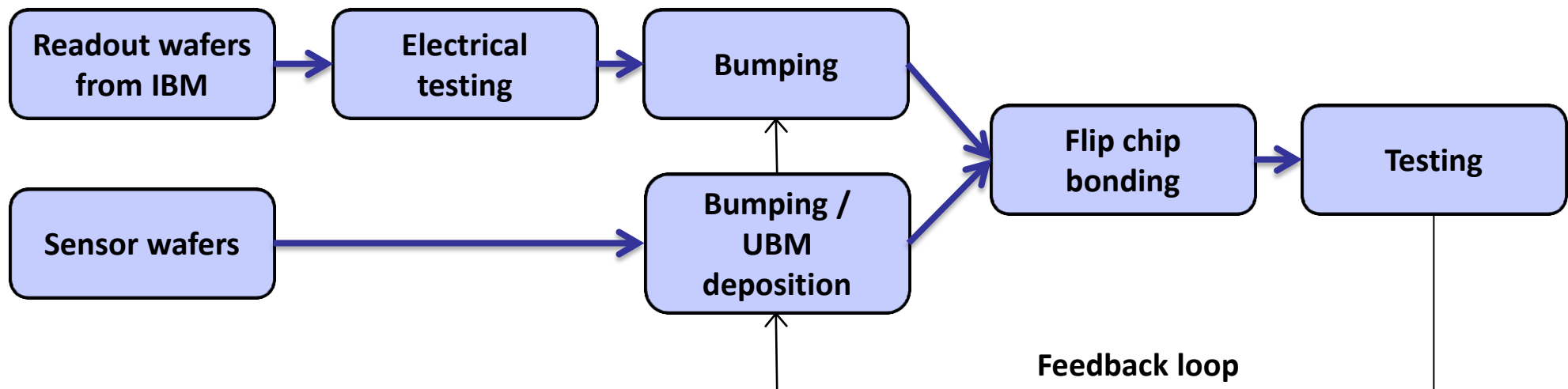


Typical Logistics for Readout Wafers

- Typical logistics of readout wafers:

1. Wafers fabricated at IBM
 - High-quality clean room – clean wafers
2. Wafers are probed at research institutes
 - Poor quality clean room – high risk of contamination
3. Flip chip processing at packaging house
 - Good quality clean room – sensitive process against contamination
4. Testing of assemblies at research institutes – poor quality clean room

- Rule of thumb: Do not let the wafers get contaminated prior to process steps that are sensitive against all contamination – contaminated wafers cannot be cleaned!



Issues with Wafers Before Bump Bonding

- **Four main types of contamination/damage seen on wafers at incoming inspection**

- **Particles**

- Handling of wafers without showing care
- Exposing wafers to air in poor quality clean room

- **Scratches**

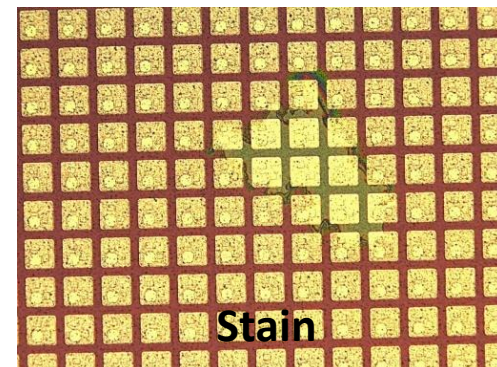
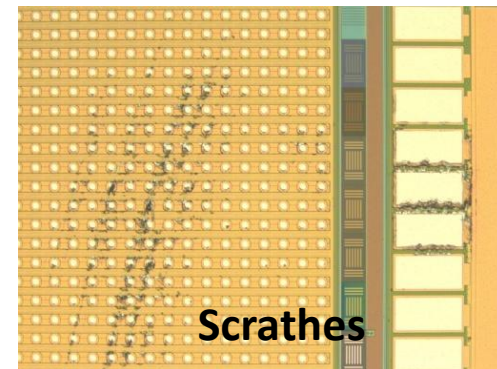
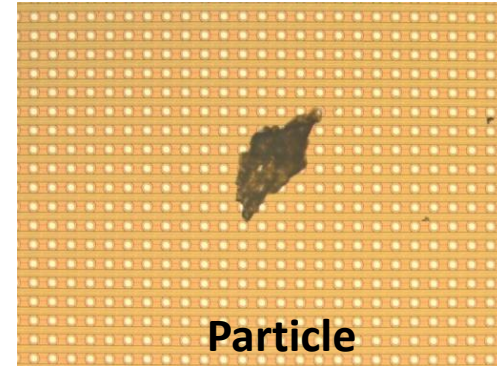
- Human mistakes during probing and wafer handling

- **Stains**

- Organic substance on sensors
- Almost impossible to understand their effect

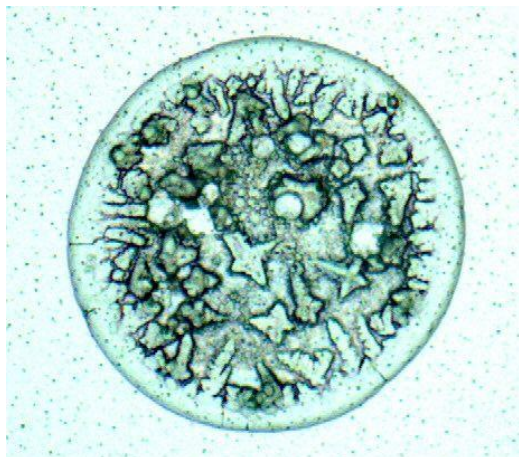
- **Metal contamination**

- Can be transferred on wafers during the testing
- Especially problematic for TSV processing in metal-ion clean foundries

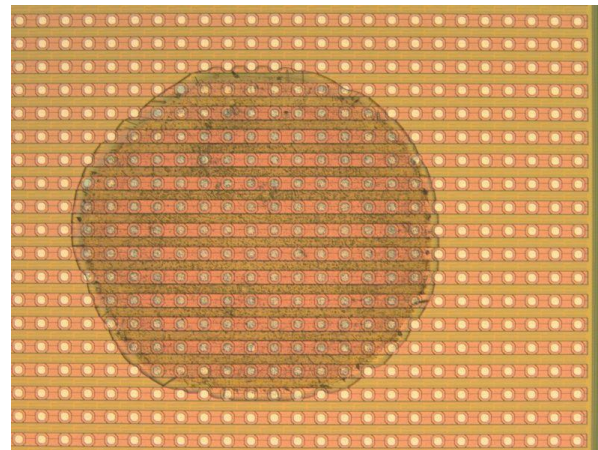


Dressing Code - Examples

- Proper dressing code should be followed when handling of wafers
- It is worthwhile investing in protective gear (example on next slide)
 - Clean room coat & hat to avoid dust, hair and particles
 - Mouth mask to minimize the risk of spitting on wafers when coughing
 - Disposable rubber gloves to avoid particles and dust – wafers shouldn't be touched by hands
 - Use tweezers to avoid grease



Sensor: something under Al



ROC: dried organic matter

Calculation Example – Value of KGD

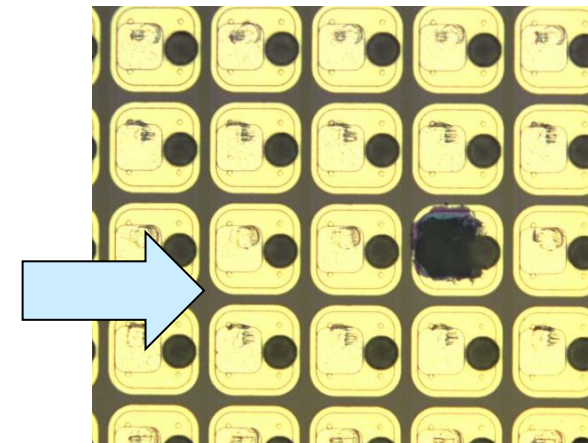
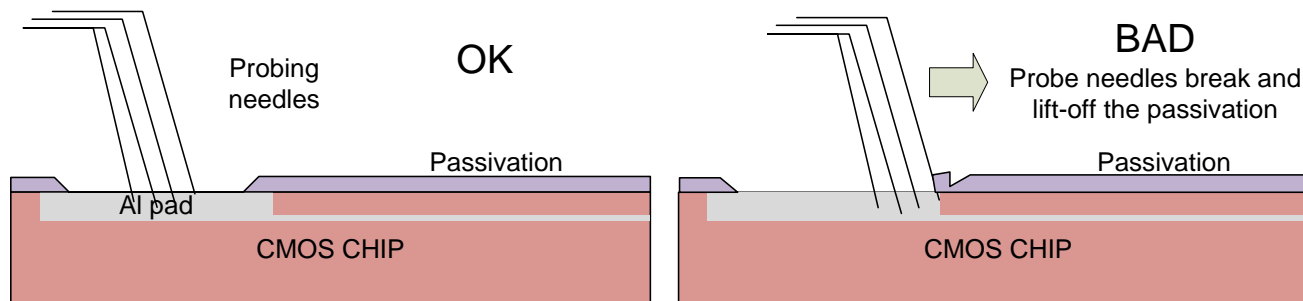
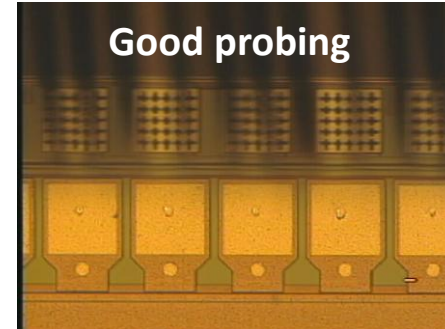
- **Readout wafers cost 2,000€ at IBM will be refined to wafers with a value of about 6,000€ after probing, solder bumping and dicing**
 - Typically the electrical yield of large ROCs is low $\sim 60\%$
 - Assumed number of ROCs per wafer is 100
 - Yield will be further reduced during the solder bumping process (solder bumping yield is not 100%)
 - Eventually about 50 % the all ROCs on the wafer can be used for flip chip bonding
 - Each good ROC going for flip chip bonding will cost 120€
 - *Local, non-removable, contamination will cost ≥ 120 €!*
- **Sensor wafers are not typically probed**
 - Fabrication yield is good $> 90\%$
- **Sensors suffer from inconsistent quality which effectively drops the yield of bump bonding**
 - Disturbing film stresses \rightarrow significant bow often seen \rightarrow problematic for flip chip bonding of large sensor modules

Electrical Testing

- **First electrical testing is typically done at a research institute to specify KGDs**
- **Second testing round is done after the flip chip assembly**
 - **Importance of prompt feedback**
 - Reacting early to problems
 - FC bonding quality control
- **Long feedback time create many delays**
 - Typical for phases when there is some uncertainty
 - Changes in the basic process
- **On site testing after flip chip assembly should be considered**
 - **Best solution**
 - **Electrical testing (probing with source) to be greatly simplified**
 - Simple pass or fail criteria
 - Probing should be simplified if it is going to be done at packaging houses

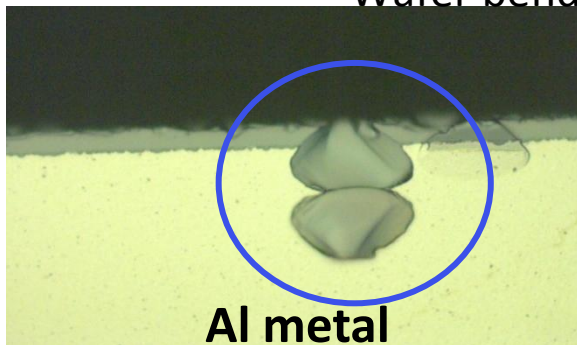
Issues with Probing of Wafers (before flip chip)

- Typically wafers are probed first and then send for flip chip processing
- Probing might destroy chips if:
 - Probes go too deep in Al
 - Electroless-Nickel Immersion-Gold (ENIG) deposition removes Al and might leave a spot without Al
 - Probes break and lift-off the passivation layer
 - Adhesion metal cannot protect Al from corrosive Cu etching chemicals because of discontinuous layer

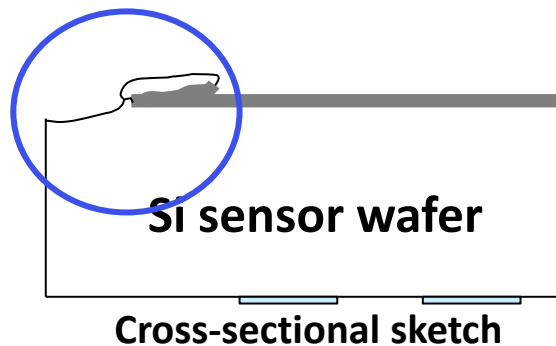


Sensor wafers – Back Side

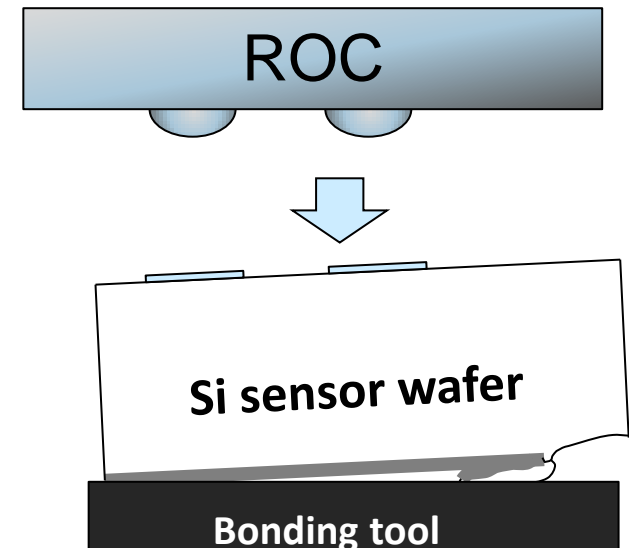
- It makes sense to have a passivation layer on the Al metallization but open it at dicing lanes to minimize chipping
 - Particles adhere well to soft Al
 - Hard glass passivation protects Al & Si from scratches
 - No scratches – easier interpretation if sensor can be used in flip chip
 - Film stresses become more symmetric (pixel side vs. back side)
- Patterning of Al on the back side of the sensor (not pixel side) is important
 - Less chipping that affects the leveling during the flip chip bonding
 - Dicing of thin wafers is creates lot of chipping
 - Wafer bends during dicing



Top view of a chipped silicon which has adhered to Al

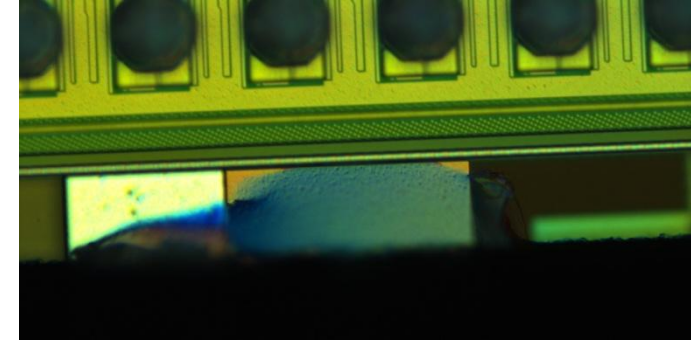


Cross-sectional sketch

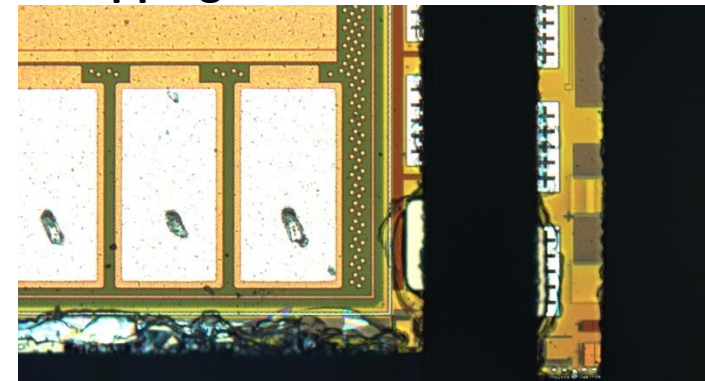


Hints to Optimize Dicing Quality

- **Designers: try to keep the dicing lanes clean**
 - **Metallic test structures cause large chipping and make visual inspection hard**
- **Make dicing lanes with equal width if possible in X and Y directions**
 - **Sensors: 80 μm**
 - Do not place critical implantations near the dicing lane
 - Unacceptable leakage currents
 - **Readout wafers: 100 μm**
 - Improving of dicing accuracy
 - It's better to have clear dicing lanes and dice at the center
 - Control marginal to chip frame by using different blade widths
- **Open the passivation at the dicing lanes for sensor wafers**



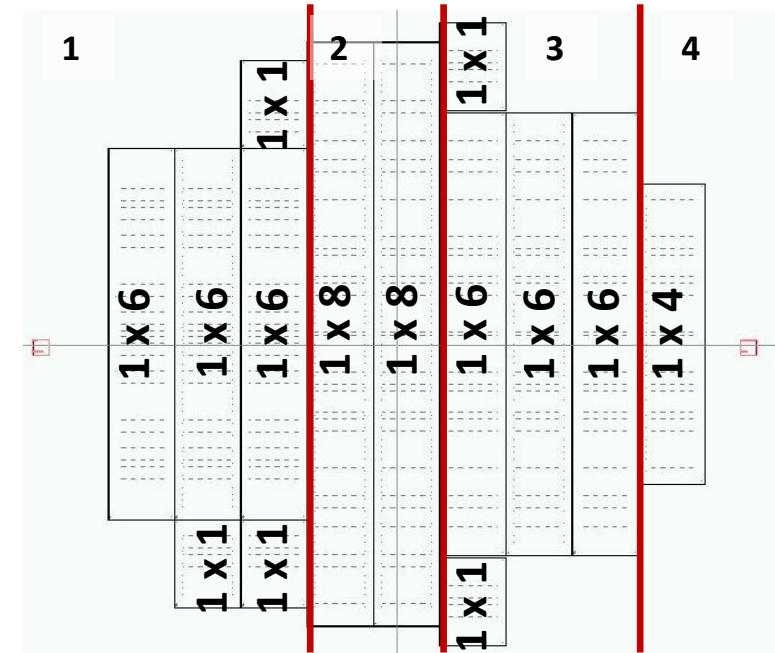
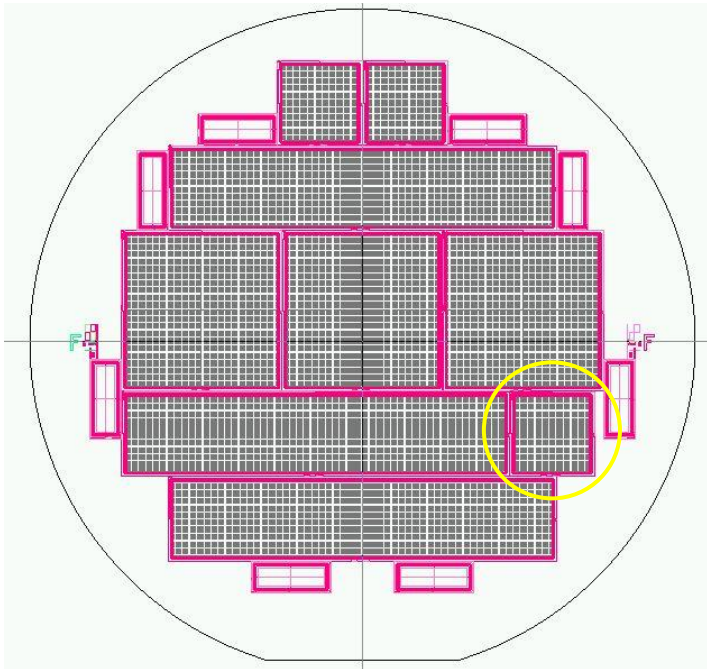
Bad example: Al test structures blocks cause huge surface chipping



Two cuts per one street cause inaccuracy and difficulty for programming

"Dicer's Nightmare" - Examples

- Sensor wafer layouts can cause headache
- It is worthwhile to put some effort in layout designs
- Picture shows an example in which the wafer has to be diced and re-laminated 4 times
 - Dicing becomes very time consuming

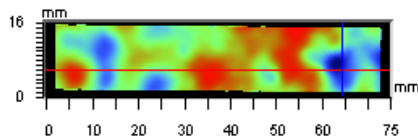


- Wise arrangement of chips saves time in dicing of sensor wafers
- Wafers should be diced with one go or with one re-lamination and dicing steps
- All the wafer area doesn't have to be covered with sensors

Example: Exchanging Sensor Wafers One Type to Another

- Changing sensor wafers or their passivation should be avoided during any production
- Bow measurement over one (diced) sensor from the back side blank aluminum

The back side profile is OK in terms of total thickness variation ($12\text{ }\mu\text{m}$), but it's not tolerable within adjacent sensor sites.



On the right end of ladder, there's a 12-micron height difference within 1 - 2 bonding sites.

| | | | | |
|-------|-------|---|---|---------------|
| X | 64.32 | - | - | mm |
| Y | 5.69 | - | - | mm |
| Ht | -6.37 | - | - | μm |
| Dist | | - | - | mm |
| Angle | | - | - | $^{\circ}$ |

Title: IRST sensor -292

Note: Ladder 1. 2.5X magn, 0.5X FOV, speed 3

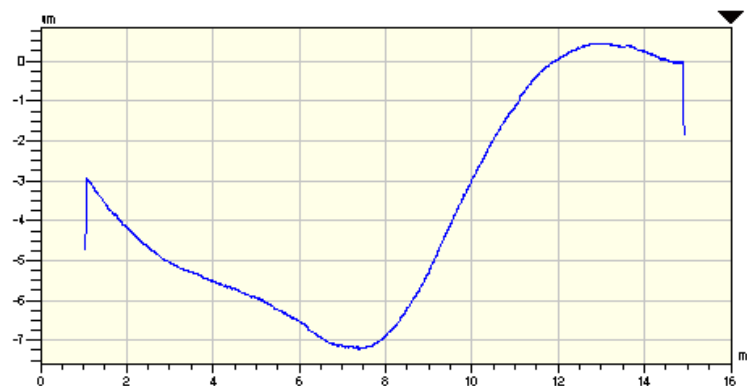
X Profile



| | |
|----|---------------------|
| Rq | 3.10 μm |
| Ra | 2.61 μm |
| Rt | 11.96 μm |
| Rp | 5.06 μm |
| Rv | -6.90 μm |

| | |
|--------|----------------------|
| Angle | 0.00 mrad |
| Curve | -0.17 km |
| Terms | None |
| Avg Ht | 0.30 μm |
| Area | 0.02 mm ² |

Y Profile

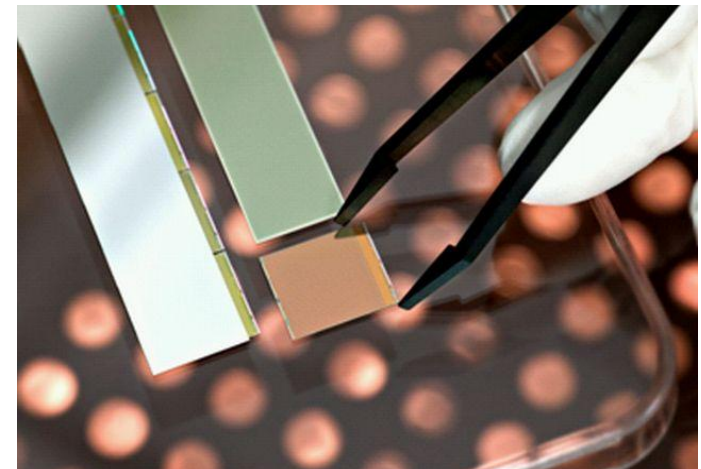


| | |
|----|---------------------|
| Rq | 2.72 μm |
| Ra | 2.42 μm |
| Rt | 7.67 μm |
| Rp | 0.44 μm |
| Rv | -7.23 μm |

| | |
|--------|-----------------------|
| Angle | 0.00 mrad |
| Curve | 4.84 m |
| Terms | None |
| Avg Ht | -3.71 μm |
| Area | -0.06 mm ² |

Flip Chip Yield

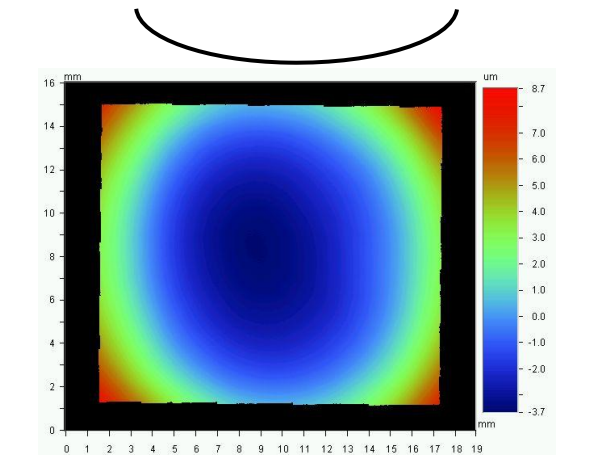
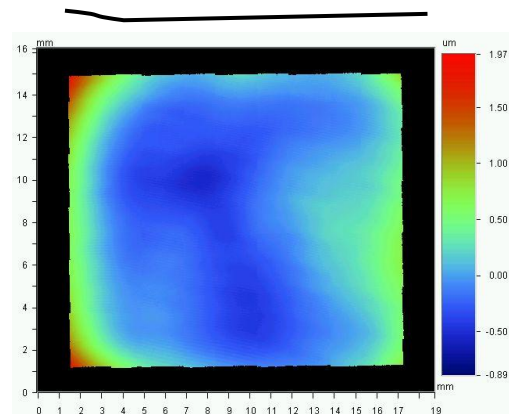
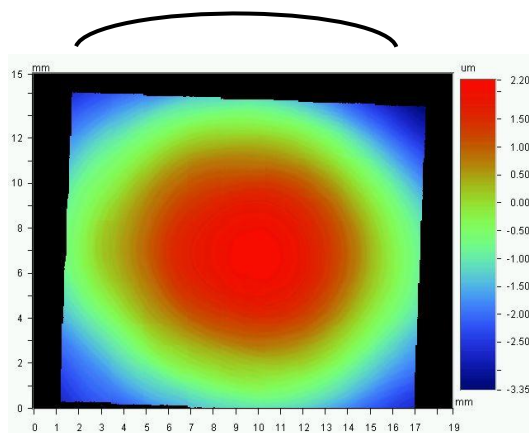
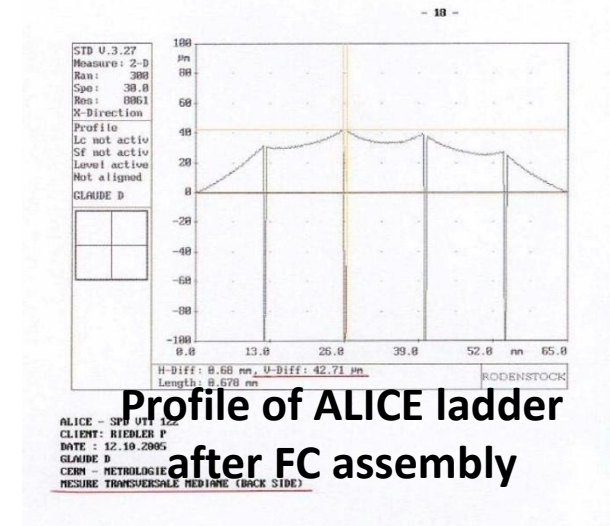
- **FC assembly yield is fairly good (~ 95 %) but various things affect it**
 - **Particles on the backside of the sensor has a great (negative) impact on the bonding yield.**
 - **Solder bumping process has a major effect on the assembly yield**
 - All the issues with either wafers or solder bumps will realize here
 - Bump bonding is expensive and time consuming and many of the problems will be observed in the very end of the process
 - Waste of resources
- **Handling of chips prior to flip chip assembly may damage the ROCs**
 - It is difficult to spot micro cracks



ROC Profiles Before and After the FC Assembly

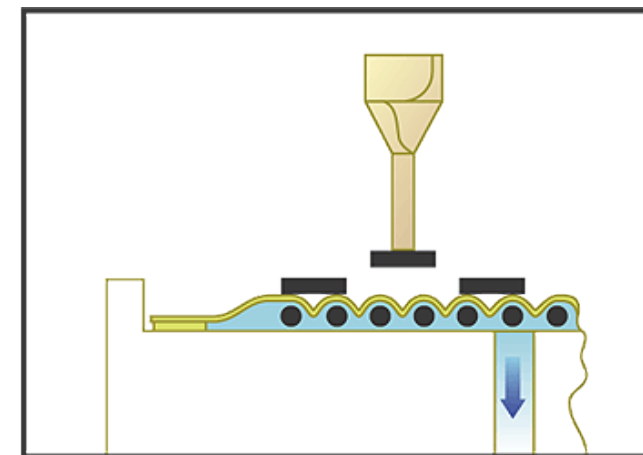
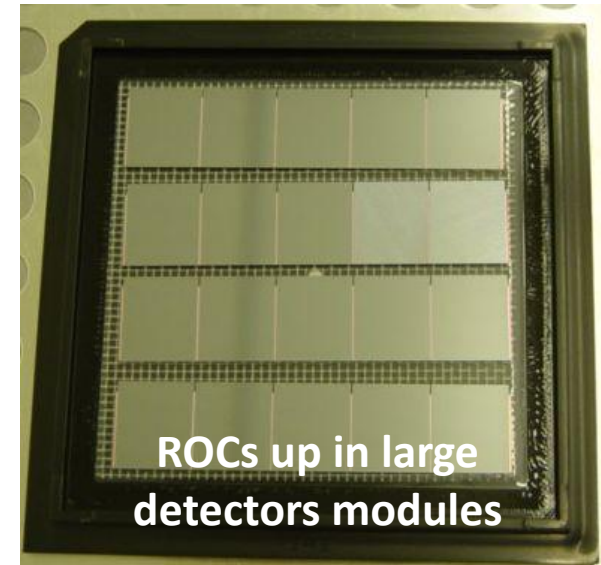
- Thinning of chips brings challenges to the flip chip bonding
- Strong sensor bow was disturbing the flip chip bonding
 - Open solder joints were seen at chip corners
- Open solder joints were often seen in ALICE project
 - Optical (white light) profilometer was used to measure the polished back side of the ROCs (150 μm thick)
 - Wire bonding pads are heading to left

Mesure transversale mediane (Back side)



Shipping - GelPaks

- GelPaks are perfect for shipping detectors
- Glue retention level and mesh value (grid density) can be chosen
- We learned that in multi-roc detector modules, large sensor side has to be placed against the glue
 - Polished bulk Si interface of ROCs adhered too aggressively to the glue
- GelPaks with X0 retention level and grid R4 had no problems in short run
 - GelPaks with X4 retention level and grid R16 had problems with removal of assembled detectors – film had to be broken and peeled off
- However, issues with aging of the glue – glue residues



Operation principle of a GelPak

Actual Cost of FC Processing

- **Bump bonding of pixel detectors has been expensive**
 - Although bump bonding seems to be trivial (one mask level process) the process takes a effort and is sensitive
- **By ambitious packaging and low volumes it is difficult to achieve low cost – lower costs is available in high volume production**
 - Experiments could work together to gain higher assembly volumes
- **Cost is dependent on the number of chips per wafer and the electrical/bumping yield and the state of the wafers**
- **Actual processing cost can be affected by optimizing the wafer layouts**
 - Discussion with the assembly partners in advance about the wafer layout
- **Wafer breakage of a significant cost adding factor**
 - Thin sensor wafers break easily and thinning of readout wafers was a problem in ALICE production
 - Reserve additional wafers (25% or so) to prepare for unexpected issues

Availability of the Desired Assembly Technology

- **Challenges of the bump bonding will become tougher when the chips are thinned to 100 μm**
 - Support chips or stress compensation layers may have to be used to have good quality detector assemblies
- **Technical challenges are difficult and technology development has to be done in advance**
- **It might be worthwhile to have combined development projects between CERN experiments and packaging houses**
- **It is worthwhile to test the full assembly chain before the production**
 - Less unexpected issues

Summary

- Many issues were shown which have an impact on the bump bonding yields and actual processing costs
- Electrical testing is mandatory but the conditions have to be improved
 - Proper handling of wafers paying attention to cleanliness
- It is important to discuss about the designs with the wafer fabrication foundries and the packaging house to optimize the wafer layouts for packaging

Summary Table - Yields

- Table summarizes the typical defects and points out the outcome

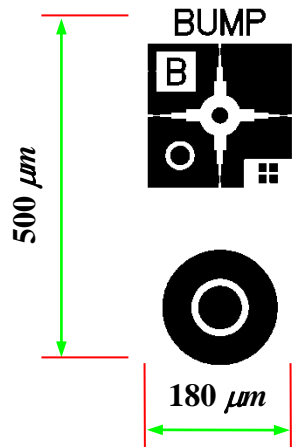
| PROCESS STEP | GUILTY PARTY | YIELD FACTOR | EFFECT |
|-----------------------|-------------------------------|---|---|
| Preprocessing | Silicon foundry | Defects, particle contamination | Lost chips and lost pixels |
| Wafer level testing | Customer / research institute | Probing | Bumping yield goes down, wrong classification of ROCs |
| Bumping | Packaging house | Missing bumps, shorts | Lost pixels and chips |
| Dicing | Packaging house | Chipping | increased leakage current, reduced die strength |
| Wafer thinning | Packaging house | Wafer breakage | Lost wafers |
| Chip handling | Packaging house | Chipping, scratches, micro-cracks | increased leakage current, defective ROCs |
| Bonding | Packaging house | Shorts, missing contacts, high contact resistance | Lost pixels |
| Post assembly testing | Customer / research institute | (accidental) mishandling | Lost detector modules |



**VTT creates business from
technology**

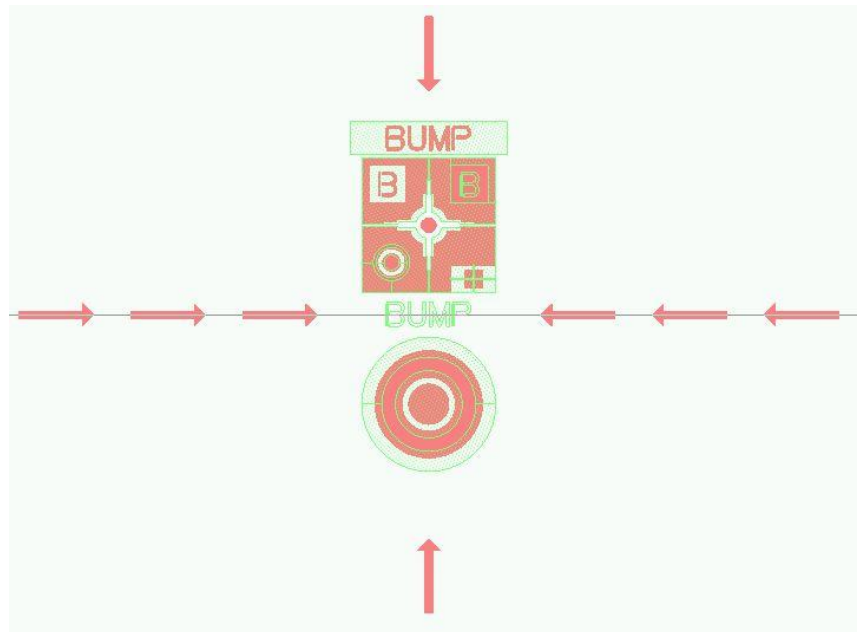
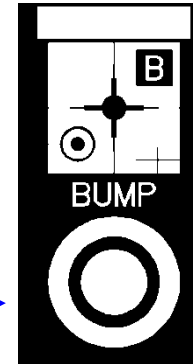
BACKUP SLIDES

Alignment Marks



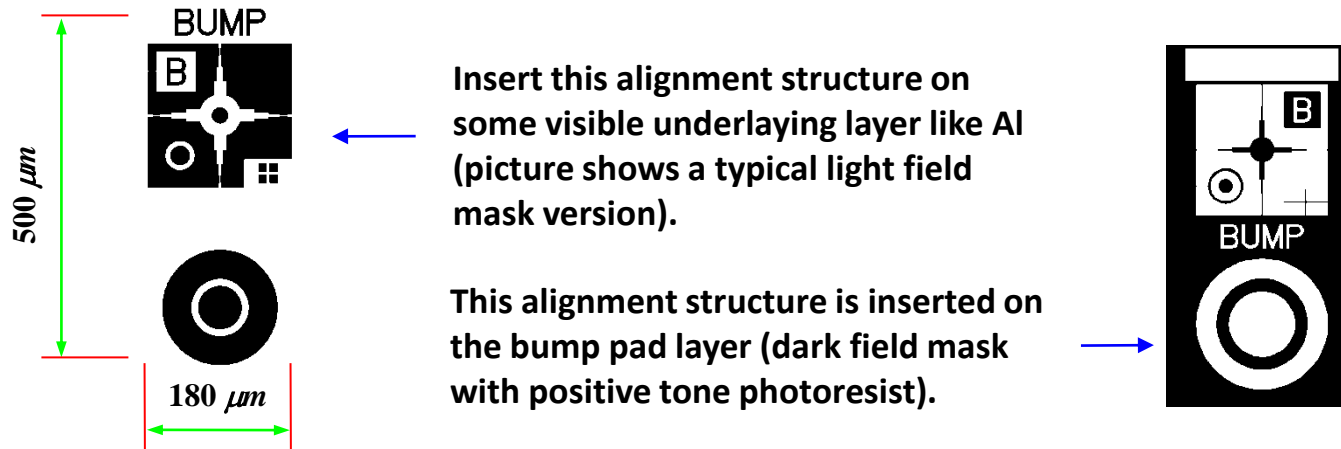
Insert this alignment structure on some visible underlayer like Al (picture shows a typical light field mask version).

This alignment structure is inserted on the bump pad layer (dark field mask with positive tone photoresist).

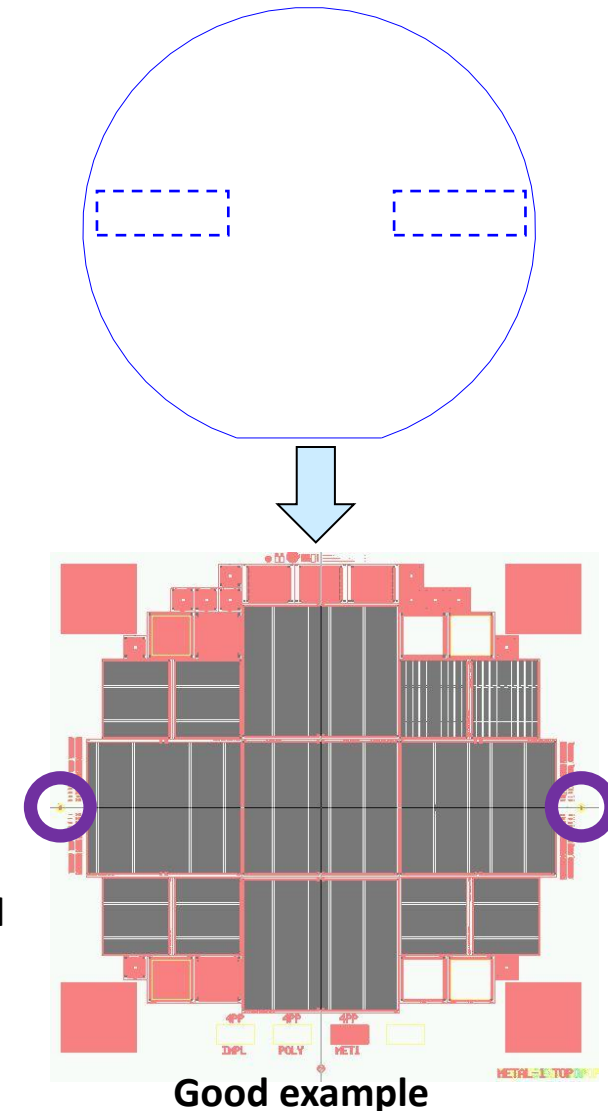


Good example: red = sensor metal
Green = VTT alignment mark

Alignment Marks

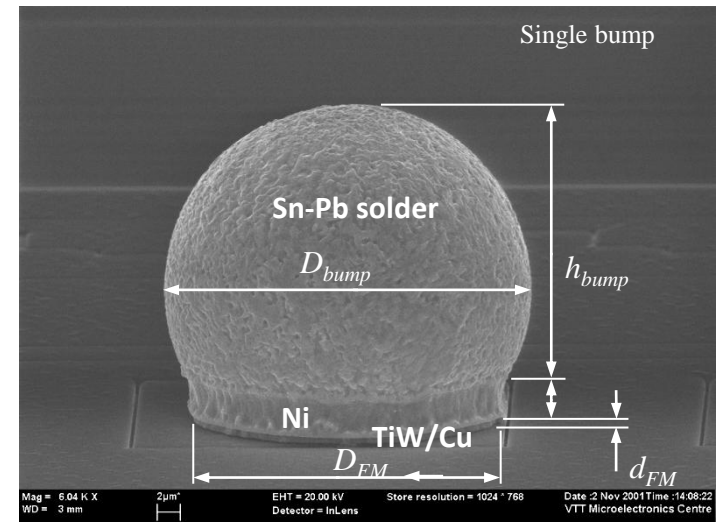
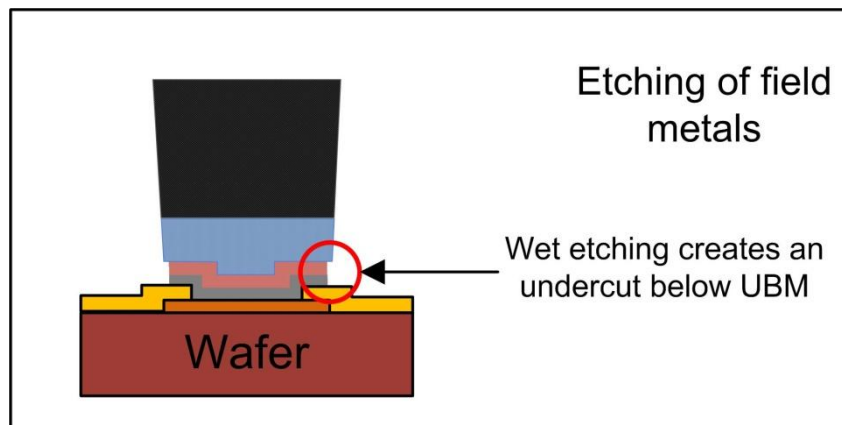


- Discuss about the alignment marks with wafer manufacturers and the packaging house.
- Place alignment structures (one in each field) near wafer center-line close to wafer perimeter (picture top right).
- Do not place alignment marks on dicing lanes or on the chip area to be flip chip bonded.
- Photolithography for bump electroplating is carried out using a wafer level contact mask.
- It is useful to have alignment marks at the corners of the sensor chips
 - Possibility for automatic alignment in flip chip bonding phase
 - Very useful also in dicing – automatic correction of the dicing trench



Design Rules for Bumping

- It is beneficial to seal the contact metallization and passivation opening hermetically
 - Protecting sensitive Al metallization
- Typically the diameter of the solder bump is 8 – 12 μm larger than the size of the passivation opening
 - This is to compensate:
 - Inaccuracy in mask alignment (up to 2 μm)
 - Underetching of the seed layer in wet etching of the seed layers (up to 2 μm per side)



Bump model (FM stands for field metal)