PAUL SCHERRER INSTITUT

PSI

Wir schaffen Wissen – heute für morgen

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CMS (barrel) pixel interconnection issues

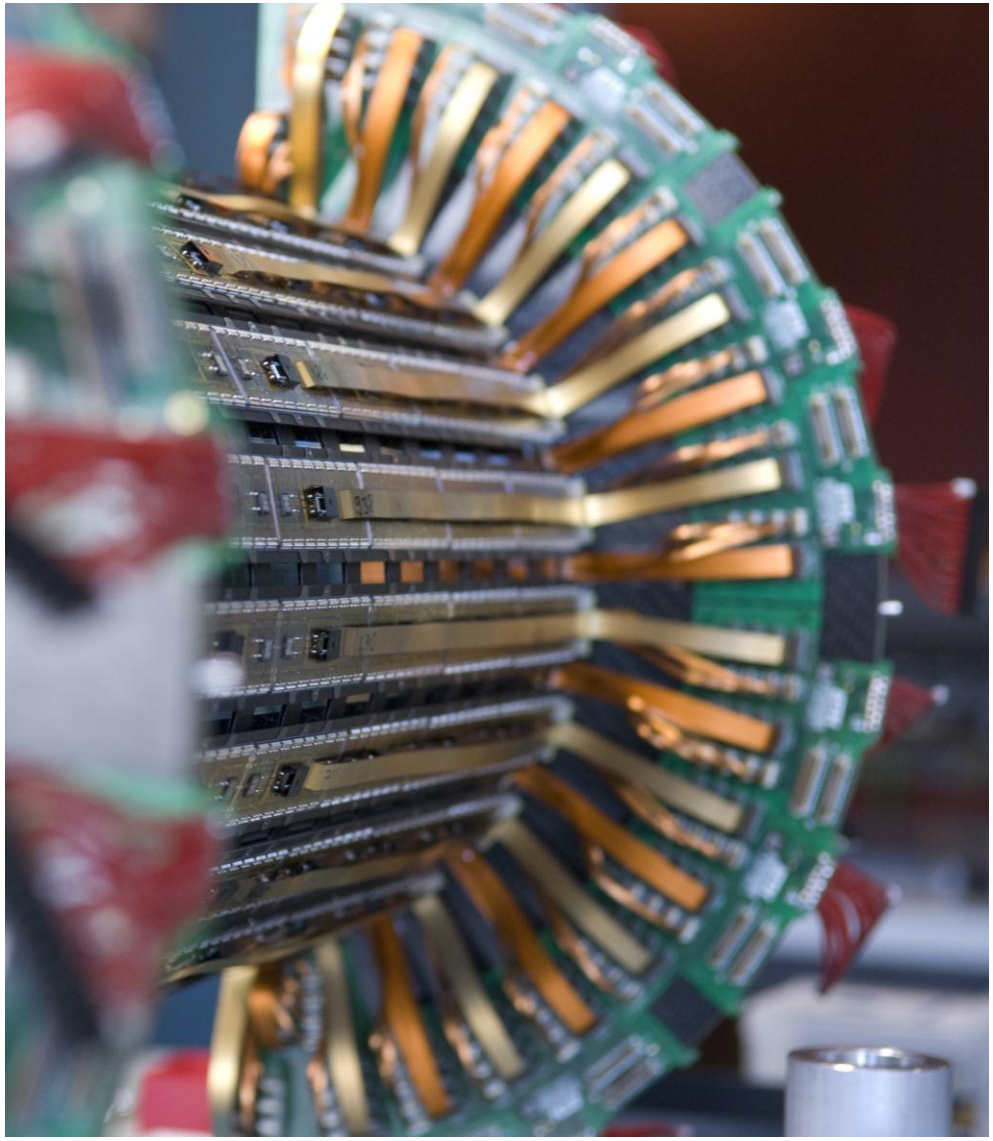
Introduction

Restrict on the construction of the CMS pixel barrel

- 1st hand experience
- FPIX are much different form barrel
  - Will probably agree in most conclusions
  - Try to mention differences

Personal remark

- Project was quite small (~1000 modules)
- Crucial steps were performed in-house
  - Daily interaction between the people
  - All people involved had vital interest in success



History:

- 1994: Pixel detector proposed for CMS, Technical Proposal
- 1998: Tracker Design Report
- 1994-2005: R&D on readout chip (ROC) and sensor
- 2005-2006: final version of ROC and sensors

BPIX:

- 6/2006-3/2008: module production and testing
- 11/2007-3/2008: mounting modules on ladders
- 2/2008-4/2008: integration with supply/service tubes
- 3/2008-6/2008: system tests at PSI
- **2008: insertion of BPix on July 23-24**

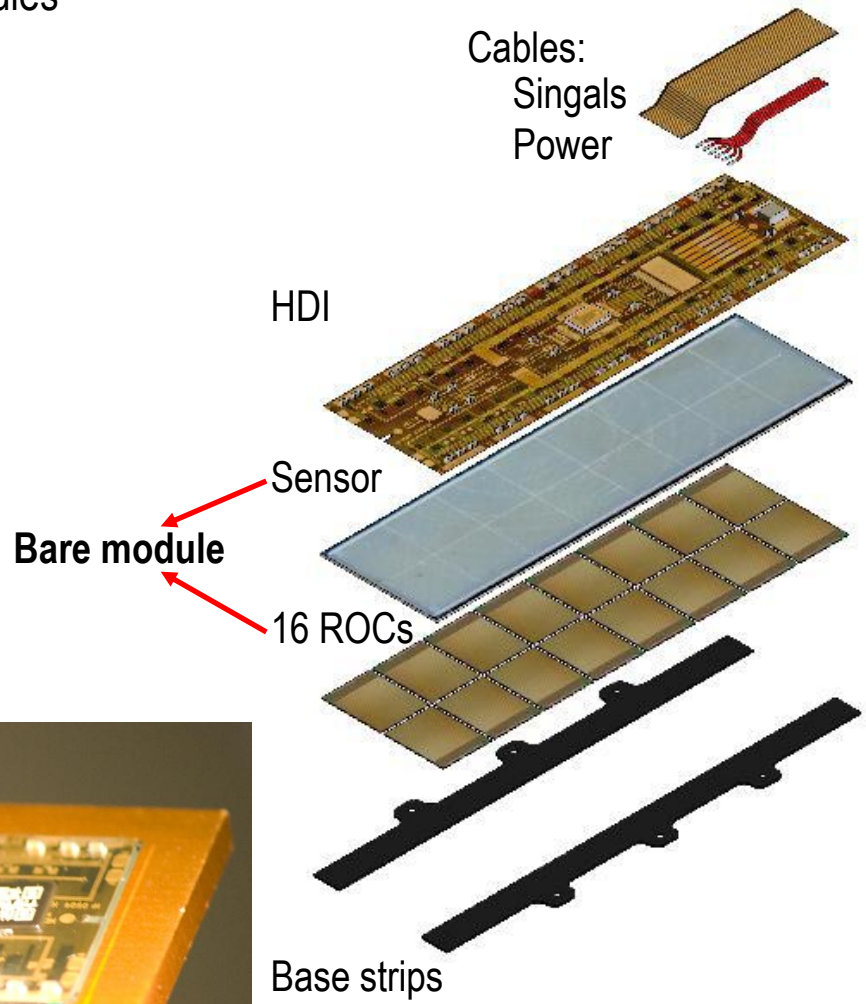
Pixel barrel module

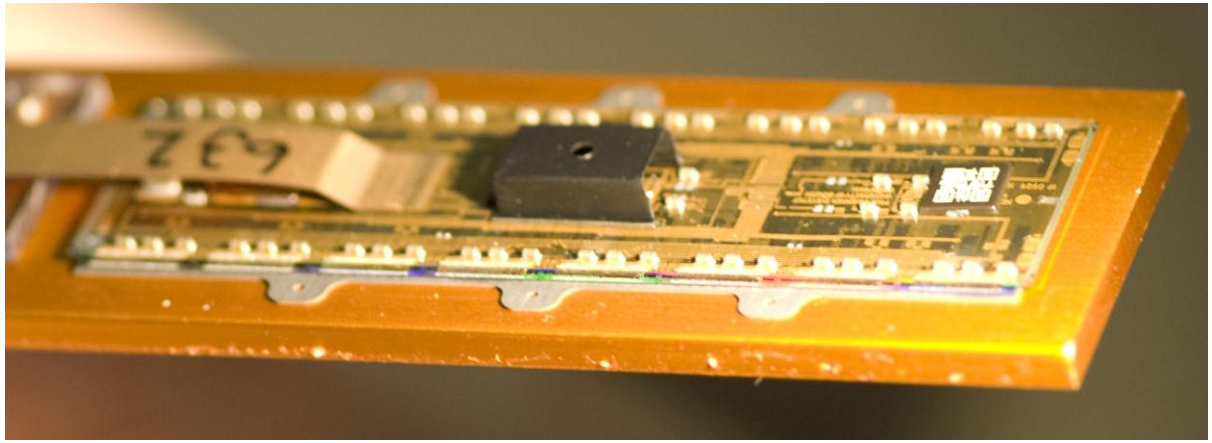
Total number of modules in CMS: 704/96 full/half modules

- Production time: ~1 ¾ yrs
- Team size: < 10 persons

Module parameters:

Full size: 66.6mm × 26mm
Sensor size: 66.6mm × 16.3mm
Segmentation: 16 × 4160=66560 pixels
Sensor thickness: 285 µm
ROC thickness: 180 µm
Weight: 3.5 g





Workflow for bare modules

ROCs
- After delivery
  - **Test of each ROC** using a semi-automatic probe station (wafer map used to group ROCs)

Post processing
- UBM and indium deposition
- **Optical inspection**
- Thinning
- Dicing
- Picking (group 16 good ROCs together) into tray
- Cleaning
- **Optical inspection**
- **Reduced functionality test on flip chip bonder**

Bare modules
- Join 1 sensor and 16 ROCs
- **Sensor IV**
- **ROC functionality**
- **Bump map**
- Last moment were a rework is possible

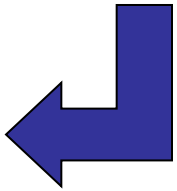
Module assembly
- Several gluing steps

Finished Module
- **Final qualification and calibration**

Final Integration

Sensors
- After delivery
  - Already tested and classified by vendor,
  - **IV-test of random sample only**
  - **Optical inspection**

Post processing
- Bump deposition
- **Optical inspection**
- Dicing
- Picking
- **IV-test**
- Cleaning (including the edges, labor intensive)
- **Optical Inspection**



Tests in total:

4 × ROC

3 × sensor IV

After production of >1000 modules, we consider all tests necessary

Optical inspection:

Important, but you need to know what to look for

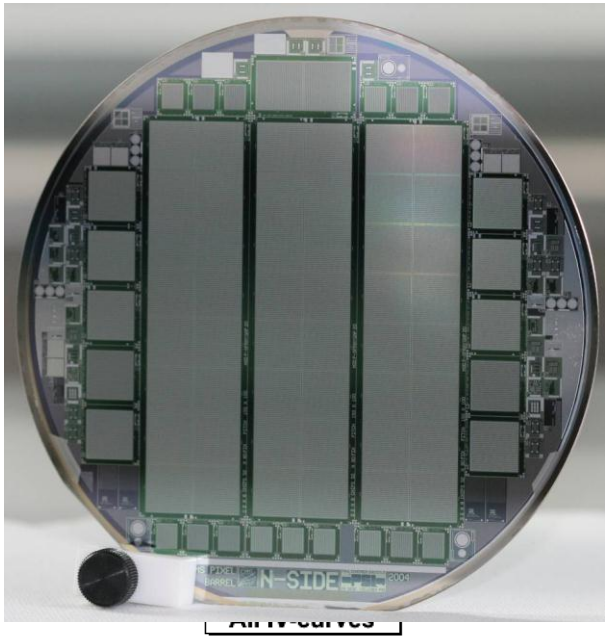
Test of sensors before bump bonding

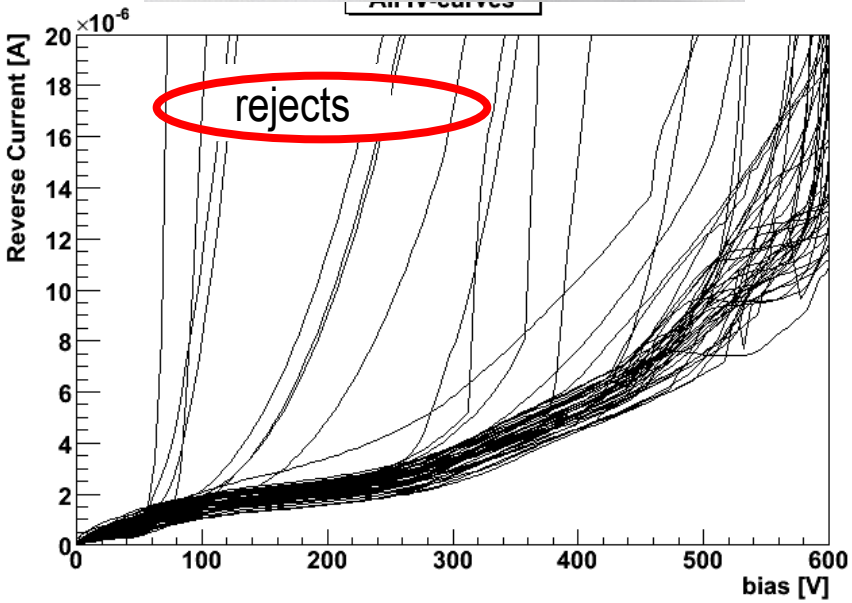
Module

- I(V=150V) < 2 µA (typical value ~1µA)
- Slope I(V=150V)/I(V=100V) < 2
- I(V=150) should be stable in time
- IV curve is very sensitive and a good indicator of device quality
- Test structures only used if there “was a reason”
- **Modules were tested on wafer by the supplier**
  - Only periodical checks were necessary

Post processing

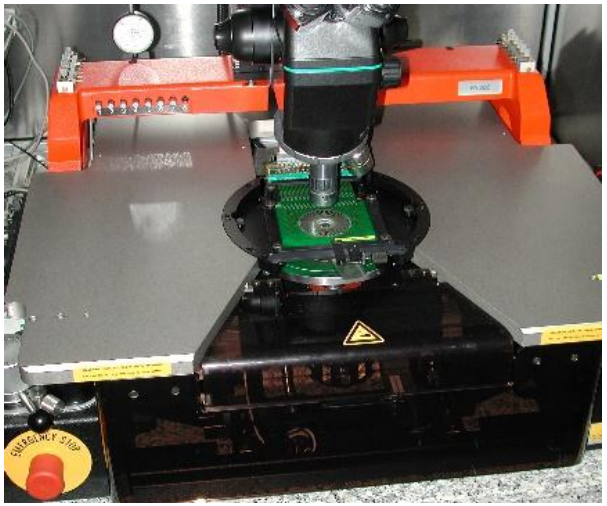
- Bump deposition (1 photo lithographic step)
- Dicing
- Picking
- **IV-test**
  - **Failure rate: about 7%**
  - Retest of each module after cutting
  - Important for the yield of the bare modules
  - Throughput of test: up to 24 wafers/day
- Cleaning, optical inspection and reflow





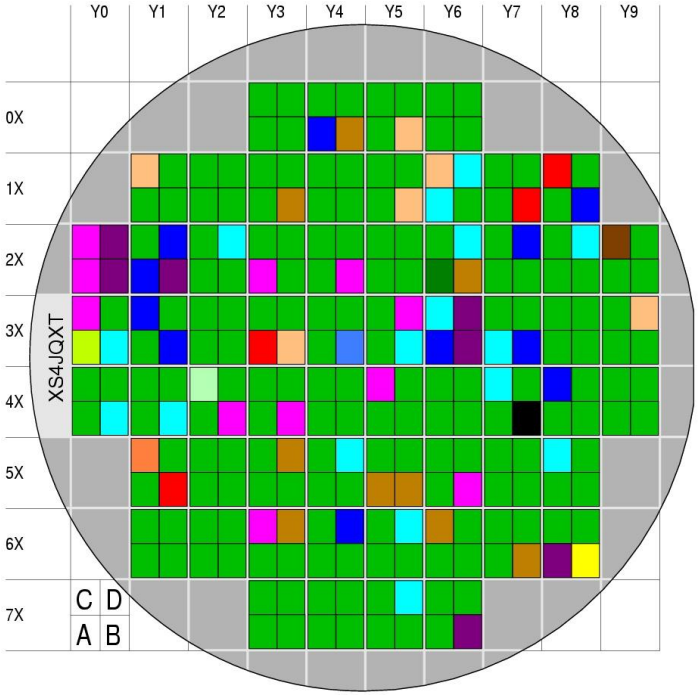
Test of ROC wafers before bump bonding

- Semi-automatic probe station (Suss PA 200)
- Probe card
- Test board (FPGA which generates signals and analyzes output)
- Throughput: 2h wafer (4 wafers per day)



Aim

- Check quality of delivered product
  - After post processing vendor will not accept complains
- Yield varies drastically between batches
  - Typical yield ~75%
- Group the chips to modules
- Get “feeling” for the distribution of chip parameters
  - Be able to detect changes caused by the bump bonding procedure



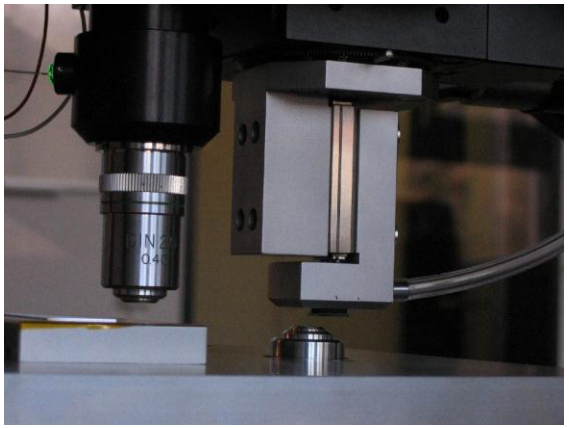
Post processing

- UBM and indium deposition (1 photolithographic step)
- Thinning (external)
- Dicing (external)
- Picking (external)
- Cleaning (PSI)
- **Lots of handling → expect to loose some devices**

Chip test on flip chip bonder

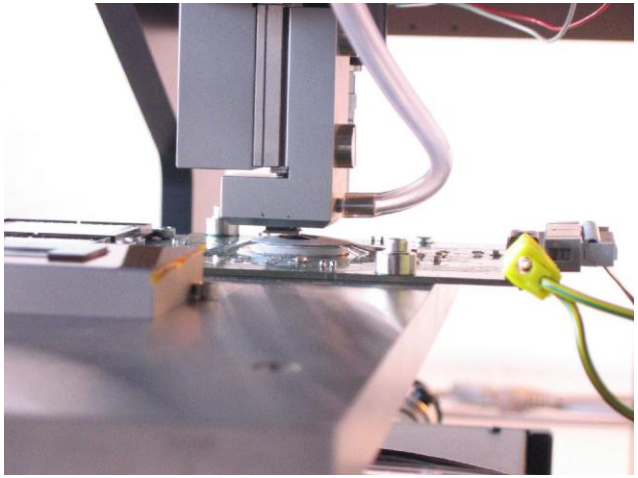
Test all ROCs after post processing

- Many individual (picked) ROCs
- Very labor intensive



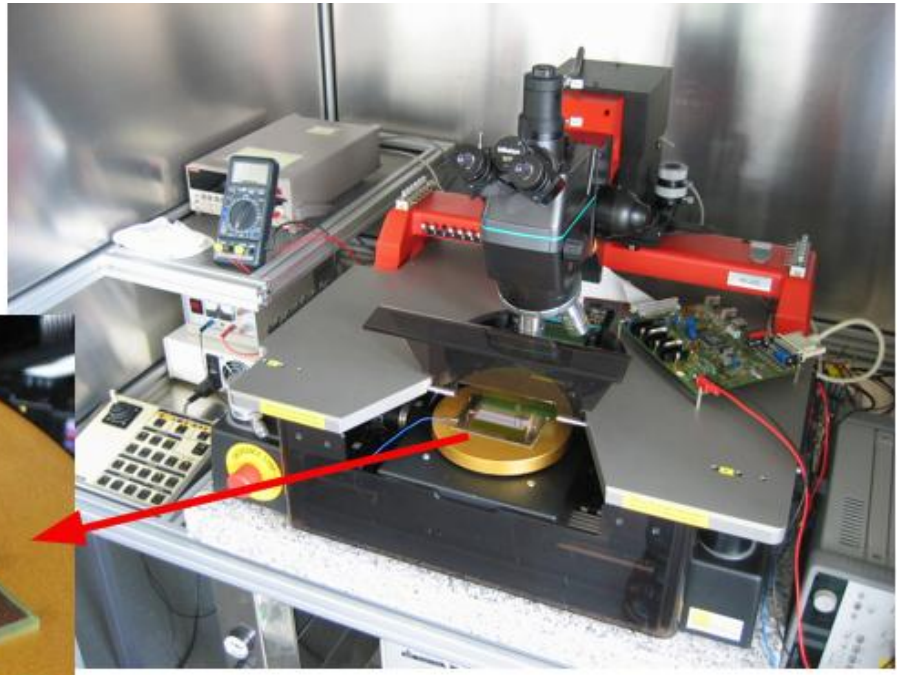
Alternative:

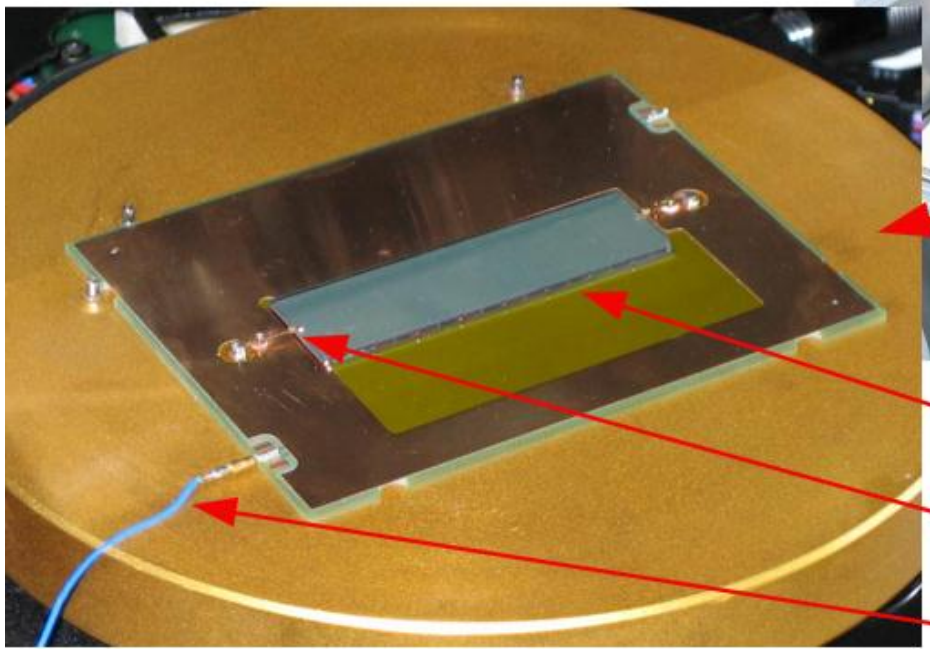
- Do it on flip chip bonder
- Chip is on bonding tool in well defined position anyway
- This step is important:
  - **Chip failure of the order of 1%** (was in the order of e few %) **results in module failure of the order of 15%**
  - Only short functional test done (few seconds)
    - Current consumption
    - I^2C interface
    - Token
    - DAC for V_{ana}
    - Temperature sensor
    - LVDS levels
    - Analogue levels
    - “Pixel alive”



Bare module test

Wafer probe station





Bare module

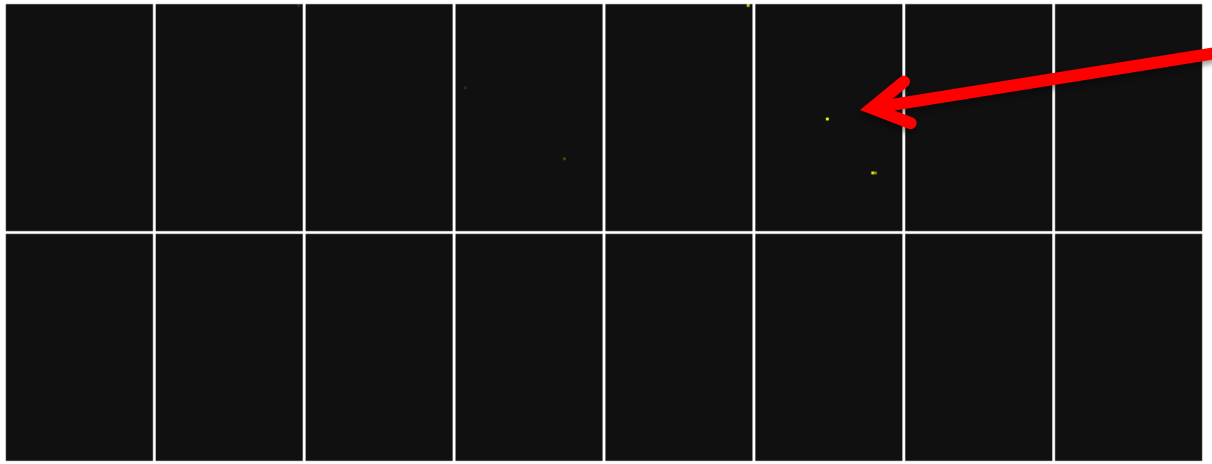
HV contact to sensor

HV connection

Bare module test

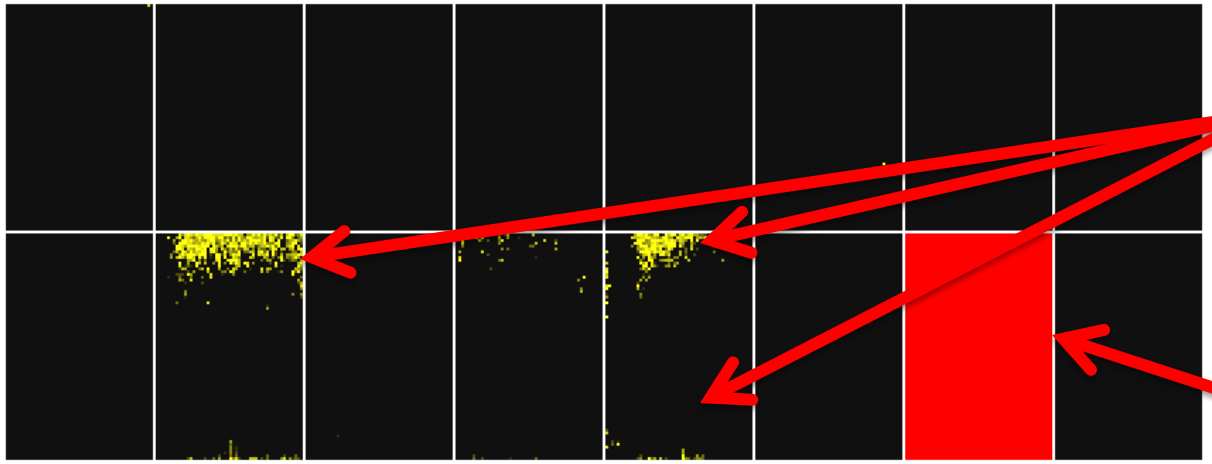
- Routinely made for **all bare modules** (time needed: ~15 minutes)
  - Test is “dangerous”: there is some chance to either damage the module or the probe card (**only use experienced staff**)
- Very fast feedback to bumping / bonding process (**same day** in our case)
  - **Processes are never stable**. Do not expect that once you made it through the learning curve, you will only produce good bare modules. It happed several times that bare module yield basically went to zero. We stopped immediately stopped production and investigated the cause
  - A **fast feedback** will save you a lot of money
  - Ideally this should be done at the **bump bond vendors place**
- **Tests done:**
  - Sensor IV curve (failure rate ~5%)
  - Basic ROC functionality (failure rate ~2%, mostly shorts)
  - Bump yield (failure rate ~3%, here rework had highest success rate)
- Last stage where module can be reworked
  - Rework can be done successfully
  - PSI: ~80% success for selected modules (IZM did it routinely for ATLAS modules)
- Components still needed to finish module (HDI, signal cables, base strips) are substantial contribution to budget
- **FPIX:** Did not test diced ROCs and did only IV test of bare modules
  - Less ROCs per bare module →higher yield of bare modules
  - Rework was possible after wire bonding

Test result



Good module

Very few isolated pixels. No concern, some might even be ok (test is not 100% reliable on pixel by pixel basis). Test will be improved in new ROC



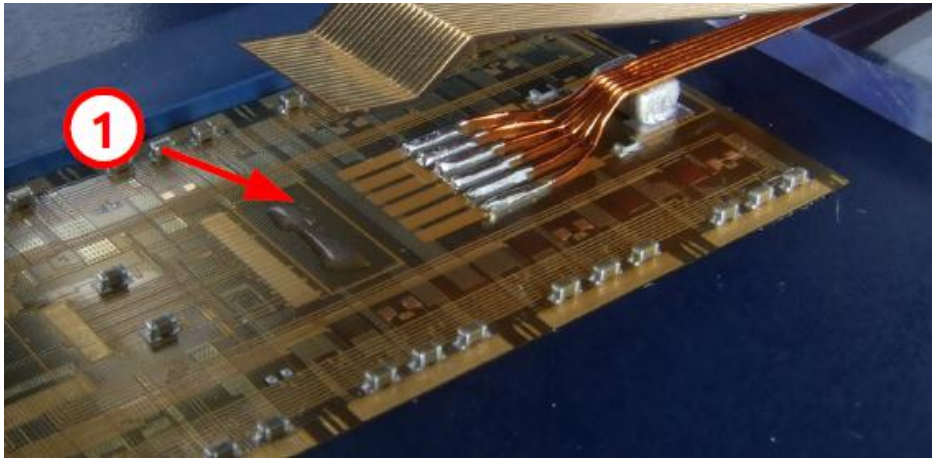
Bad module

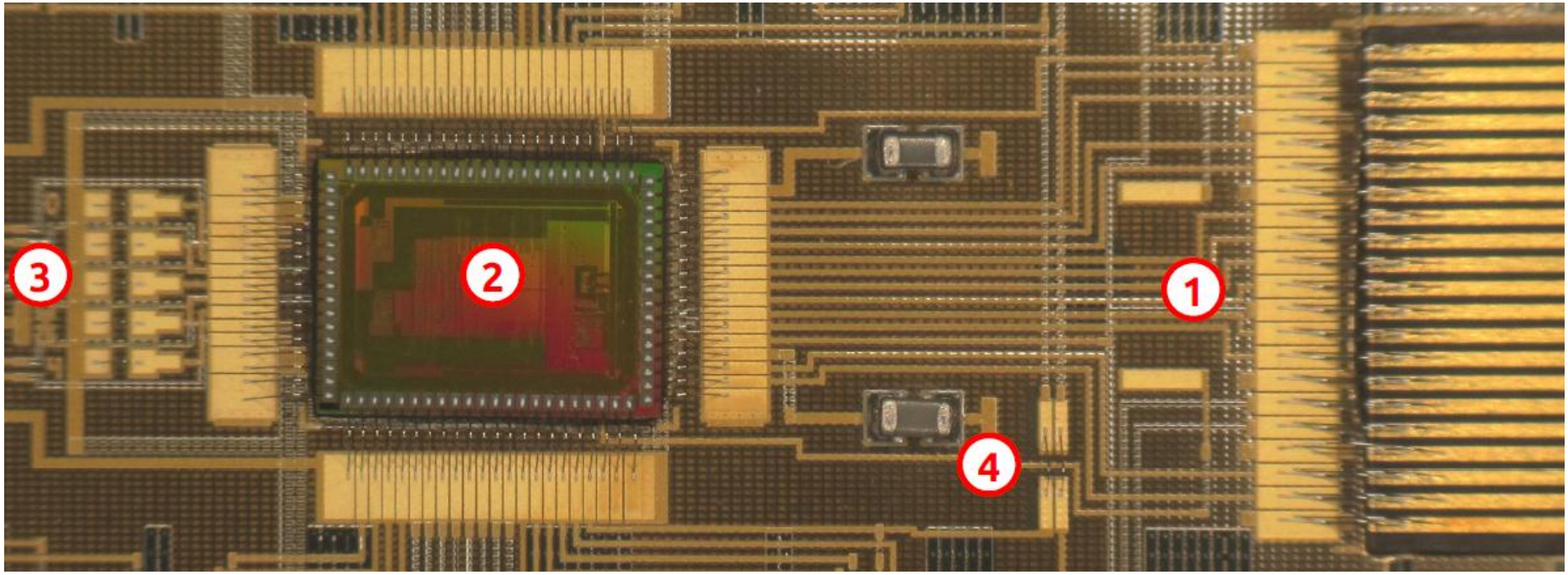
Bump bonding defects
You are only worried if they come in regions

Power short in ROC: not testable

Wire bonding of the HDI

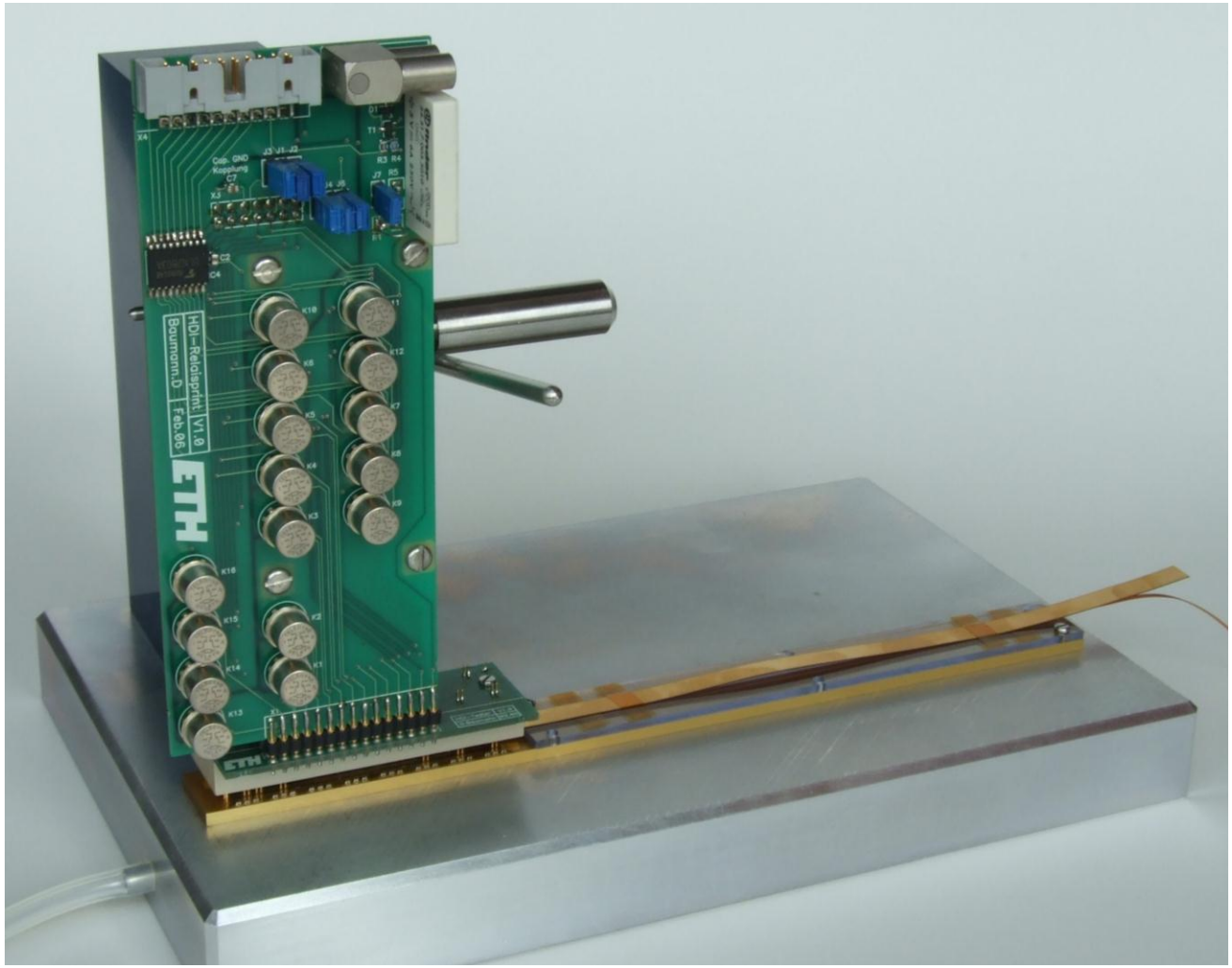
1. Wire bonding of **signal cable** (3 wires/signal)
   - Surface of the signal cable critical
   - Readjustment of parameters needed
2. Wire bonding of **TBM**.
3. Wire bonding of all **address lines** (5x).
   - Some will be removed to define the module address
4. Wire bonding of **token** (2x) for testing purposes.
   - Will be removed after successful HDI Test.





Chip test on Test of HDI

- HDI with handle fixed on holder with vacuum
- Spring loaded pins of the HDI-probe card connected to test pads
- Test checks
  - TBM
  - Most critical traces
  - HV
- After successful testing of HDI testing wire bonds need to be removed



Wire bond connection between HDI and bare module

1. Connection of sensor HV (3 wires)
2. Connection of ROCs (16 × 35 wires)

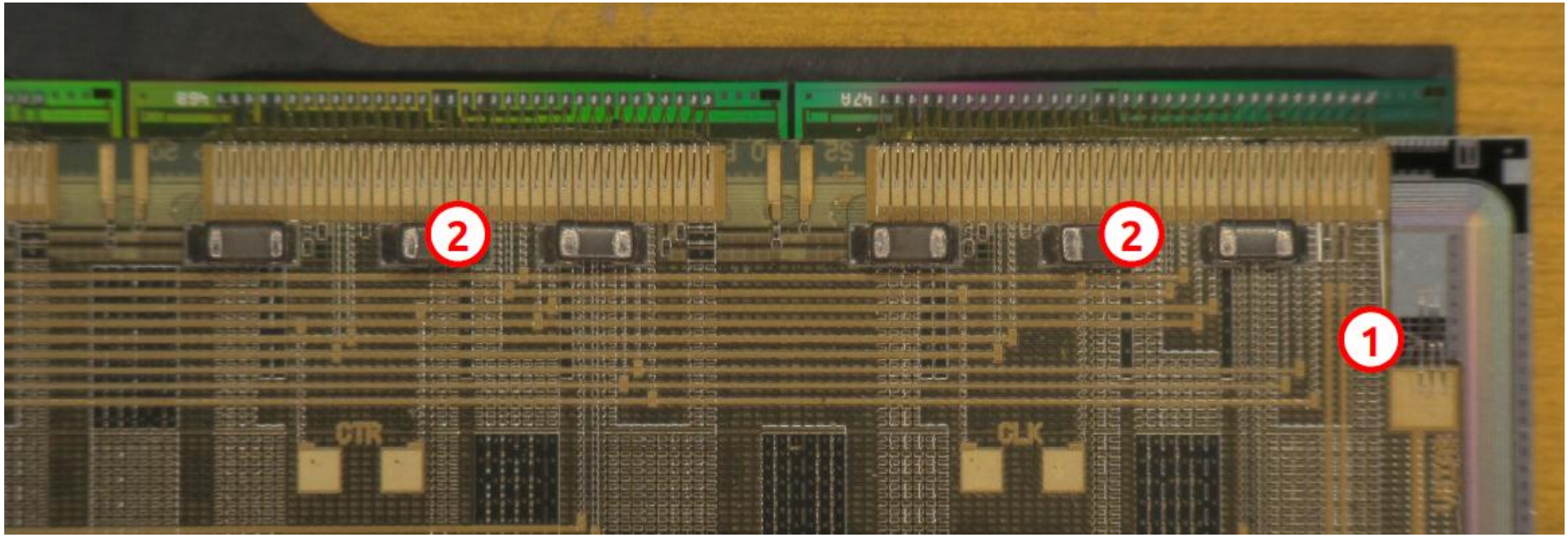
Problems

- Bond wire connection not stable at HDI
- Delamination of the pads
  - Specific to the process and the design
- Wire bonding of ROCs and sensor was never problematic

Measures

- Very careful optical inspection of the incoming HDIs
- Bonding tests with sample HDIs of each batch
- Not successful:
  - Additional cleaning of pads: Bond held, but became unstable after some time
- Some long term issues still not understood
- Understand better the technical limitations of the HDI vendor

FPIX: Automatic pull tests, potting of bonds (B-field)



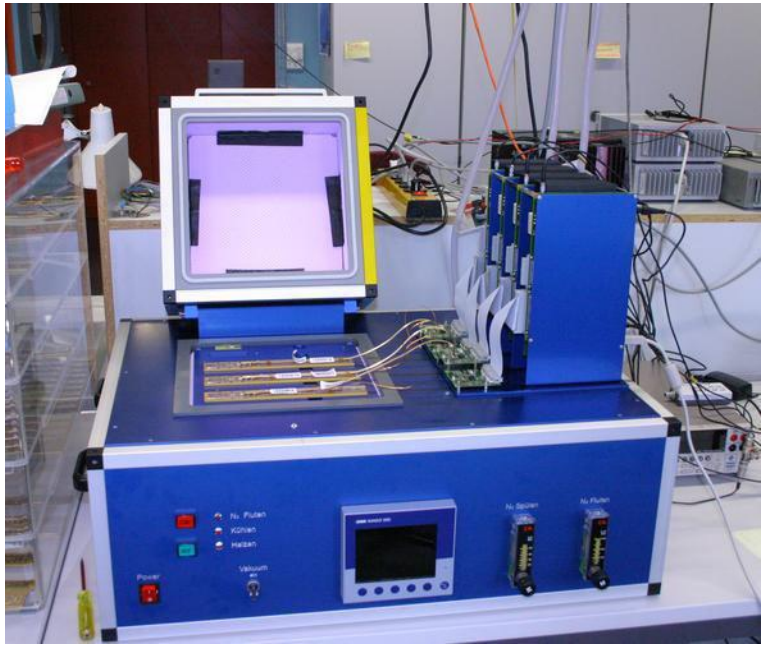
Final module test and calibration

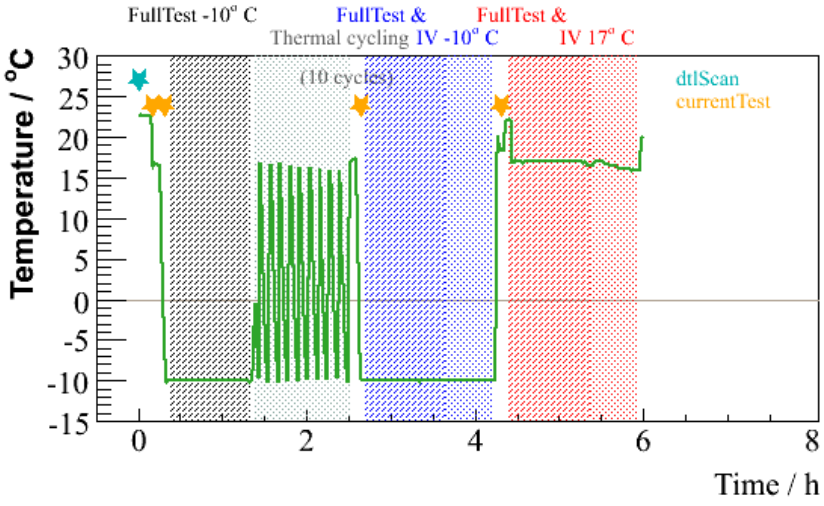
Acceptance test:

- Verify module functionality at T=+17C and -10C
  - Functionality (ex: pixel readout, trim bits)
  - Performance (ex: bump bonding)
  - Calibration (ex: trimming, T sensor)
- Thermal cycling
- Grading scheme: A (L1/L2), B(L2/L3), C (not used)
- Main challenges
  - Large number of channels (~67'000 per module)
  - Large parameter space (29 DACs per ROC)
- Test time: 6 hours for 4 modules in parallel
  - Done by a team of 2 scientists and 3 PhD students

Source Test

- Later it was decided to test each module with a source
  - Confirm it is a "particle detector"
  - Calibration of the internal Cal-injection capacitor
- Used a Americium-241 source with 3 targets: Mo(4844 e−), Ag(6139 e−), Ba (8906 e−)





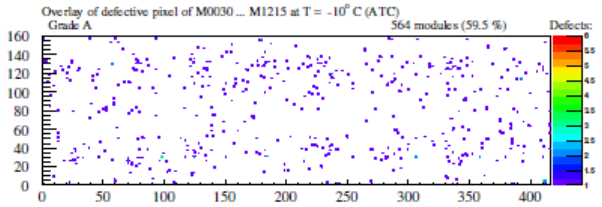
Summary of test

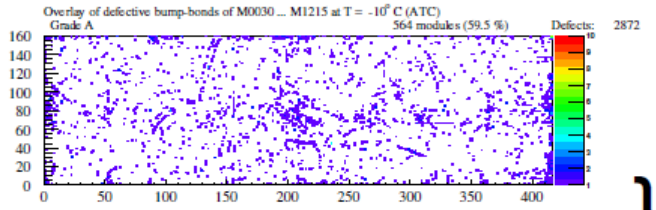
948 modules tested (827 full/ 121 half):

- 565/161 graded as A/B → 88% resp. 87/23 → 91%
- 101 graded as C → 12% resp. 11 → 9%

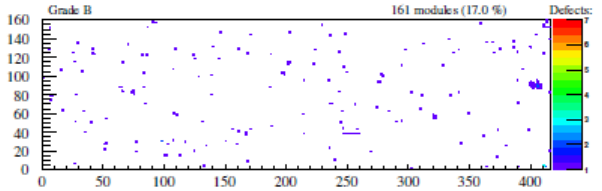
Overlay of modules tested at T = -10^{o} C (ATC)

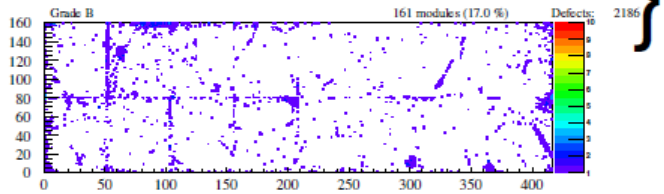
Final Grade A (564 modules)





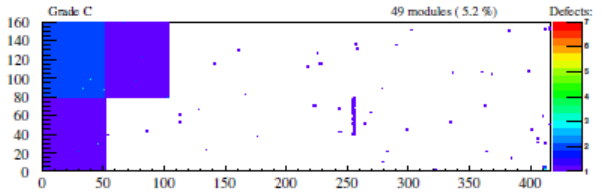
Final Grade B (161 modules)

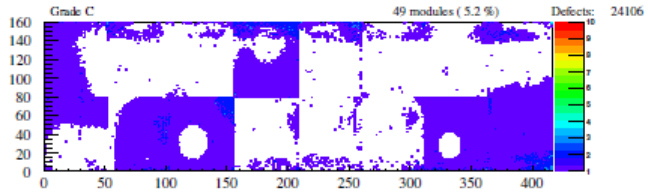




} 48.3M pixels

Final Grade C (49 modules)





3.3M pixels

Dead pixels

Dead bumps

Conclusions

Bump bonding

- Failures during bump deposition affect whole batches
  - Most can be detected with optical inspection (if one knows what to look for)
  - Some corrosion effects show up a bit (weeks) later
- Failures during the flip chip procedure
  - Damage the components
    - Functional tests of all components immediately before and after the procedure needed
  - Results in bad bump yield
  - Rework is possible but painful, try to avoid

Wire bonding

- Bond strength on HDIs is always an issue
- HDI production is difficult and has to be taken serious
  - Go to the limits of the design rules only if really needed. This will have implications on yield.

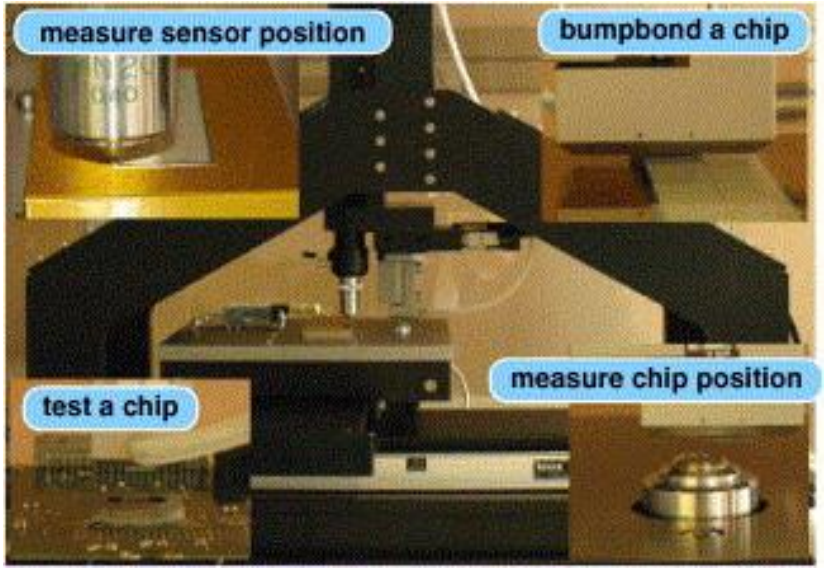
General

- Try to avoid multiple module geometries
- BPIX module production was a “small” project done with a small team (5 scientists, 2 technicians) of the people which have developed the process, no people were hired just for the production
- Those people informally met several times per week to discuss and adjust the procedures (no formal documents)
- **Very fast feedback of bare module test was very valuable**
- Simple and local database to keep track of all components is useful if batch-failures are detected later
- Testing and qualification of finished module needs a lot of resources (2 scientists and 3 PhD students)

Spare slides

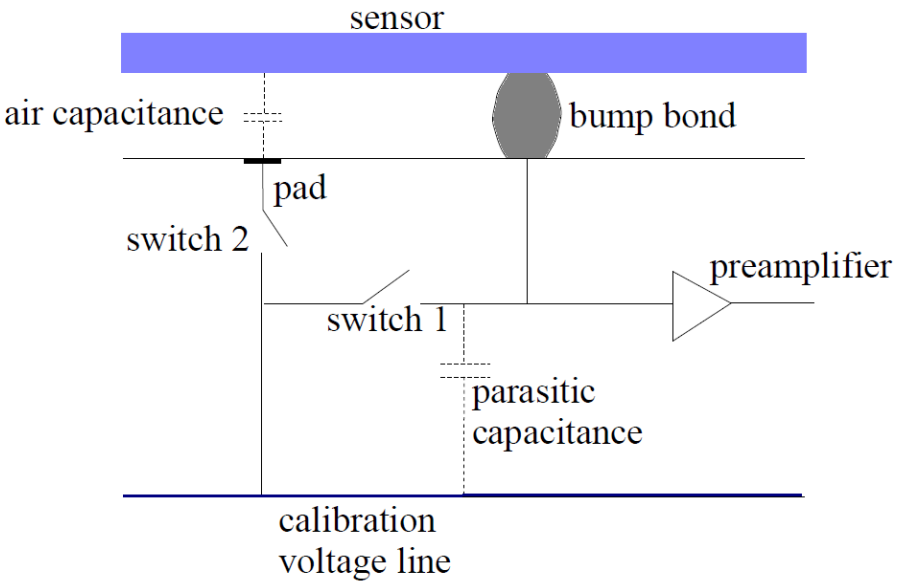
Chip placement machine

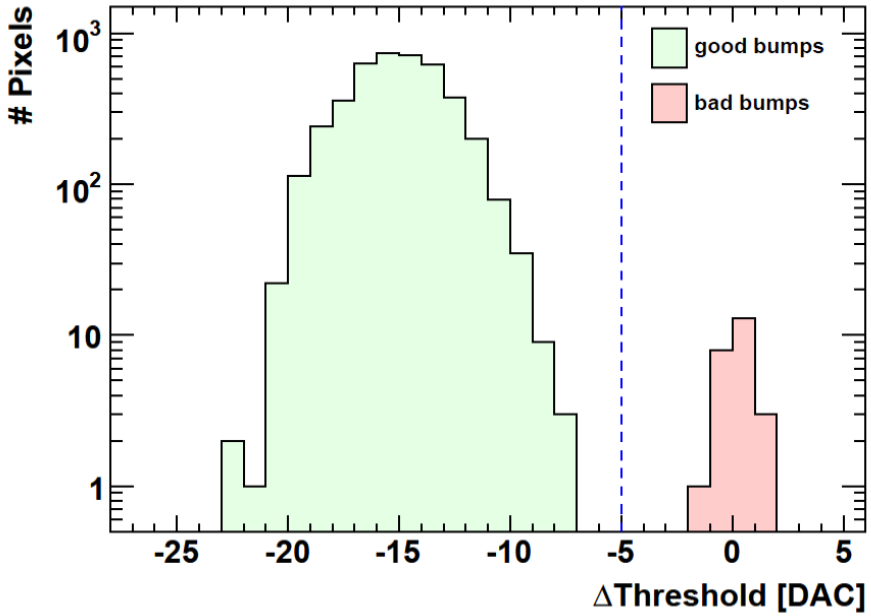
- Sensor position is measured with camera
- ROCs placed face down on a gel pack
  - Taken and measured with other camera
  - Pressed to probe card and tested
  - Spare chip is taken if test fails (a few % of the cases)
  - Pressed on sensor
- Process fully automatic
- Time ~ 45 min (incl. cleaning of ROCs and senosor)
- Throughput of more than 8 modules per day is not realistic



Test of bump connection

- Inject (rather high) signal via switch 2
  - Measure the threshold from which the pixel starts firing (S-curve, V_{thr} varied)
- Inject (rather high) signal with both switches open
  - Measure the threshold from which the pixel starts firing (S-curve, V_{thr} varied)
- If both S-curves are similar, the bump is missing
  - In some cases, cut is not so clean (some "high" ohmic connections)
- Next ROC iteration will have the parasitic capacitance removed and the 2nd step will not be necessary





Sensor concept and testability

Collect electrons (n-side readout)

- Less prone to trapping
- Larger Lorentz angle
- n-side isolation required

Avoid problems in module design

- N-Substrate (FPIX: 100-FZ, BPIX: 111-DOFZ)
- Guard rings (and junction) on back side
- All sensor edges on ground potential
- Double sided processing
  - Limits choice of producers
    - FPIX: Sintef
    - BPIX: CiS

Pixel call layout

- FPIX
  - Open p-stops, some over depletion needed to separate channels
  - large gaps, smaller C (value not yet measured)
- BPIX:
  - Moderated p-spray with bias grid (lower voltages, insensitive area)
  - Small gaps, homogenous drift field, higher C ~ 80fF