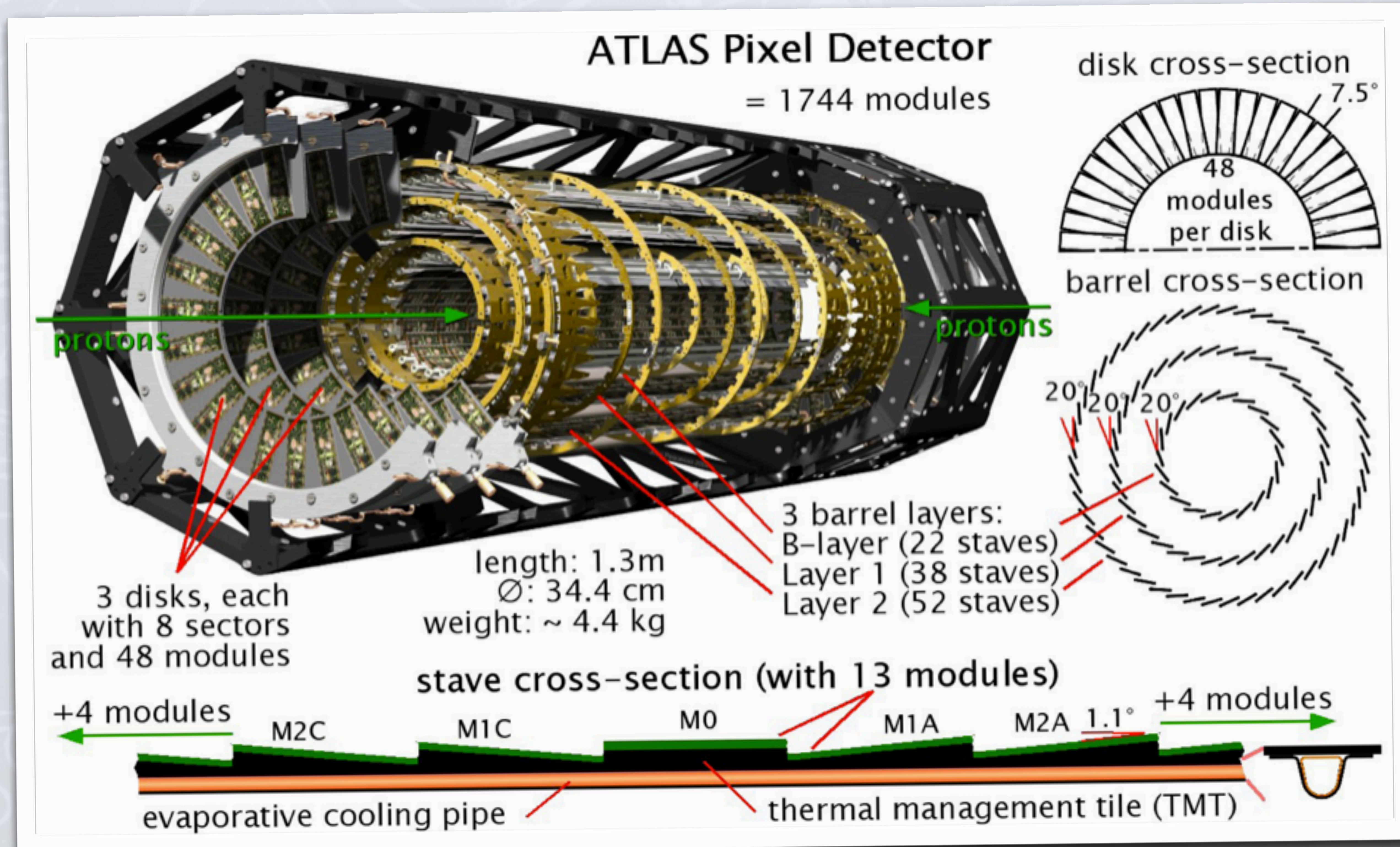
ATLAS Pixel Interconnects Issues

Workshop on Quality Issues in Current and Future Silicon Detectors
03 Nov. 2011
CERN

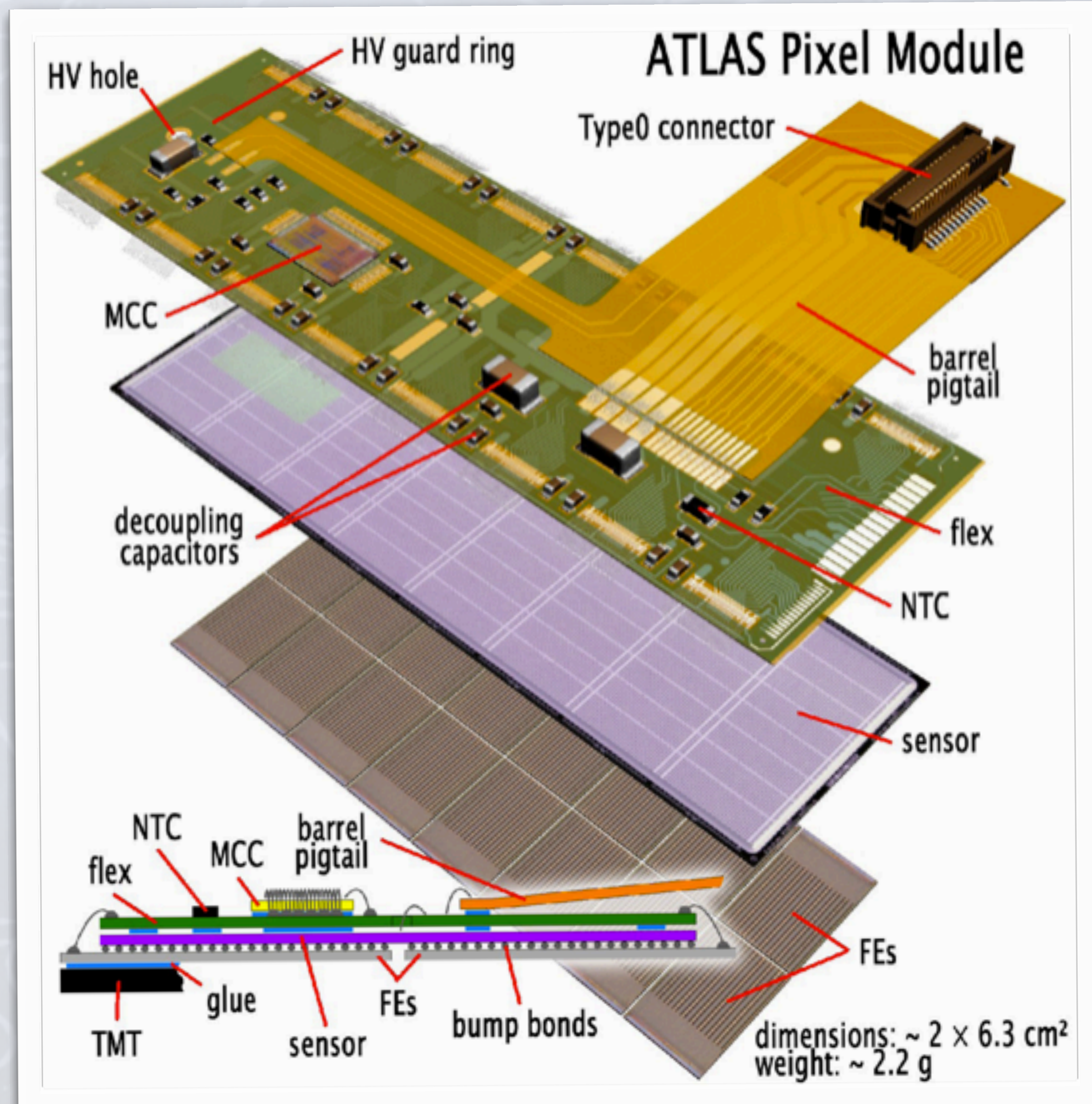
D. Dobos
on behalf of
ATLAS Pixel

Outline:
- ATLAS Pixel
- Bump Bonds
- Wire Bonds

ATLAS IN A NUTSHELL Pixel Detector

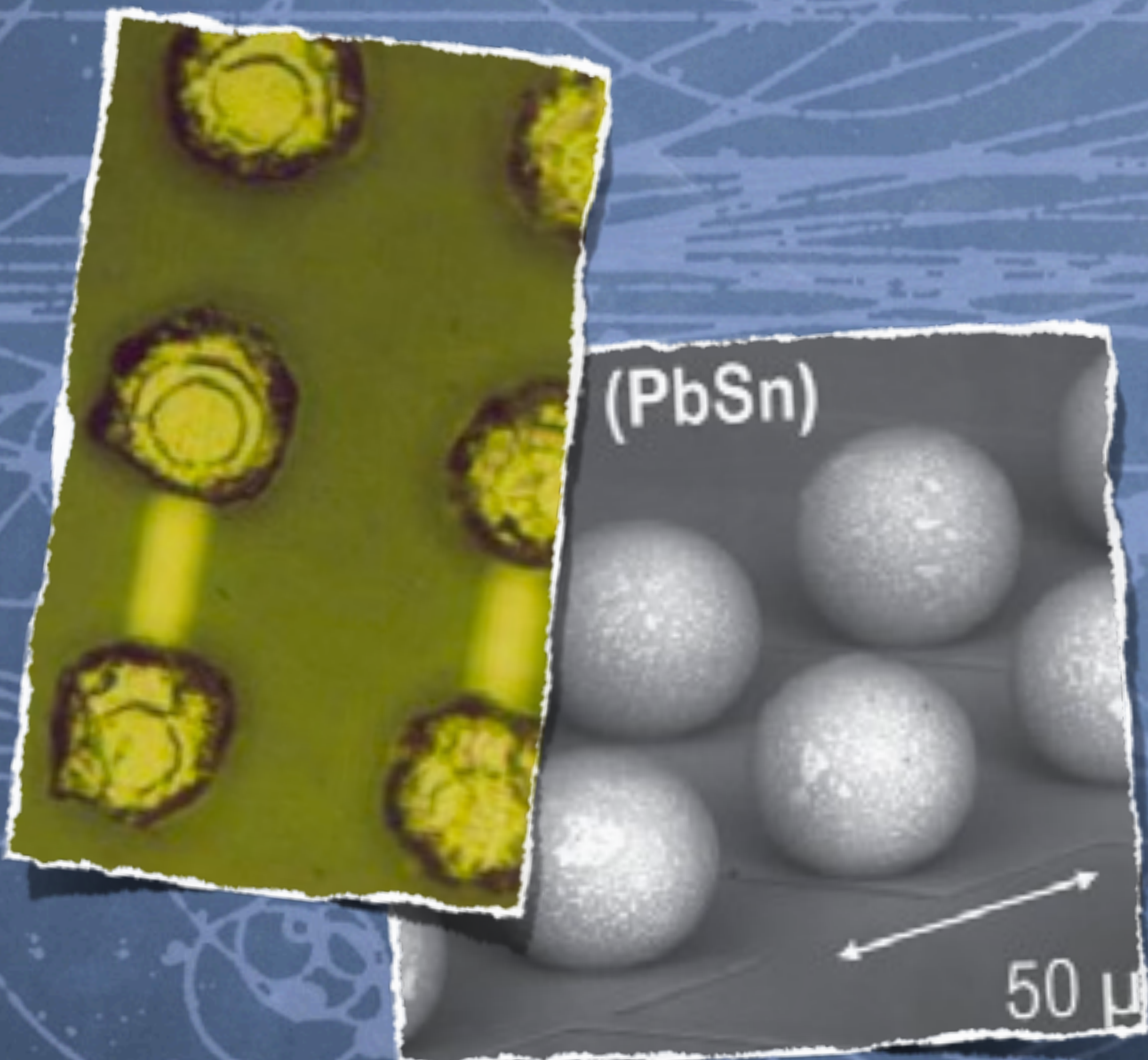


Pixel Module



Pixel Module:

- Planar n-in-n silicon sensor (n^+np^+), 250 µm thick, active area: 16.4 x 60.8 mm^2
- 16 FE-I3 readout chips, 180 µm thick, cover 7.2 x 10.8 mm^2 (2880 pixel cells) each, 3.5M transistors, 0.25 µm DSM technology
- Flexible circuit layer with Module Control Chip (MCC) and passive components



Bump Bonding

Pixel Bump Bonding Process IN 5 STEPS

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More than 46k electrical connections between sensor & 16 FEs:

- Connection density: ~ 4,800 cm^{-2}:
- Minimal pitch between two connections: 50 µm
- Only mechanical interface between the sensor and the FEs
- Challenging some years ago: high density, high yield, low pitch

1. Deposition of a Under Bump Metallization (UBM) on the sensor and FE wafer
2. Deposition of bumps either only on the FE wafer or on the FE and sensor wafer
3. Thinning of the FE wafer down to about 180 µm
4. Dicing of the sensor and FE wafers and selection of good components by probing
5. Flip chipping of FE chips to the sensor after precision alignment and formation of electrical and mechanical connection at appropriate temperature and pressure

Pixel Module Interchip Region

PIXEL TYPES

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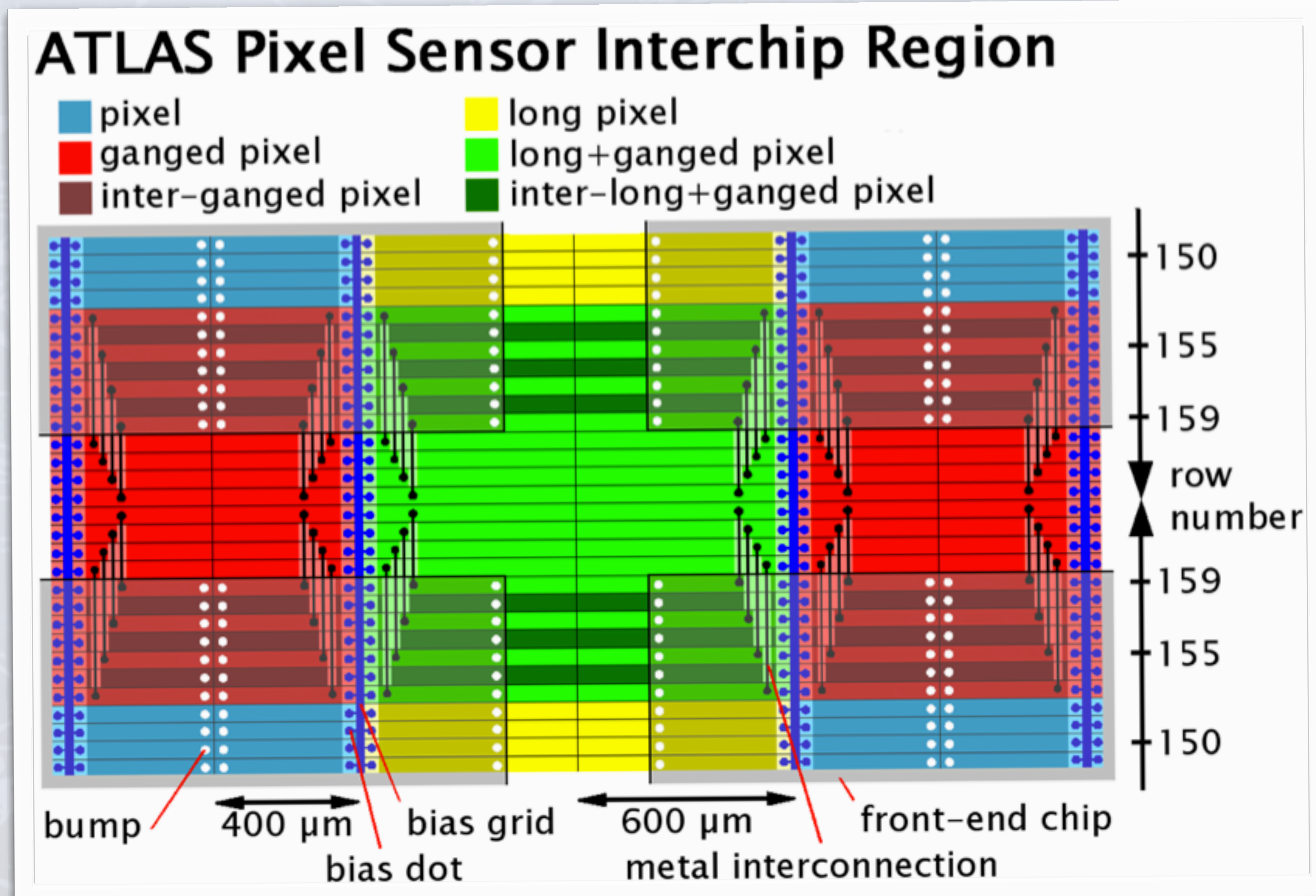
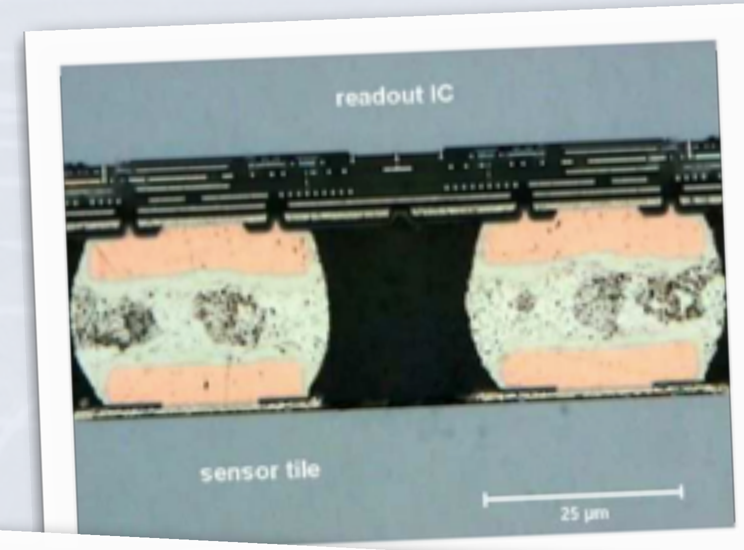
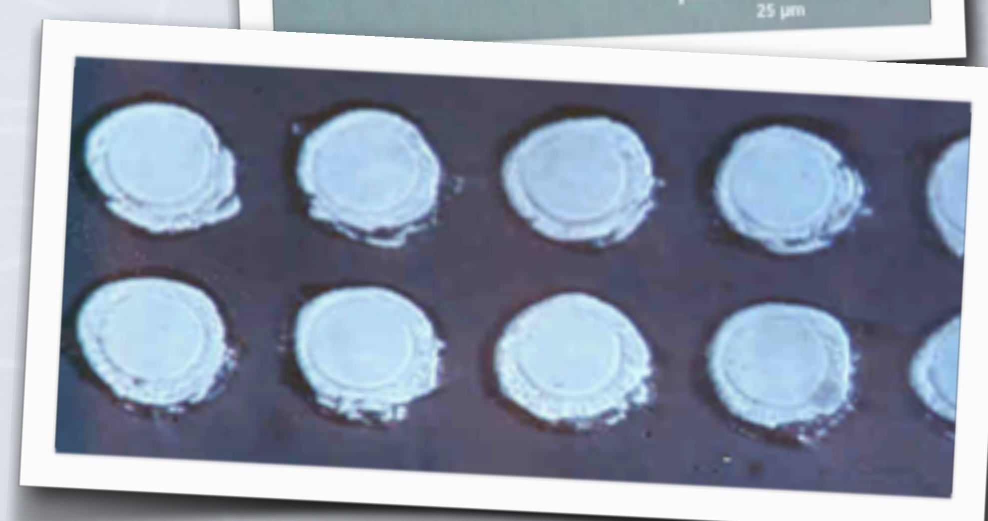


Pixel Bump Bonding Vendors AMS & IZM

To have a technical redundancy during development and to use multiple sources to fill the needed quantities, two different manufacturers of bare modules were used.



- IZM (Frauenhofer Institut für Zuverlässigkeit und Mikrointegration, Berlin, Germany) uses a bump bonding technique with solder bumps



- AMS (Alenia Marconi Systems, Roma, Italy) later SELEX uses indium bumps for the interconnections

Both manufacturers get the FE & sensor wafers provided with aluminum bump pads. Besides opening for bump pads, the rest of the wafer is covered with a SiO_2 and Si_3N_4 passivation layer.

Pixel Bump Bonding Process IN 5 STEPS

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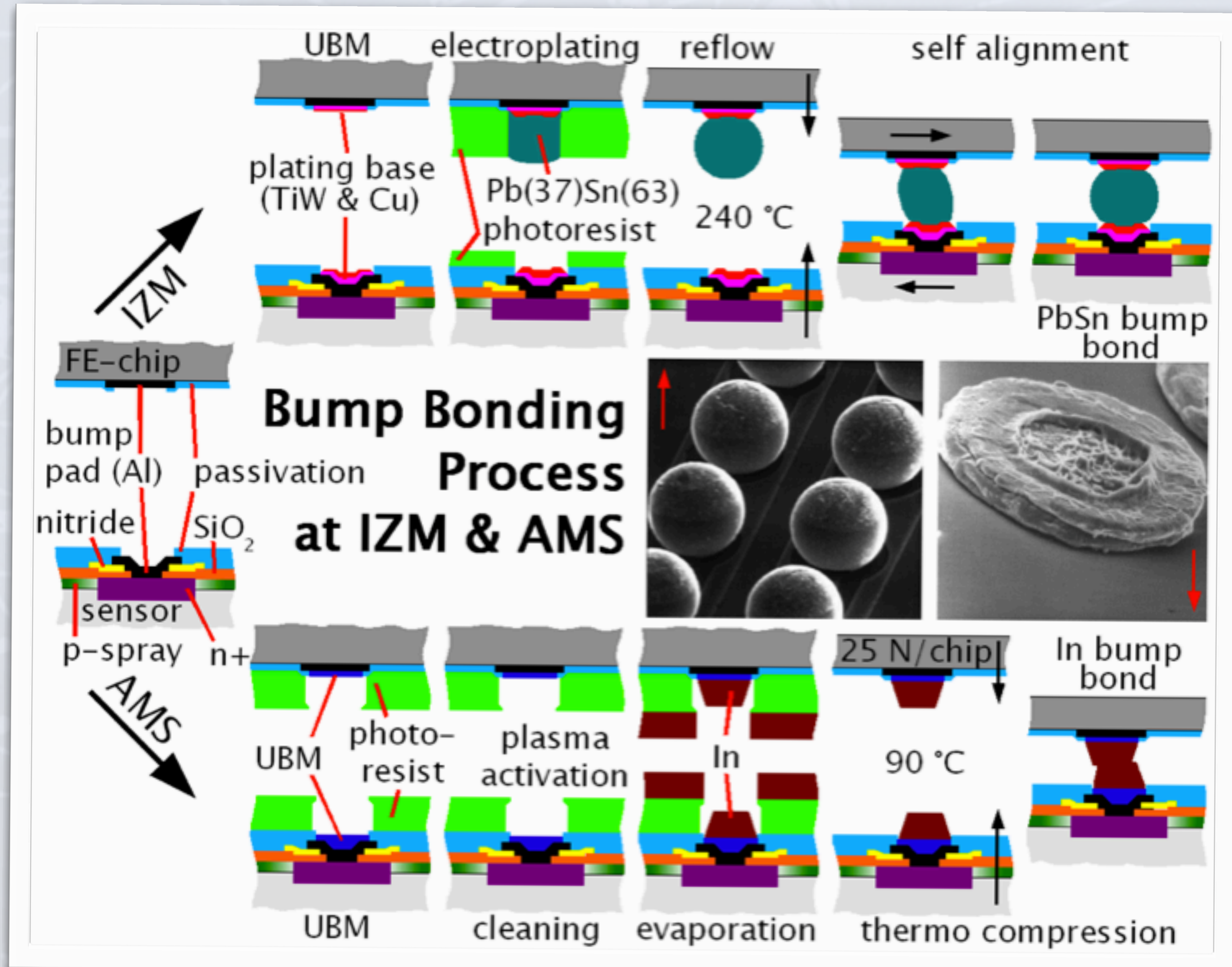

Solder Bumps & Indium Bumps

In & PbSn

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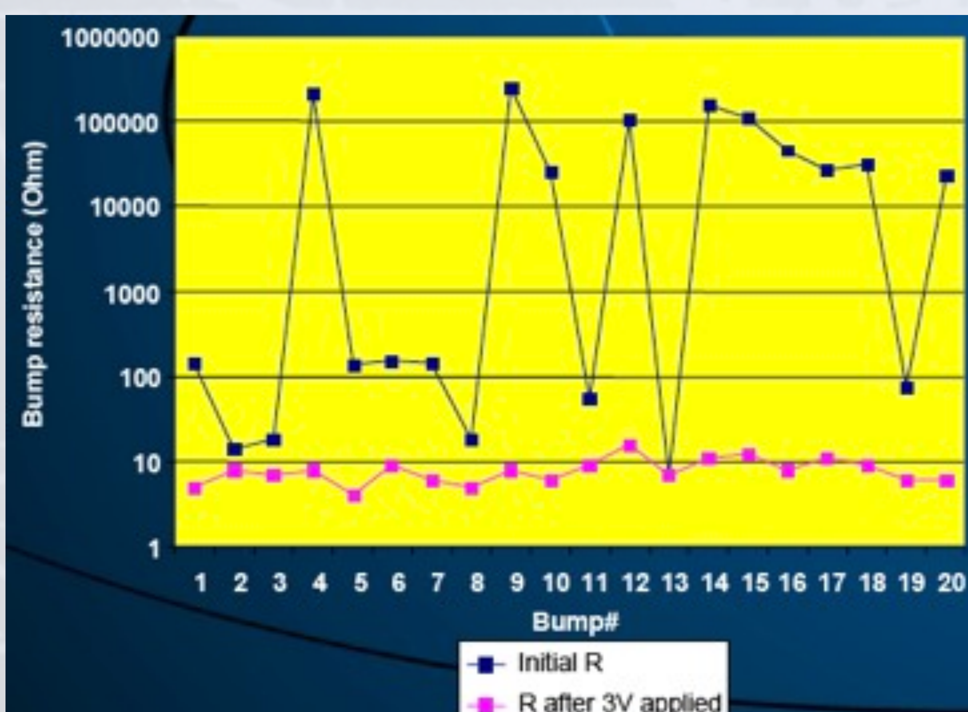
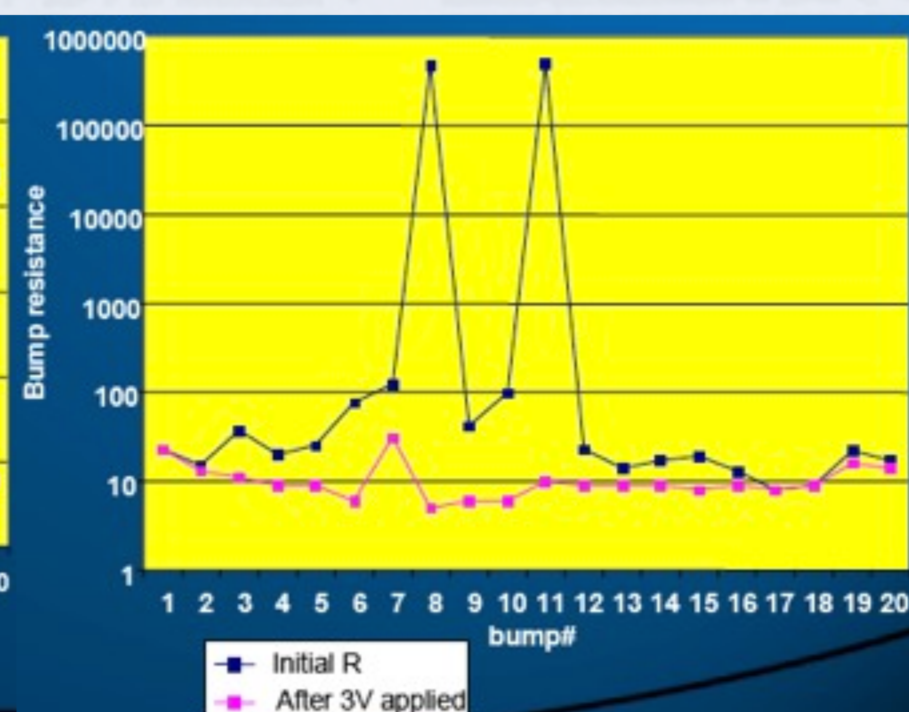
Advantage of indium bumps: lower flip-chip temperature

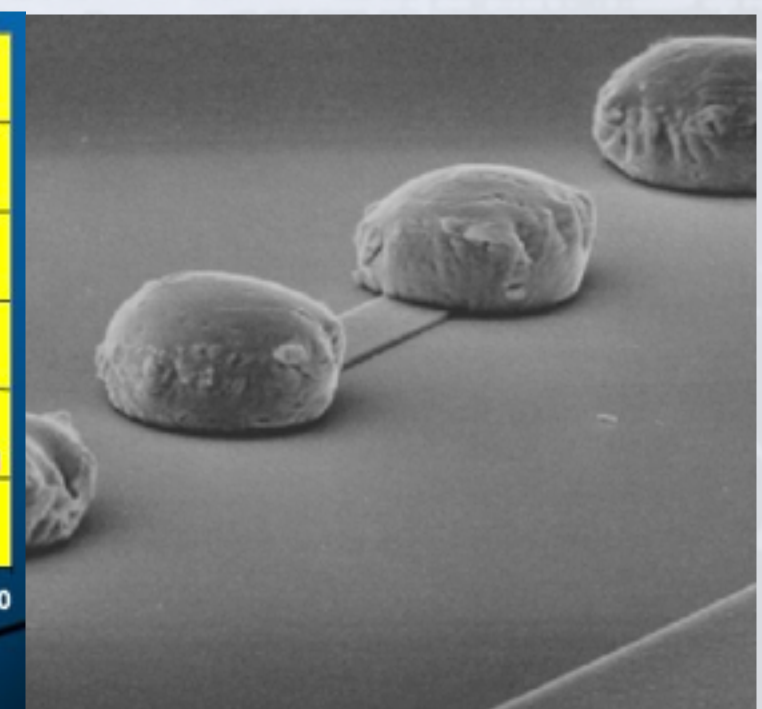
Significant difference is interconnection electrical resistance:

- Solder bumps have a constant resistance of about 0.5 Ω
- Indium bumps resistance ~10 Ω. Increase up to 500 kΩ observed on ~10% indium bumps. Caused by In_2O_3 oxidation layers on bumps - can be broken by applying a 3 V bias voltage to electronics.

Bump resistances have to be kept small to avoid a significant contribution to the FE preamplifier noise.







Quality Control

XRAY & ELECTRICAL

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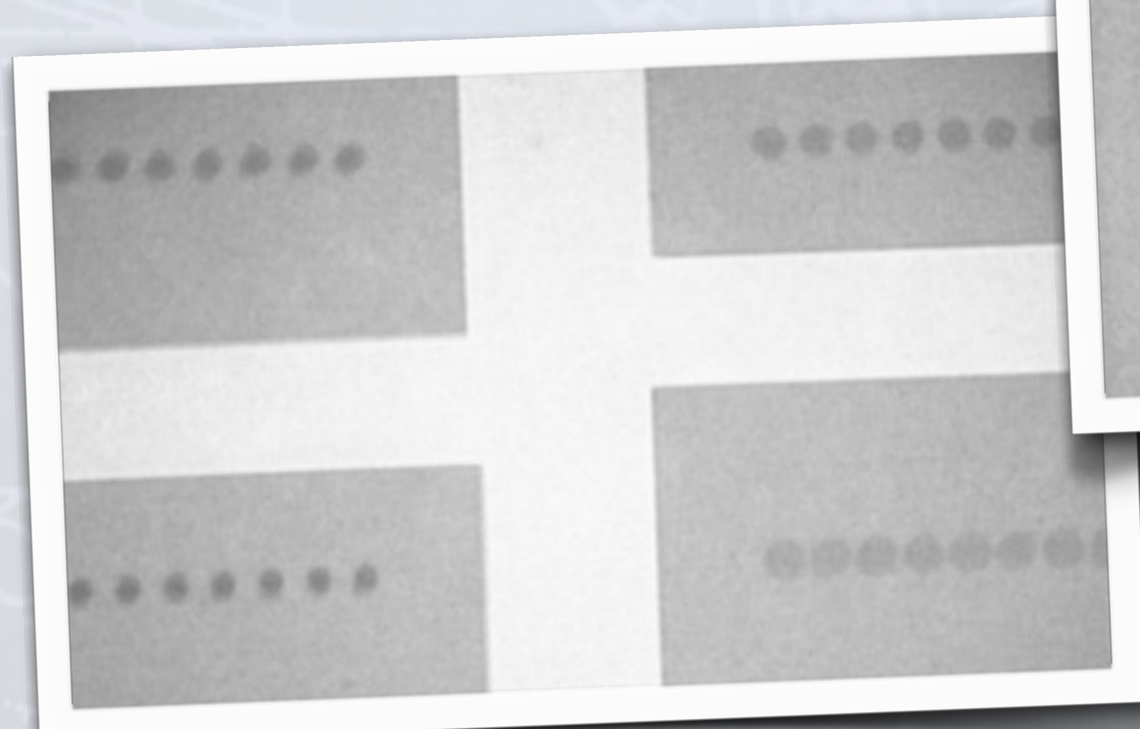
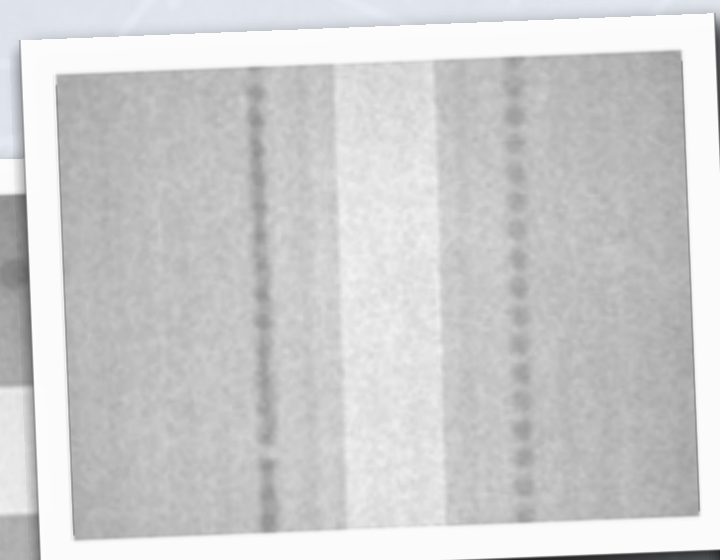
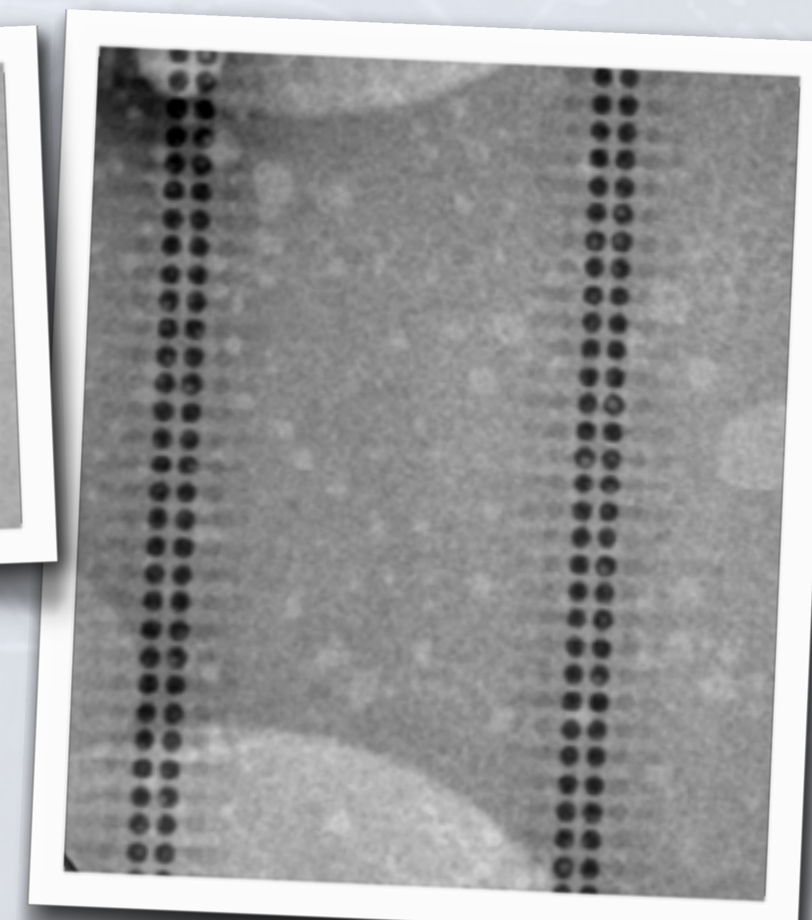
High resolution (2-5 µm) X-ray inspections with phosphor screen CCD system and pattern recognition used to detect merged and missing bumps. Results crosschecked with further electrical tests. FEs with bump defects (missing or merged bumps, residue between bumps, damaged FEs) can be reworked. Reworking FEs successfully demonstrated for both technologies.







Pixel Bump Bonding Vendors AMS & IZM

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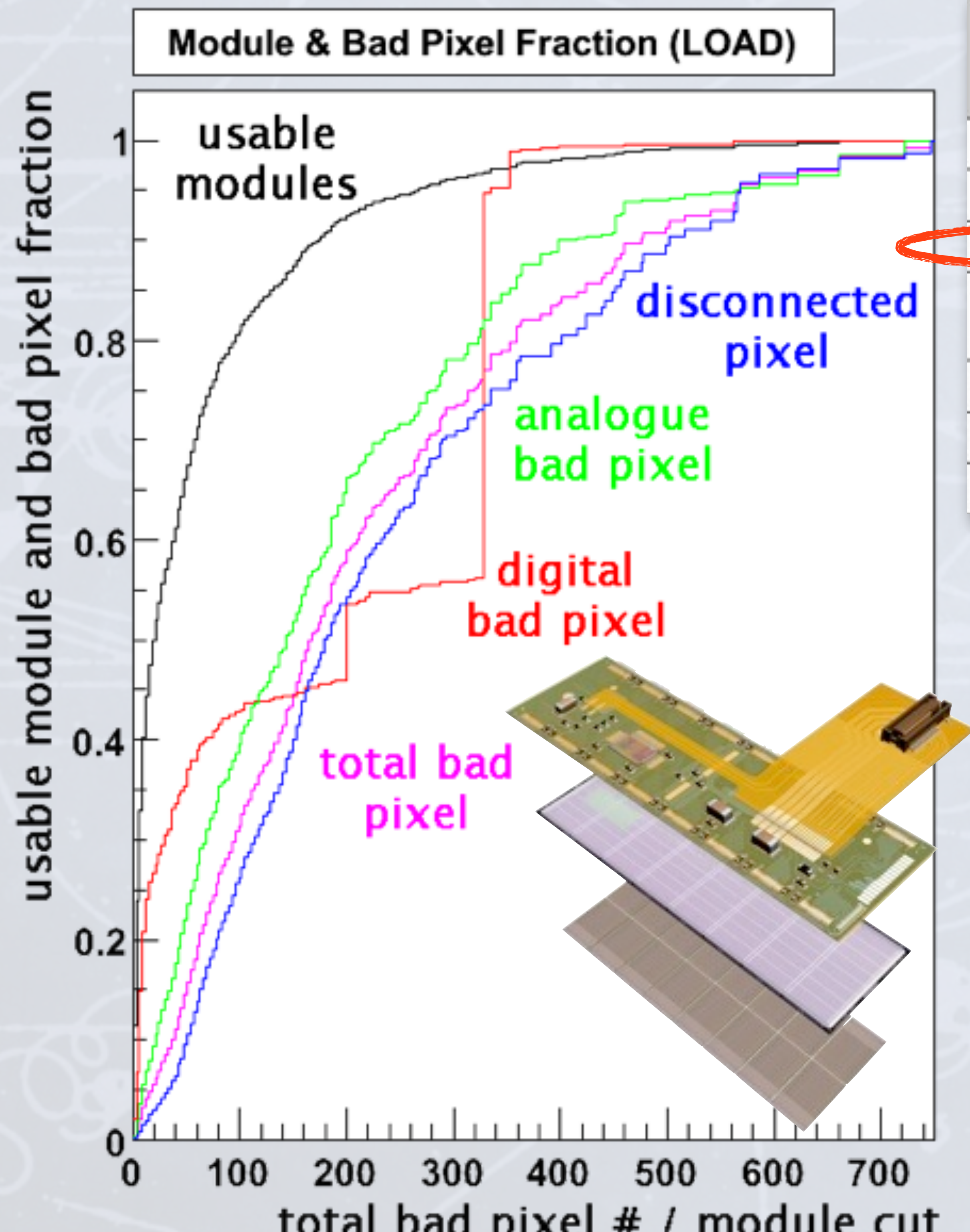

Bad pixel type:	*LOAD bad pixel amount (fraction):*	*BIST bad pixel amount (fraction):*	*LOAD total fraction:*	*BIST total fraction:*
digital injection	875 (0.9%)	1047 (1.0%)	0.013‰	0.016‰
analogue injection	36542 (36.9%)	40518 (37.1%)	0.54‰	0.60‰
disconnected	61618 (62.2%)	67760 (61.9%)	0.92‰	1.00‰
barrel sum (~67.1M pixel)	**99035**	**109325**	**1.5‰**	**1.6‰**
B-layer (~20%)	5105 (5.2%)	5033 (4.6%)	0.39‰	0.38‰
Layer-1 (~34%)	32371 (32.7%)	36850 (33.7%)	1.42‰	1.62‰
Layer-2 (~46%)	61559 (62.1%)	67442 (61.7%)	1.98%	2.17‰

- Disconnected bumps is main reason (~1‰) for bad pixels
- Can affect mechanical connection stability - can provoke additional disconnected pixels - increase for modules with a contiguous region of disconnected pixels is expected with mechanical stress, thermal cycling, ...

Disconnected Pixels WORST MODULE

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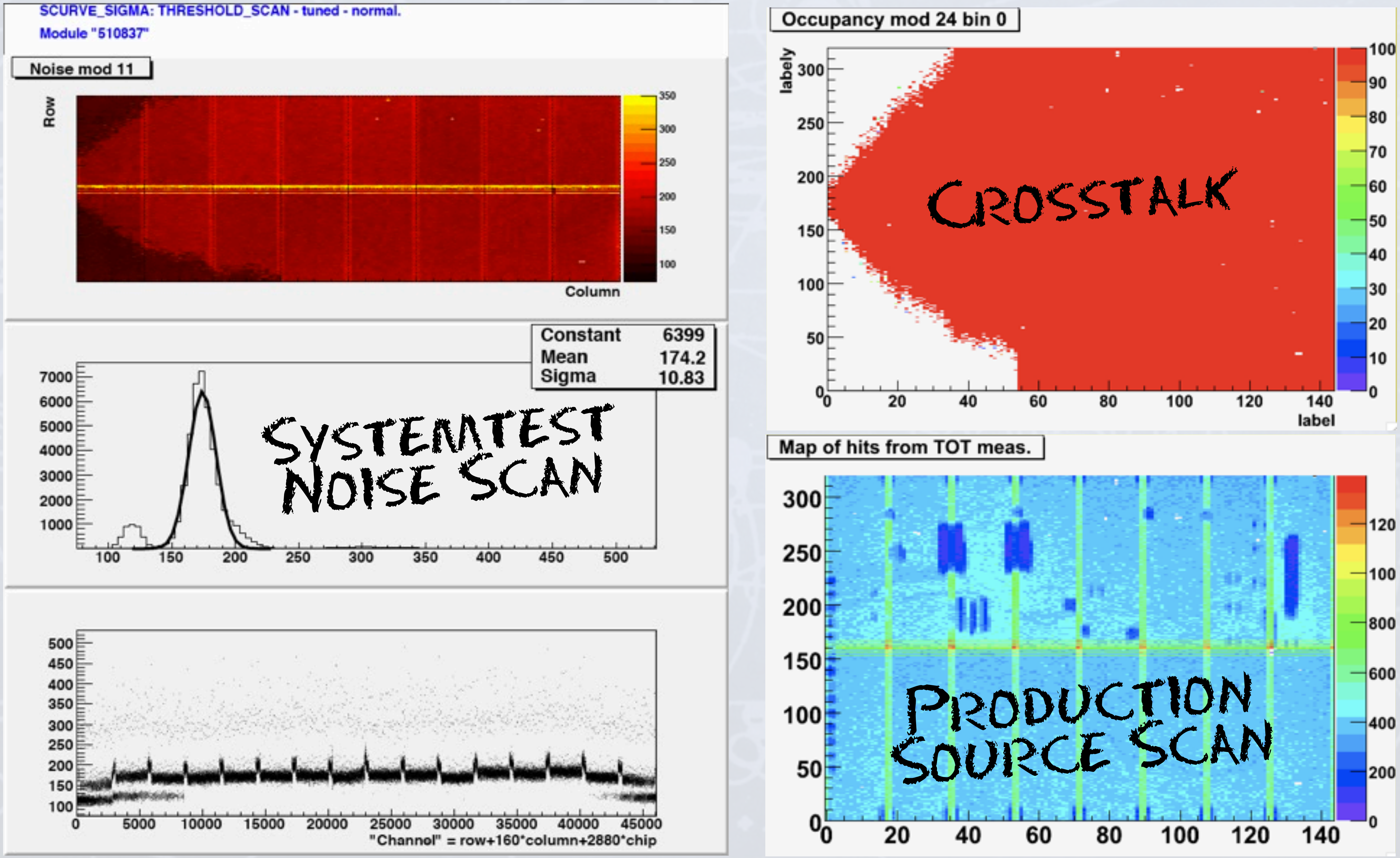

Dead Pixel Maps Offline Analysis

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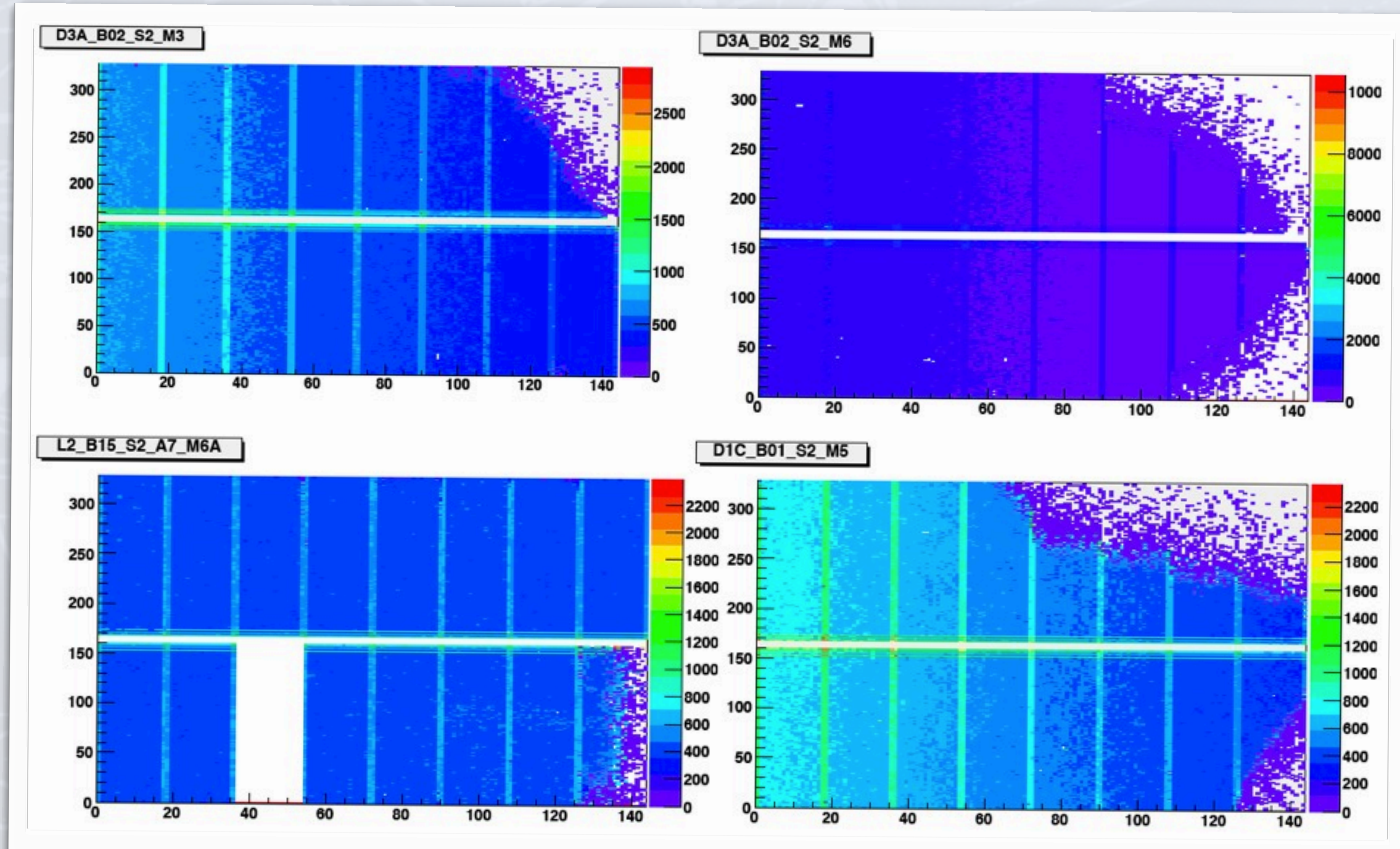

Disconnected Pixel Measurement
CROSSTALK SCAN

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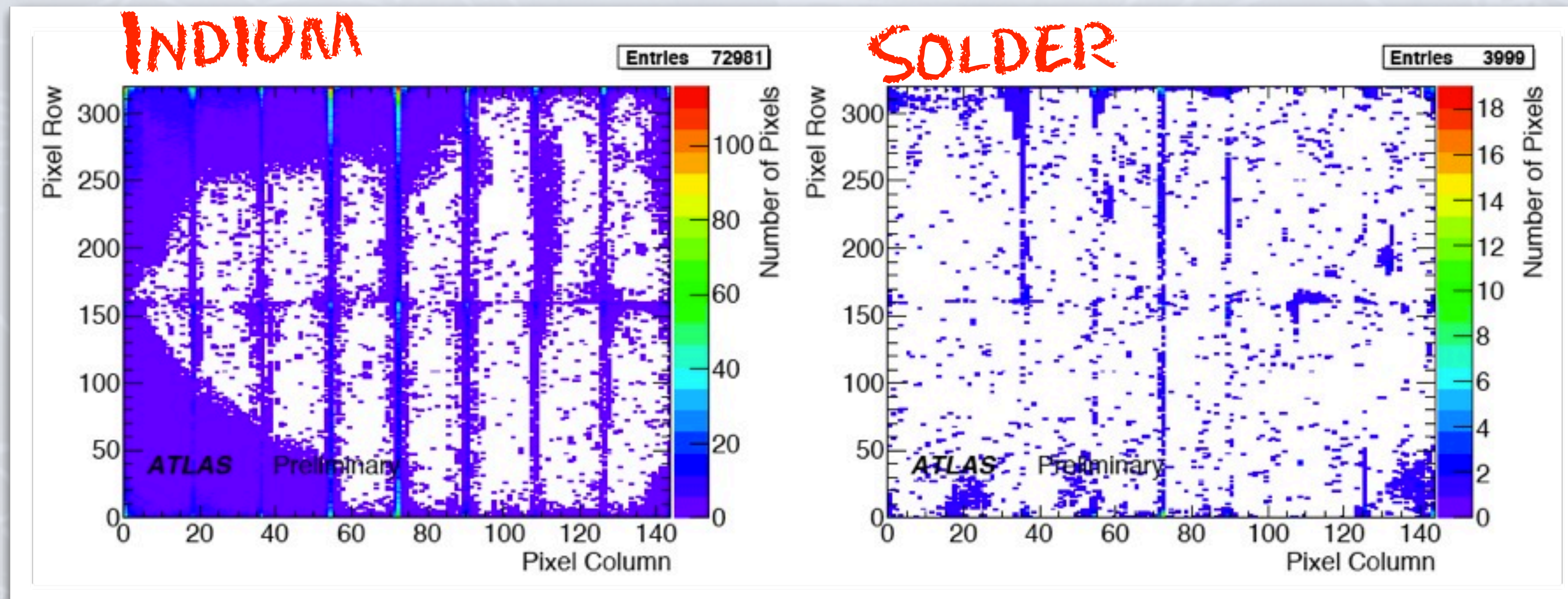
- Used crosstalk scan (4 ke^- threshold 200 ke^- injection)
- Sensor crosstalk 3.5%, low cross-talk in electronics (shielding)
- Analogue and threshold scan (noise: $160e^-$ -> $120e^-$) verification
- 76980 disconnected pixels (0.1%) in 1697 modules
- 94.8% of total disconnected bumps are Indium type bumps
- Larger connected areas are from few badly damaged modules



Disconnected Pixel Measurement

Crosstalk Scan

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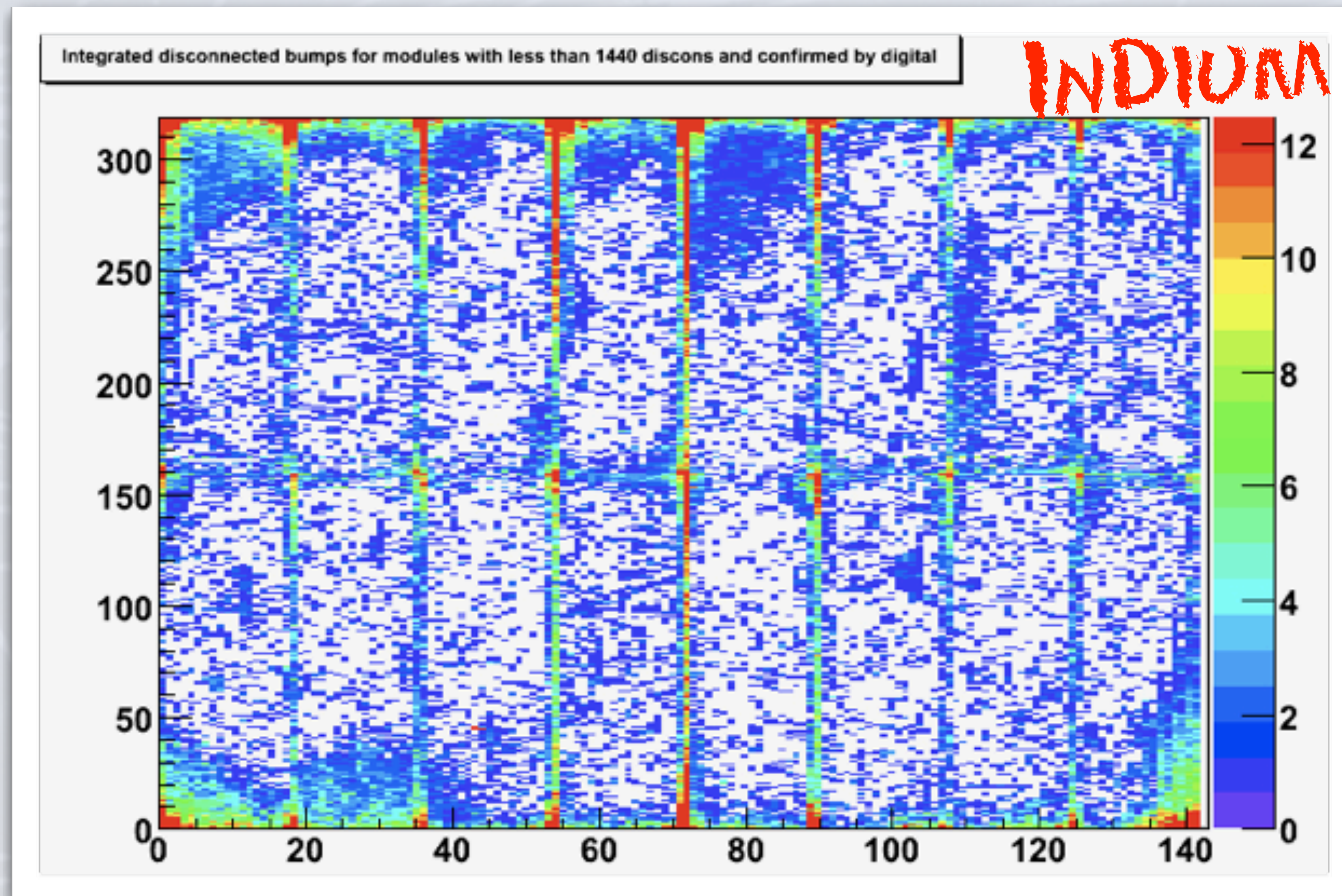
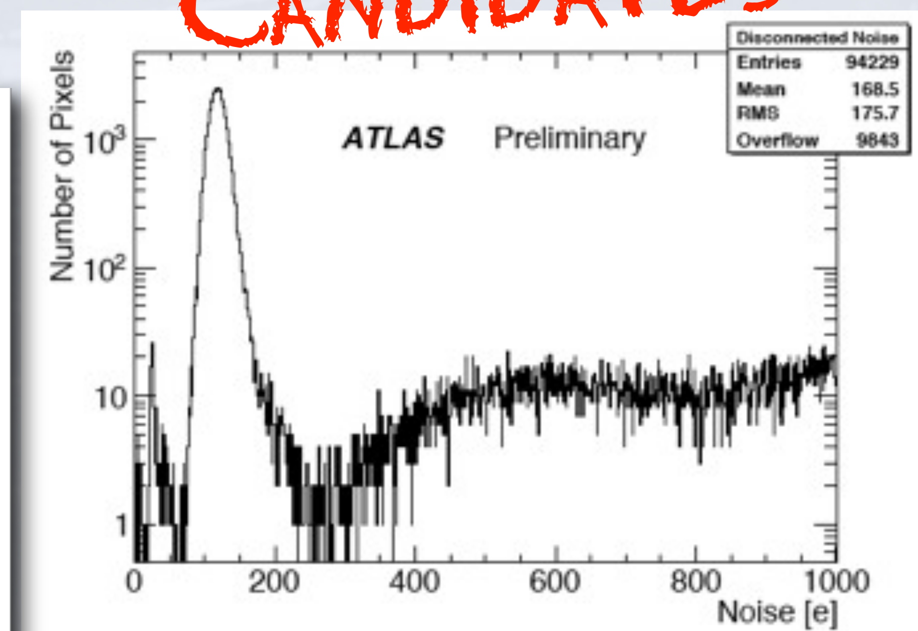
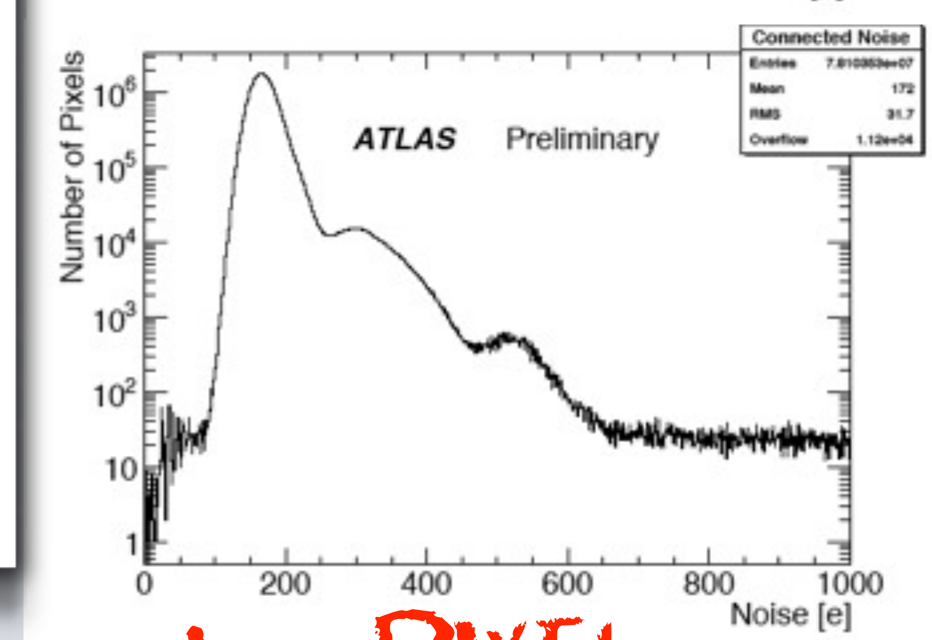
Indium



Disconnect Candidates





All Pixel

Observed Problems SOLDER BUMPS

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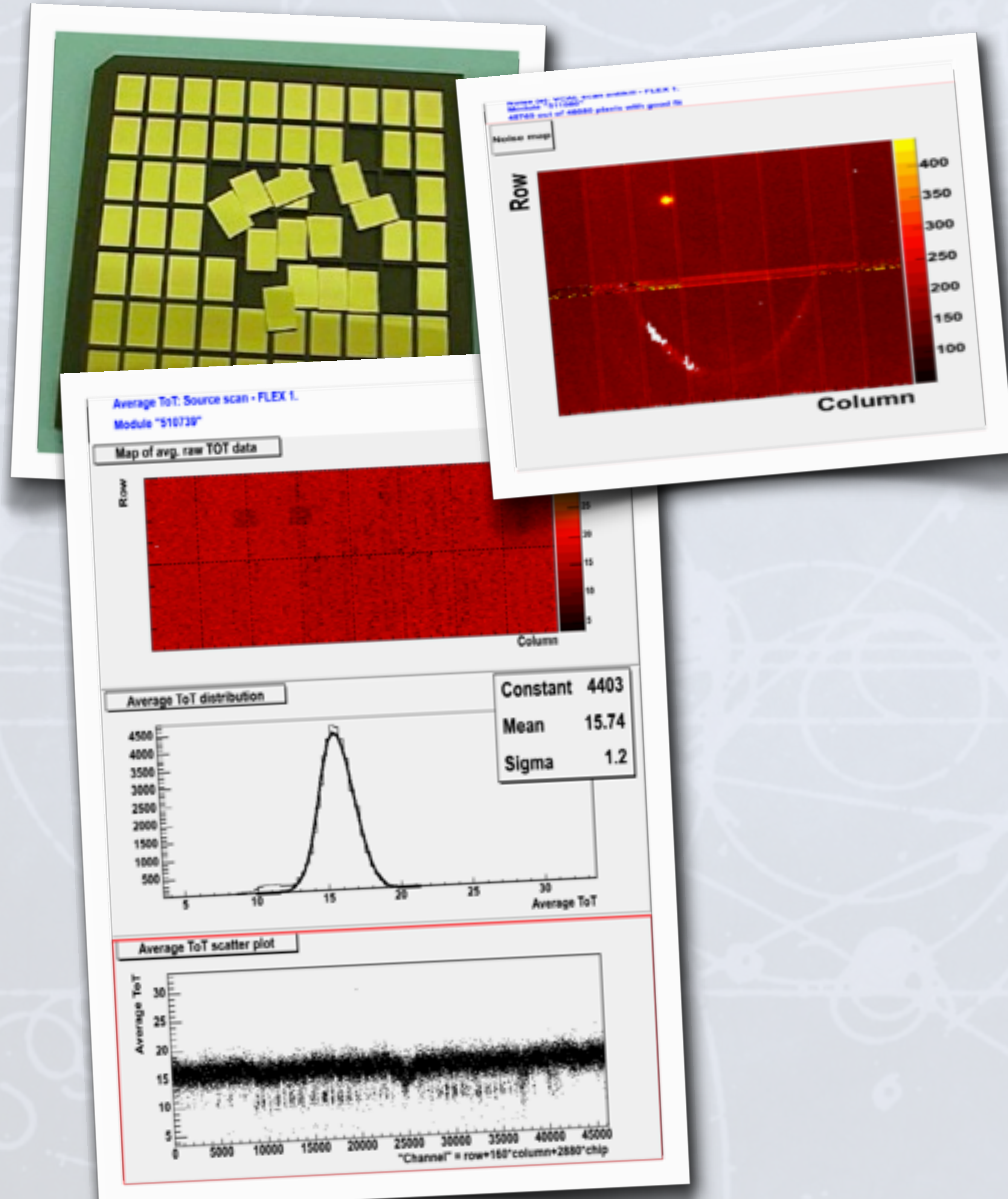

- Contamination with particles (from dicing) shorts on chips and on sensor

FE :

- Gelpack remnants & difficult handling
- vacuum tweezer accident
- Over-thinning (only initially)

Sensor:

- Poor passivation openings
- Sensor Dicing problems

Observed after assembly:

- Low-ToT pixels: problem after UBM recycling
- Noise hot spots + high Ileak

Observed Problems INDIUM BUMPS

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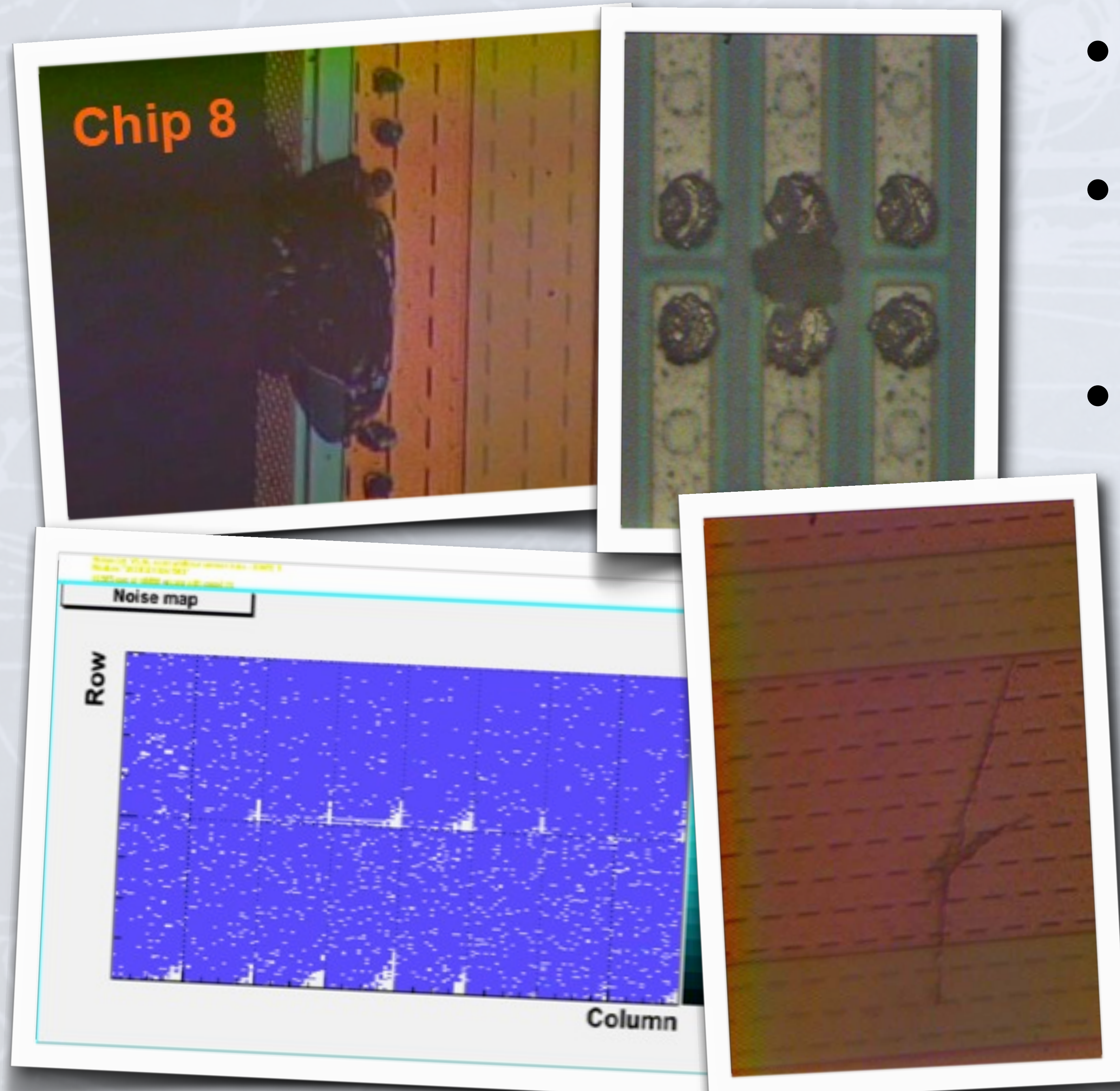

- VDDA shorts, cleaning procedure
- Silicon fragments sandwiched between sensor and FE
- Care in cleanliness and handling, inspection
    - Broken pickup tool: springs to distribute pressure along the FE
    - Damage to the electronics, problem with the manipulation procedure

Production Yields 2576 MODULES

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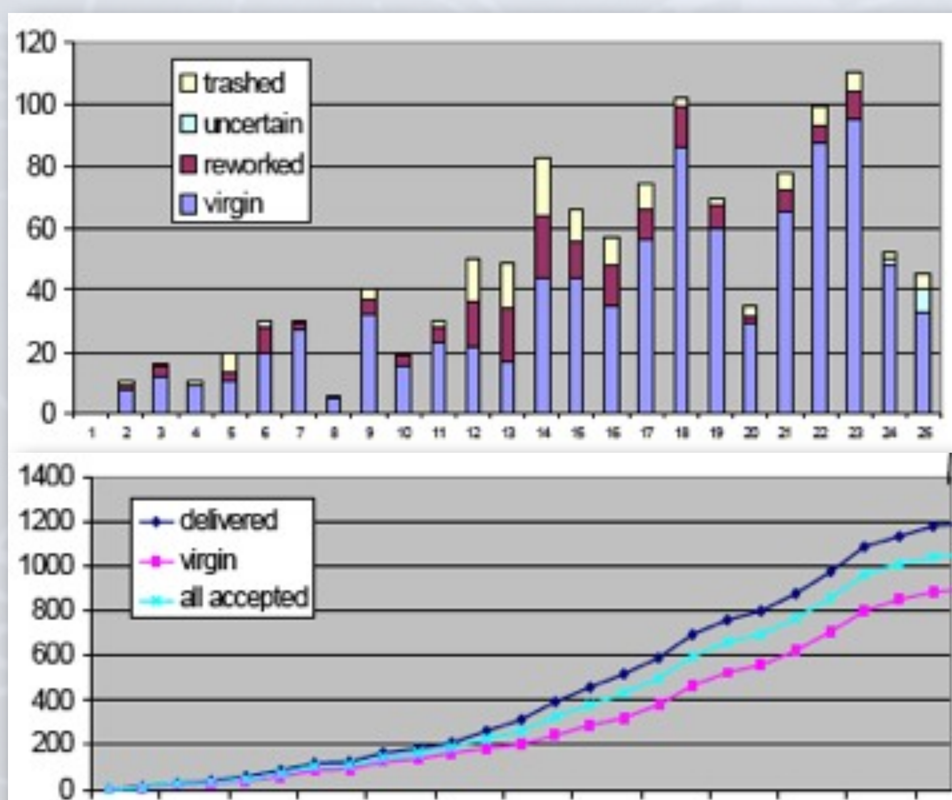
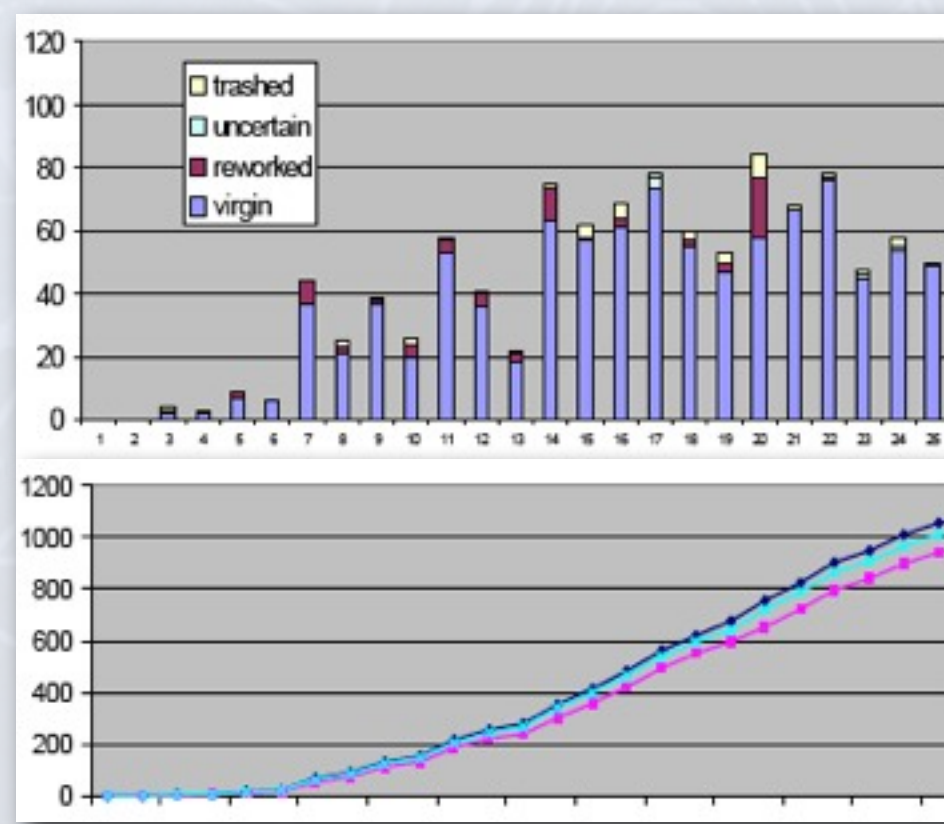
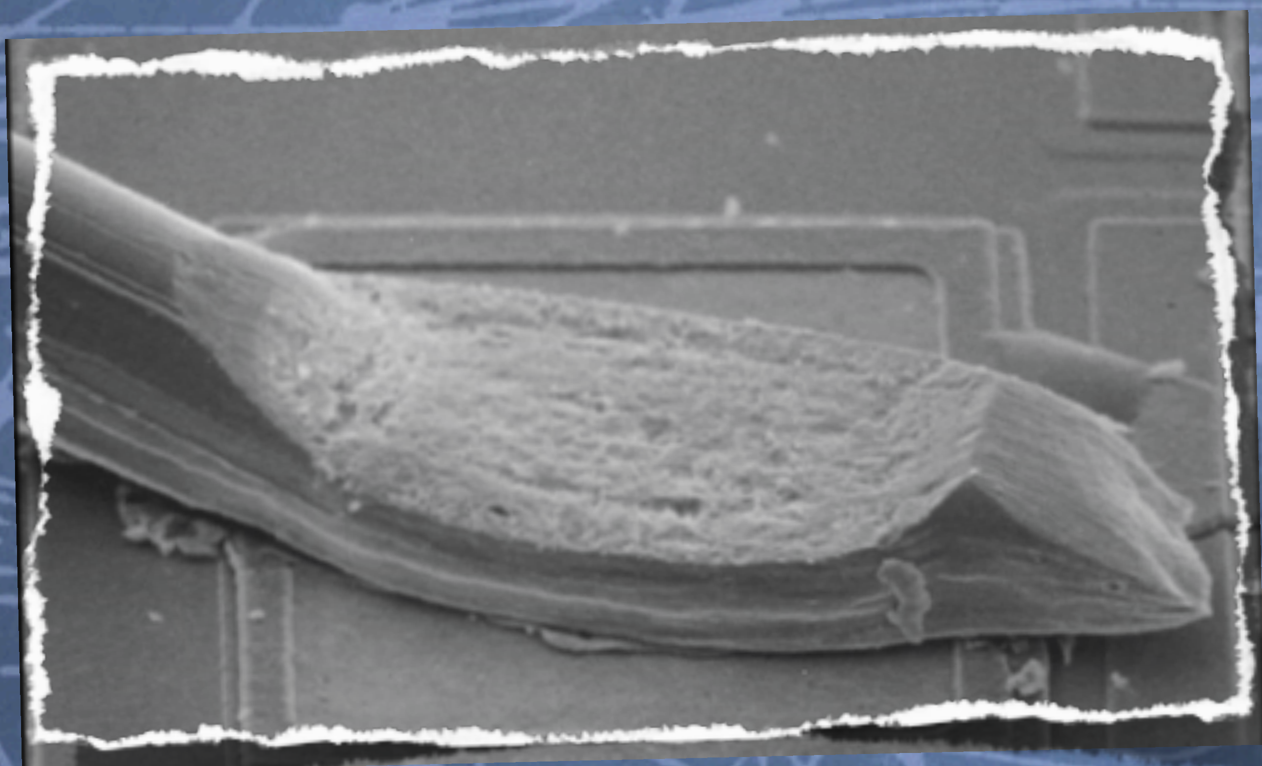
Production yield and timelines of 2576 modules:

Indium bumps:
- OK: 89%
- Virgin OK: 74%
- Reworked: 13%
- Failed: 11%

Solder bumps:
- OK: 97%
- Virgin OK: 87%
- Reworked: 7% + 3% internal
- Failed: 3%







Wire Bonding

Wirebonds on a Module

720 WIREBONDS

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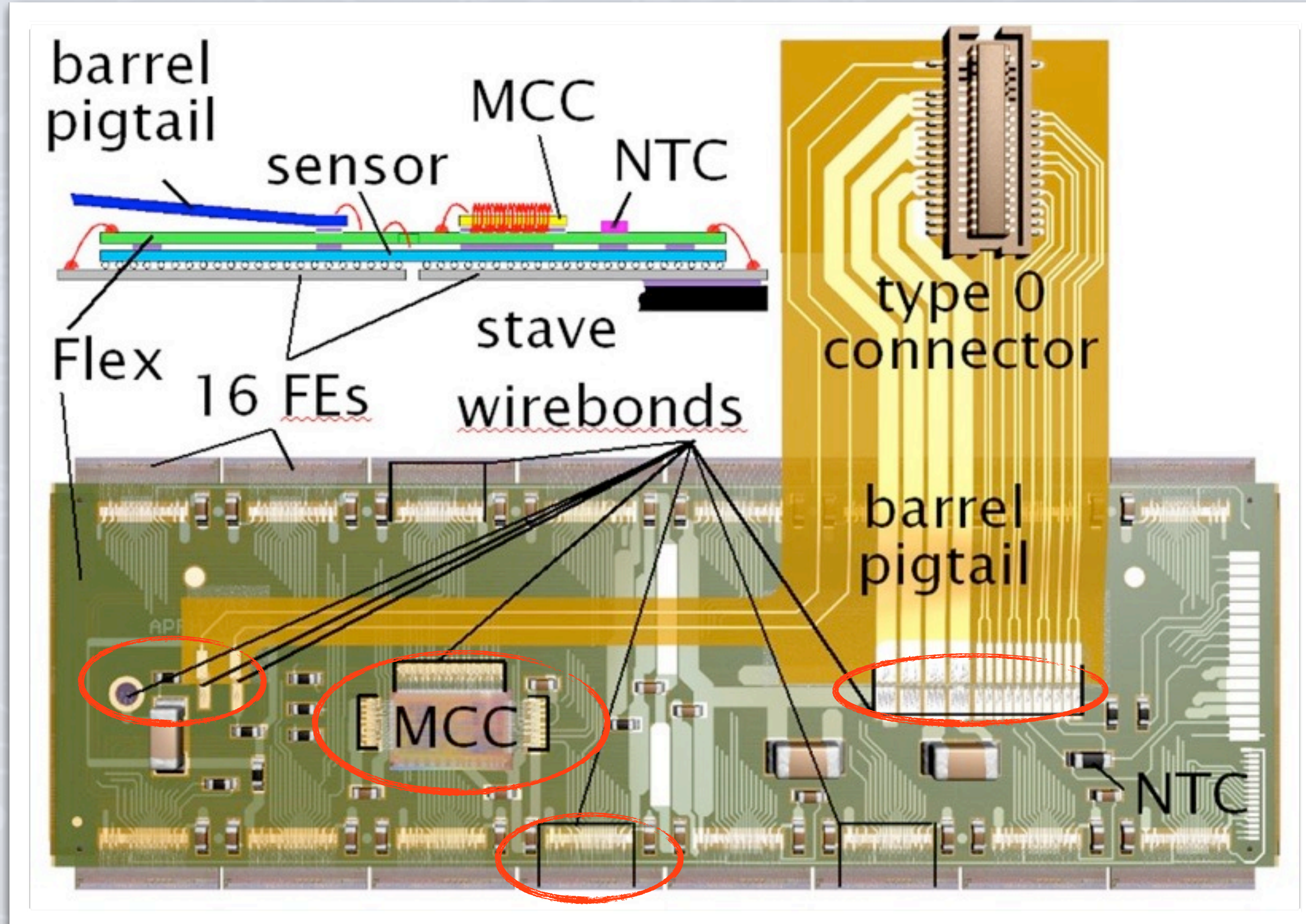

Wirebond Positions

SPLITUP & STRATEGY

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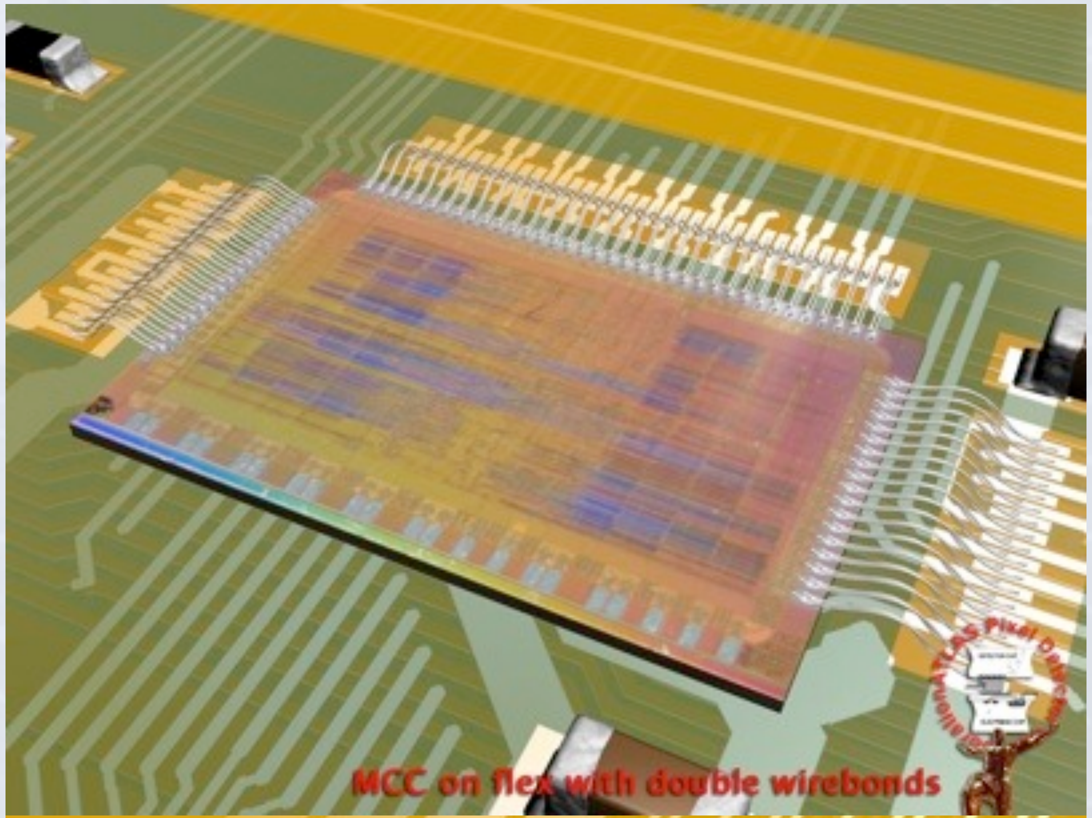
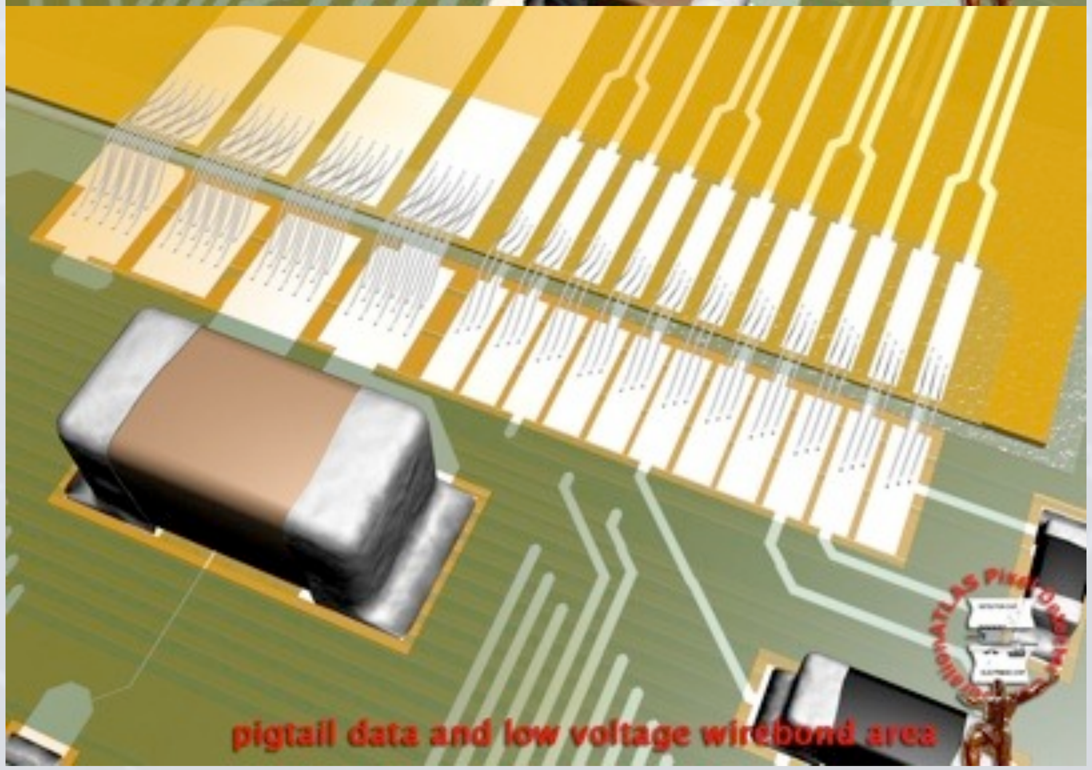
720 Wirebonds 25µm round Al:

- FE: 1 bond * 30 * 16 FEs = 480
- MCC: 2 bonds * 71 = 142
- Power: 14 bonds * 4 = 56
- Data: 3 bonds * 11 = 33
- HV: 3 bonds * 3 = 9

- three/two different lengths to avoid breaking by resonances, caused by Lorentz force in the solenoid field during power cycling or fixed frequency data
- FE wire bonds are potted at their bond feet
- MCC feet were potted at beginning of production





Wirebond Pull & Poke Quality Assurance

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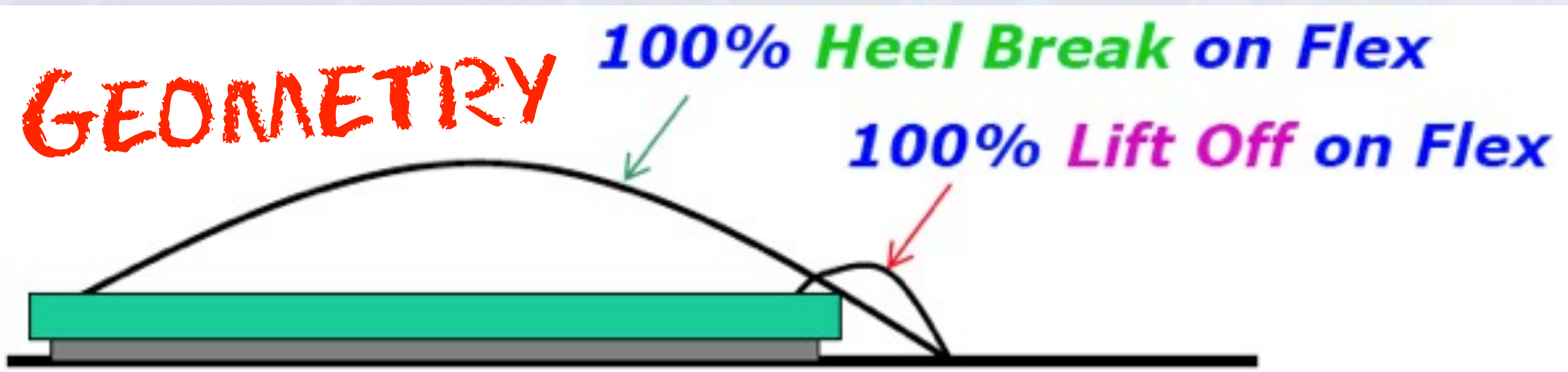
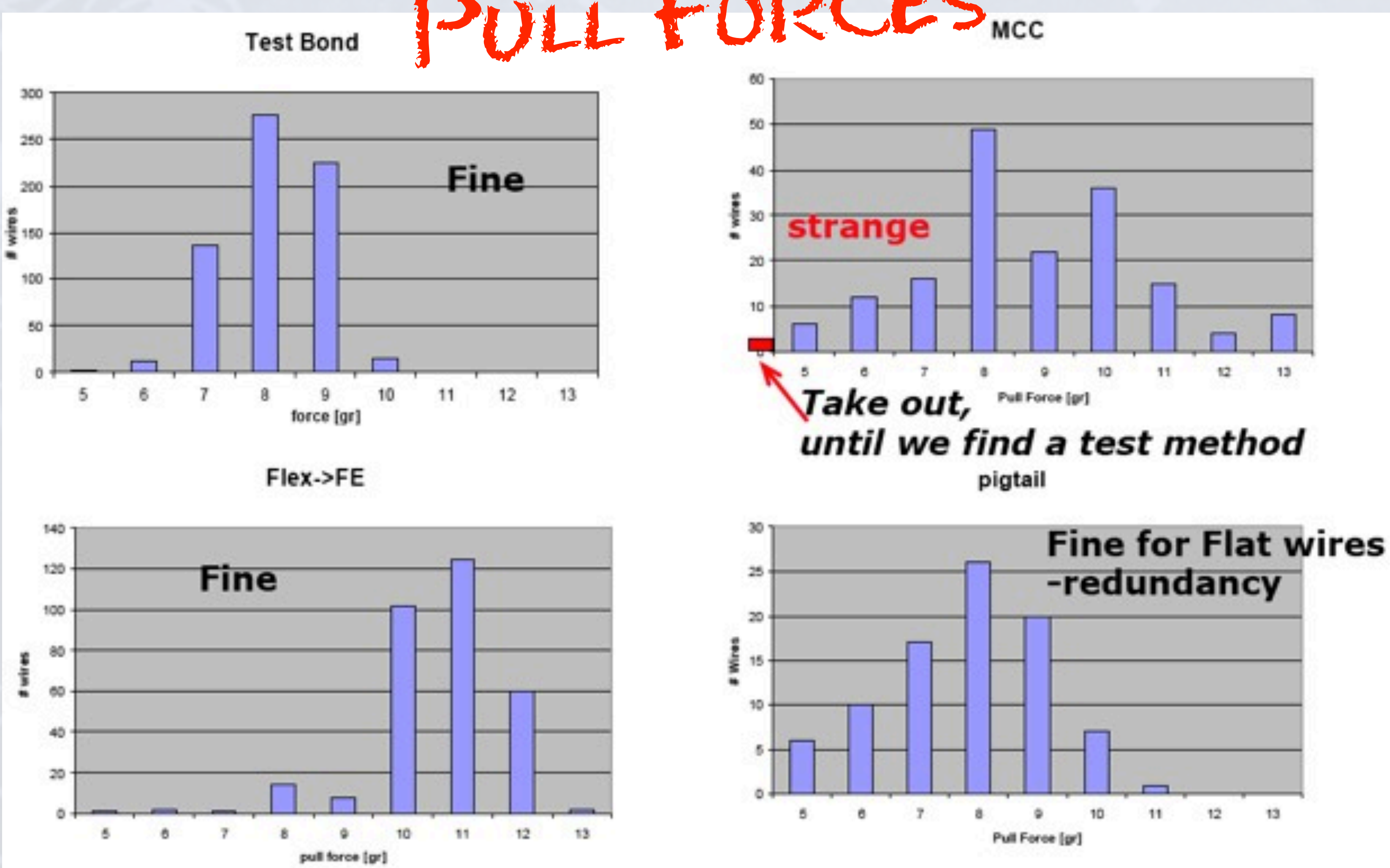
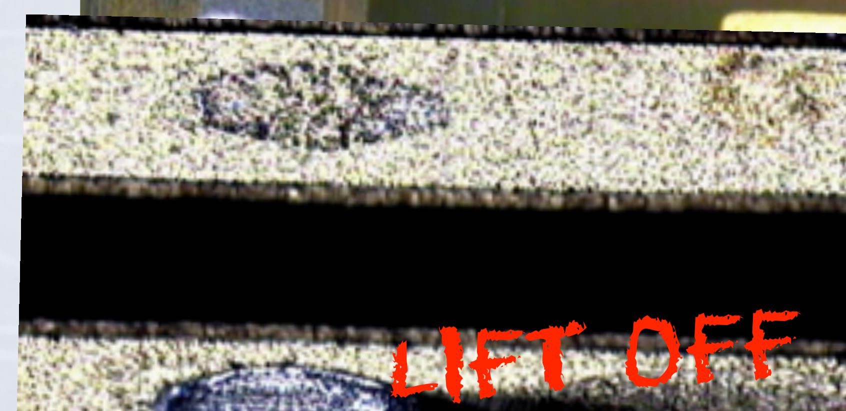


Pull Forces





Wirebond B-FIELD Resonances

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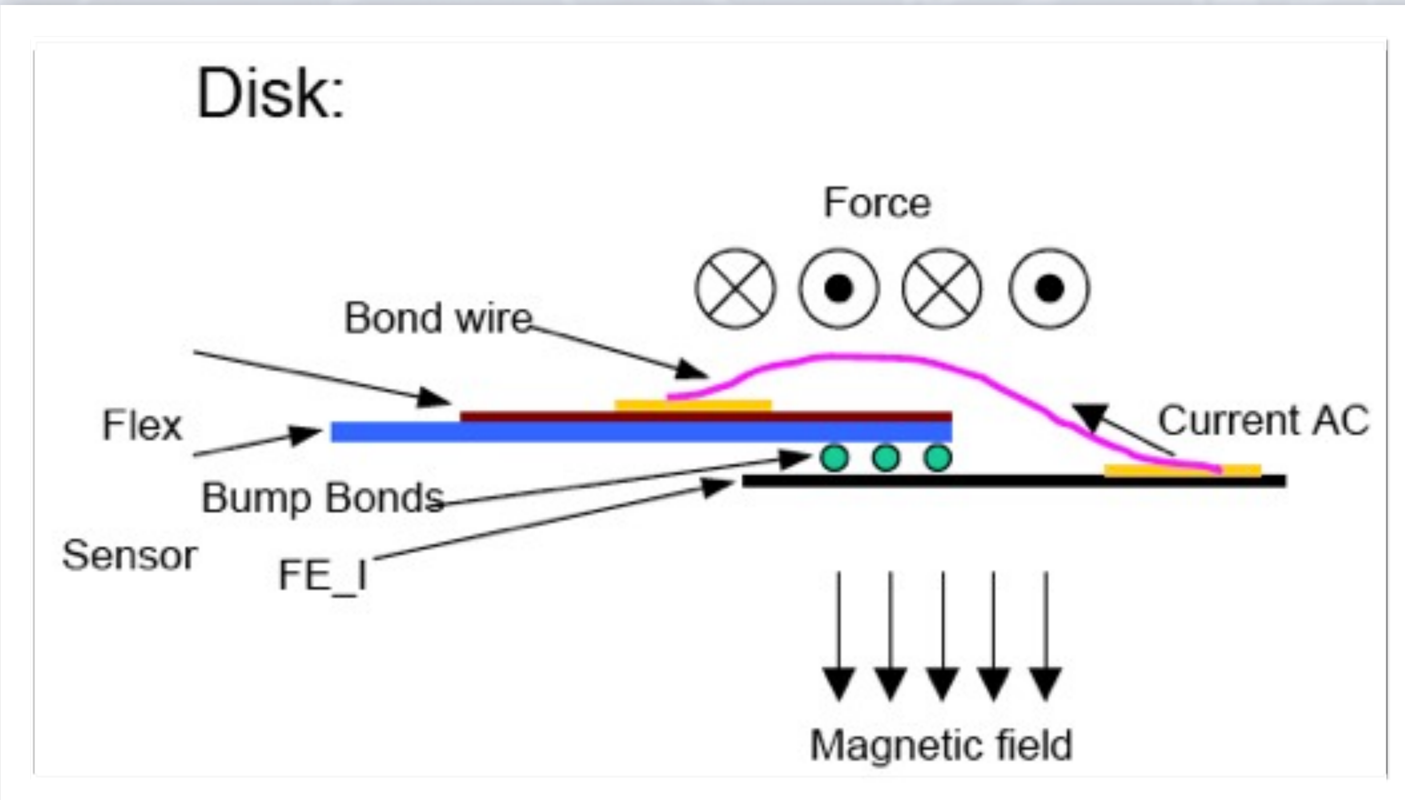
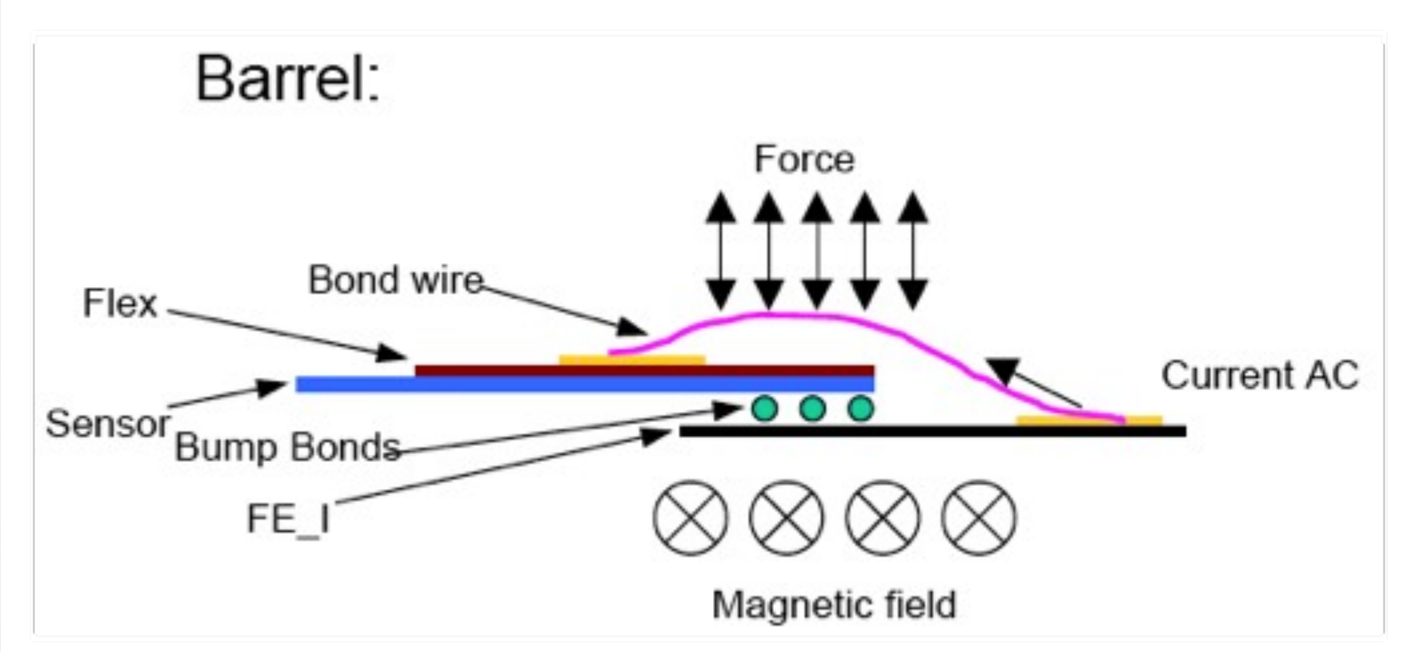
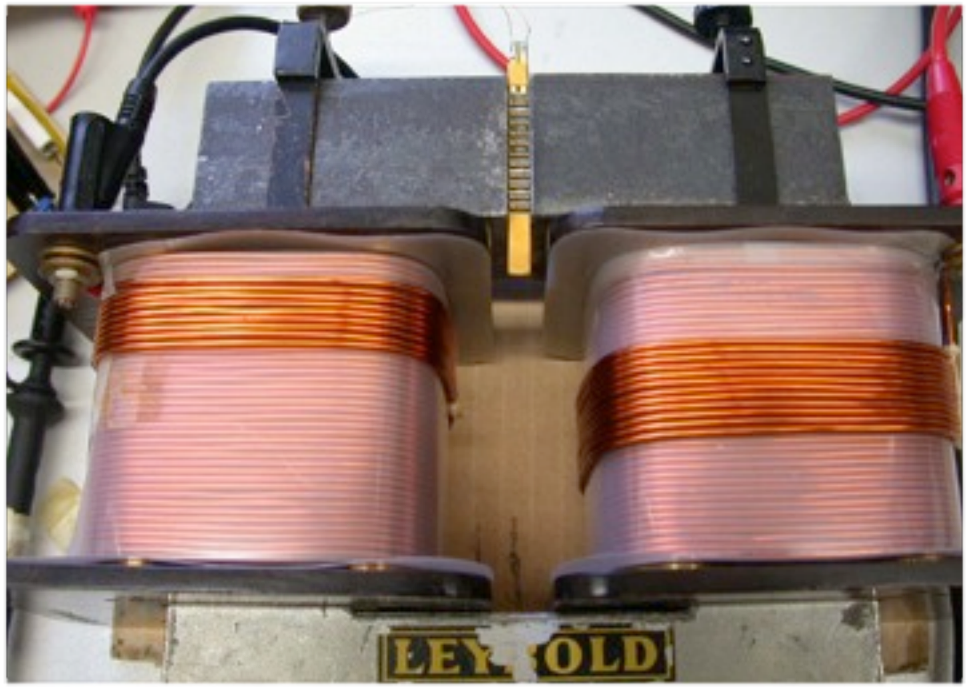


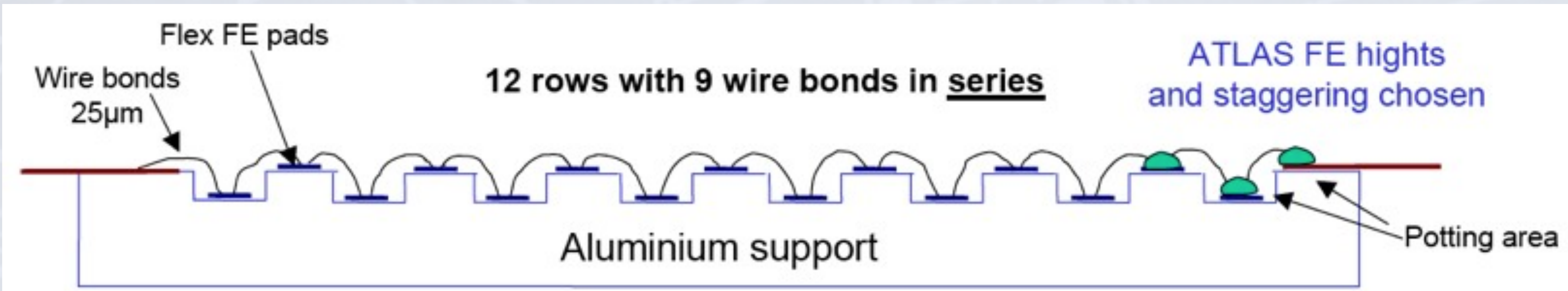


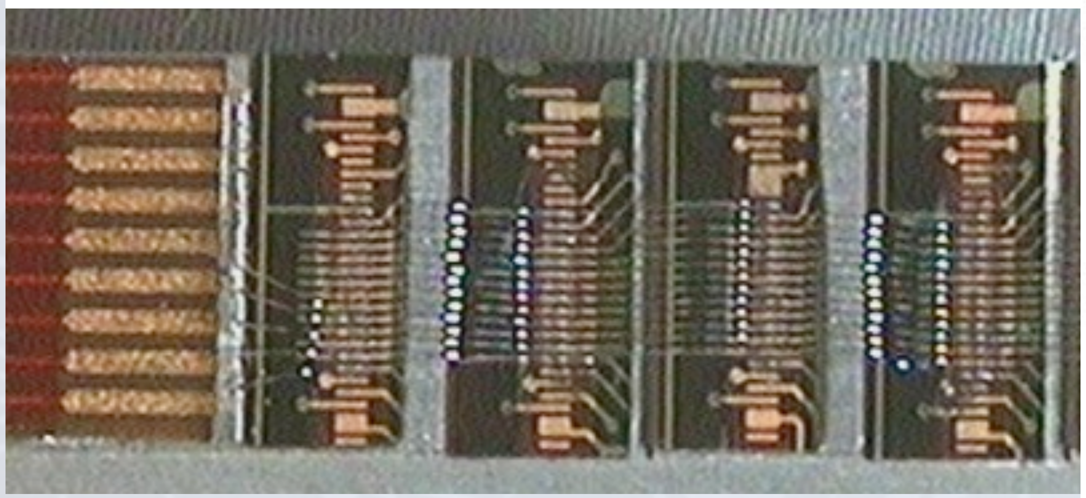
Atlas: worst case
B = 2 Tesla
Δ Iddd = 38 mA
Δ Idda = 55 mA

Test setup:
B = 0.4 Tesla
=> chose **I_{ac}= 200 mA**

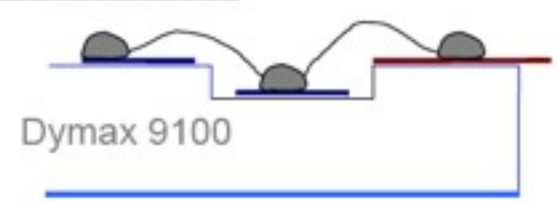


Wirebond B-FIELD Resonances

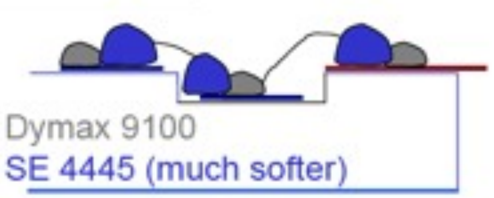




9 wire in series



27 wire in series



20kHz – 35 kHz sweeps @ 200 mA:

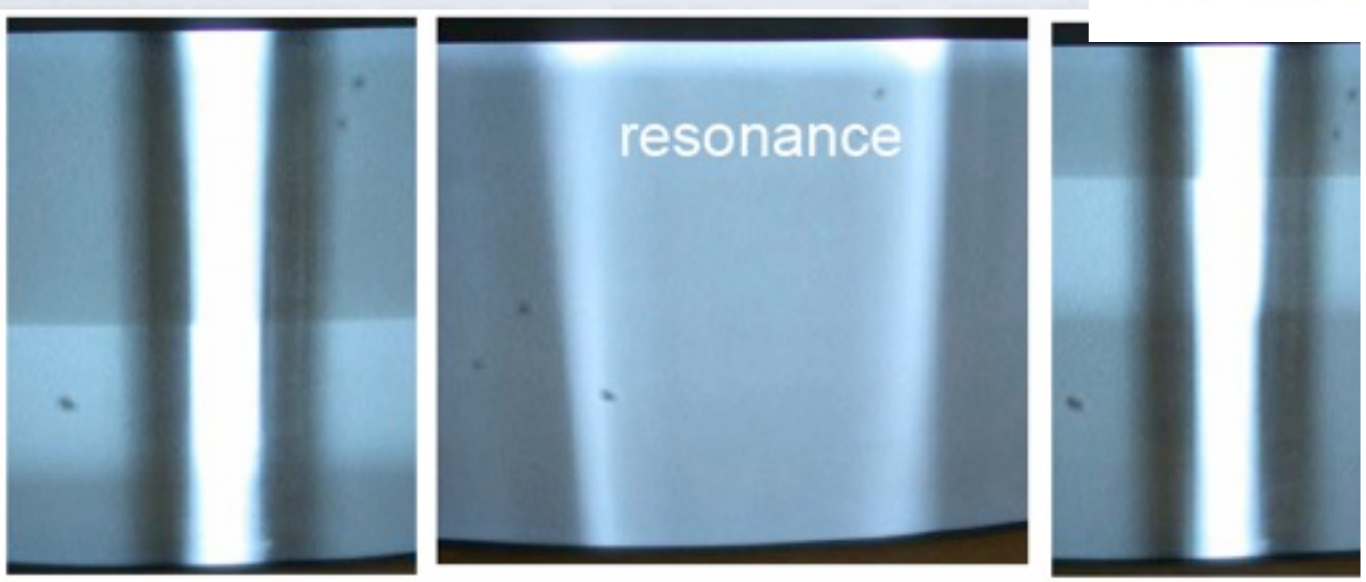
After 80 sweep cycles

@ 200 mA / 0,4 T → bond breaks

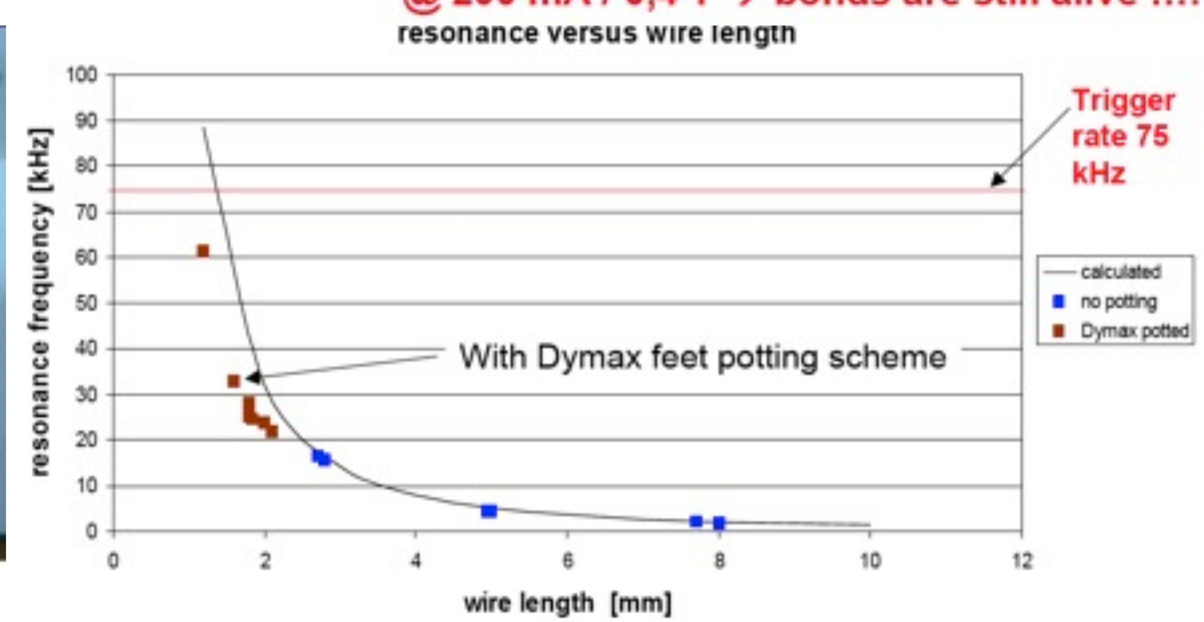
20kHz – 100 kHz sweeps @ 200 mA:

After 15480 sweep cycles

@ 200 mA / 0,4 T → bonds are still alive !!!!



18 kHz | 17,5 kHz | 17 kHz

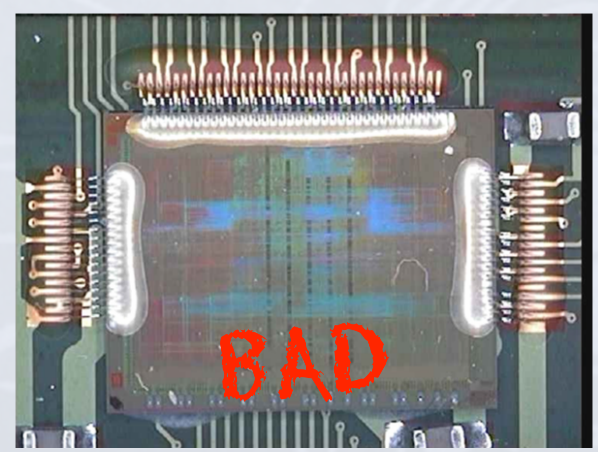


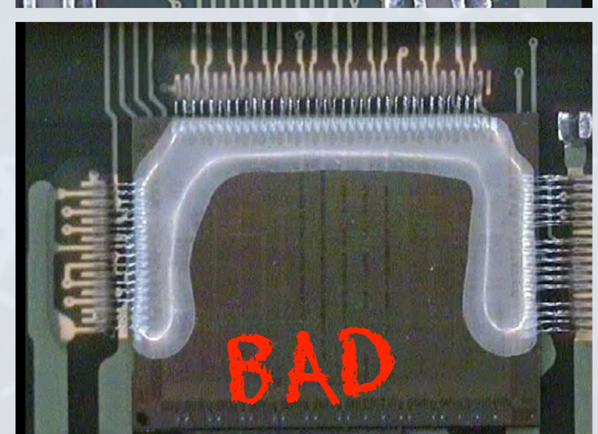
Wirebond MCC Encapsulation

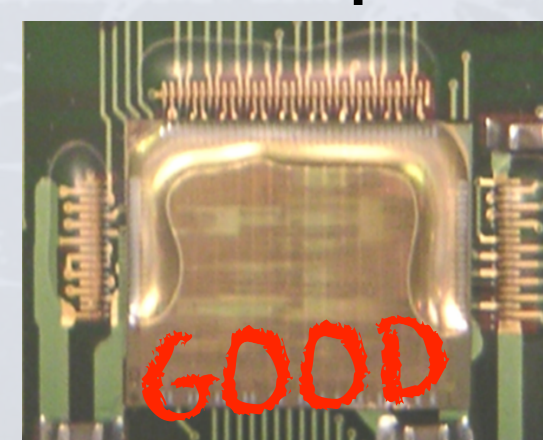
- For FE chips NECESSARY to avoid power bond failure due to mechanical resonance in B- field
- MCC bonds safe from this effect (much shorter and no AC currents), thought conservative to treat all bonds the same way
- Encapsulating detaches from the MCC surface expands and contracts 50µm with thermal cycling: CTE encapsulant = 100 x CTE silicon - sheers on the END bonds and can breaks them
- Removal of encapsulant and re-bonding

Influenced by:

- Geometry of bead
- MCC surface properties - SE4445 glue to attach the MCC to the flex - fine for Eccobond 45 glueing
- Curing procedure. Hot UV lamp vs. cold UV lamp







Summary & Conclusions

- 80.3M bumpbonds with 50 µm pitch
- Solder & Indium bumps - different electrical resistance (noise)
- X-ray & electrical quality control
- Disconnected Bumps main reason (0.1%) for dead pixels
- Large disconnected areas grow with thermal cycling, especially for Indium bonds and FE edges
- Particle contamination (dicing) create shorts and hot-spots
- Many possibilities for mechanical stress on FEs and sensors
- Anyhow good yields, especially with rework possibility

- 1.3M wirebonds, 25 µm Al round wire
- Quality Assurance: Geometry, breaking mechanisms
- Redundancy with different wire bond lengths, feet potting
- Resonances in B-field studies show need for encapsulation
- Feet potting can cause wire bond breaking as well

Backup Slides

Deposition of UBM STEP 1

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IZM STEP 1

To ensure good adhesion, at IZM, the wafers are sputter etched before sputtering of an adhesion layer (200 nm TiW) and the plating base (300 nm Cu) by electroplating. Photoresist is spin coated on the wafer and patterned by exposure to UV light through a high precision contact mask followed by an etching process. A wettable UBM (5 µm Cu) is plated followed by an 100-200 nm gold oxidation protection layer.

AMS STEP 1

At AMS photosensitive photoresist is spin coated on the wafers and patterned with the conventional photolithography process described above. A proprietary UBM is deposited.

Deposition of Bumps Step 2

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IZM Step 2

At IZM solder (37% Pb 63% Sn) is electroplated. It remains as 30 µm high cylindrical bumps after photoresist removal. The cylindrical bumps turn, caused by surface tension, into spherical bumps during a first reflow process.

AMS Step 2

At AMS the UMB is cleaned with a plasma etching process immediately before the deposition of indium, obtained by electron beam evaporation of indium under vacuum (~ 10^{-6} Torr). The photoresist is removed by a wet lift-off process and indium cylinders of about 20 µm in diameter and ~8 µm in height remain.

Thinning and Dicing of FE Wafers Step 3 & 4

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IZM & AMS Step 3

Since many processing steps of the bump deposition are hard to carry out with thinned and fragile wafers, thinning takes place after bump deposition. The FE wafers are completely coated with a thick photoresist layer to protect the bumps. They are thinned to ~ 180 µm by backside mechanical grinding at GDSI (Grinding and Dicing Services Inc., Sunnyvale, CA, USA)

IZM & AMS Step 4

The fragile wafers are diced immediately after thinning to minimize the risk of braking by handling. To ensure that FE chips have not been damaged the diced and bumped single chips are held by custom carriers and tested with probe stations.

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IZM STEP 5

Photoresistive protection cover layers are removed by the described lift-off process. At IZM all 16 FEs are tacked together to the sensor UBM by solder flux using a precision pick and place bonder. The entire bare module is placed in a reflow oven. It undergoes a 4 minutes heating cycle with a maximum temperature of 240°C for a few seconds in an activated atmosphere. The bumps and the UBM are solder merged. Caused by surface tension of the bump balls the FEs align themselves.

AMS STEP 5

At AMS a single automated machine is used to precisely align, flip and bond the FEs one-by-one onto the sensor. The bonding process itself is a thermo compression at 90°C for a couple of minutes with an applied force of 25 N per FE. Since no self alignment happens for indium bumps, the alignment and planarity of the applied pressure have to be more accurate than for solder bumps.