Final annual meeting

Praha 8 may 2025

WP 11

Microelectronics

A. Rivetti (INFN) Ch de La Taille (CNRS)

14:00

| introduction | Angelo Rivetti et al. |
| Solid21 Kochanovska hall A, FZU | 14:15 - 14:30 |

| **WP11.2 28 nm update from CPPM** | Mohsine Menouni |
| Solid21 Kochanovska hall A, FZU | 14:30 - 14:45 |

| **WP11.2 28 nm update from INFN PV** | Luigi Gaioni et al. |
| Solid21 Kochanovska hall A, FZU | 14:45 - 15:00 |

15:00

| **WP11.2 28 nm update from AGH** | Marek Idzik et al. |
| Solid21 Kochanovska hall A, FZU | 15:00 - 15:15 |

| **WP11.2 28 nm update from U Bonn** | Mr Kennedy Caisley |
| Solid21 Kochanovska hall A, FZU | 15:15 - 15:30 |

16:00

| **Coffee break** | |
| Kochanovska hall B, FZU | 16:00 - 16:20 |

| **WP11.3 130nm update from AGH** | Marek Idzik et al. |
| Solid21 Kochanovska hall A, FZU | 16:20 - 16:35 |

| **WP11.3 130nm update from CNRS/OMEGA** | Damien Thienpont et al. |
| Solid21 Kochanovska hall A, FZU | 16:35 - 16:50 |

| **WP11.3 130nm update from INFN/TO** | Andrea Di Salvo et al. |
| Solid21 Kochanovska hall A, FZU | 16:50 - 17:05 |

17:00

| **WP11.3 130nm update from WEEROC** | JULIEN FLEURY |
| Solid21 Kochanovska hall A, FZU | 17:05 - 17:20 |

28 nm chip design

Pixel array | SET | RO - TID | Single devices

R&D on hybrid pixels

- Process qualification in terms of performance for analog, low-power and low-noise circuits
- Architecture studies
- Fast charge amplifier array

Study of Single Event Effects (SEE)

- Measure the **SET cross-section**
- Measure the **SET pulse width** with a good resolution < 20 ps
- Measure the effect of the std cell size

Mini@sics of 2×1 mm2 received June 2023, consisting of 4 main blocks

- Analog pixel array (25×12 µm2) with Fast charge amplifiers for high time resolution
- SET test structures
- Ring Oscillators for TID tests on digital standard cells
- Test structures for TID tolerance studies

TID tests and qualification

- Compatibility with typical dose levels for future projects
- 28 nm process device qualification
- **Gate delay** evolution with TID and the effect of the std cell size
- TID Effects modeling → Analog and digital simulations with TID effects

May 5, 2025   WP11.2 - 28 nm update from CPPM   4

Noise and time resolution

HTRPix- Noise scan

Cdet = 0 - 4 col
Cdet = 25fF - 1 col
Cdet = 50fF - 2 col
Cdet = 75fF - 1 col
Cdet = 100fF - 4 col

Qin = 2000 e-
TDAC=10000
Ibp_DAC = 1µA
VMfb = 590 mV

Timing resolution

- cdet = 0
- Cdet = 100 fF
- Cdet = 50 fF
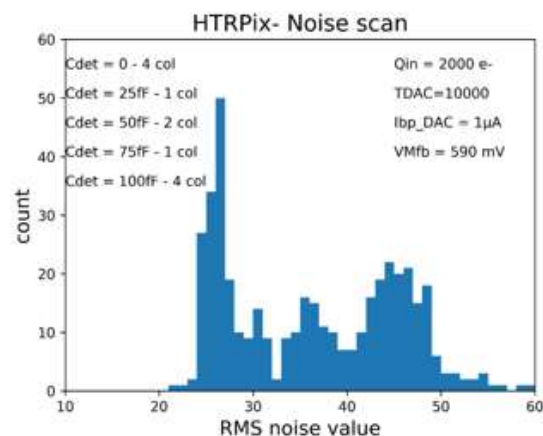
The pixels are connected to MOM capacitances to add the effect of the detector capacitance

- 4 columns without capacitance, 4 columns connected to 100 fF, 2 columns to 50 fF, 1 column 25 fF and 1 column 75 fF
- For Cdet = 0 -> RMS noise = 25 e-
- For Cdet = 100 fF -< RMS noise = 45 e-

The time resolution measured with high bandwidth oscilloscope

- Only one pixel is selected at a time
- Histogram of the Time delay between the injection signal and the hit-Or output
- Measurements show higher jitter than predicted by simulations
  - For Qin=4ke- and Cin=100 fF, the output hit shows a phase jitter of 150 ps, about 50% higher than the value obtained by simulation (100ps).
- Further work is underway to understand whether the extra jitter is intrinsic to the design or related to the test setup.

May 5, 2025

WP11.2 - 28 nm update from CPPM

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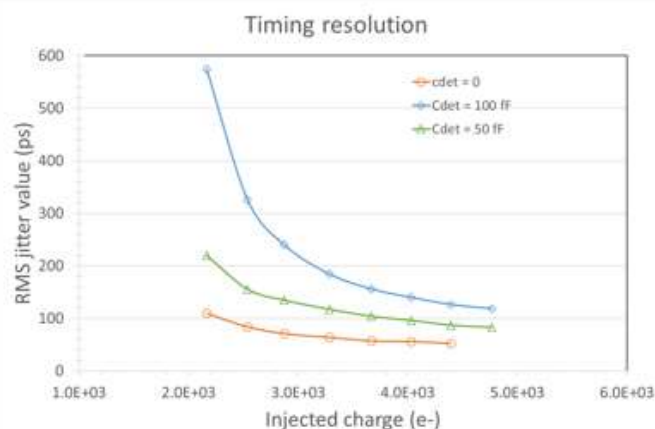
Ionizing radiation effects (up to 3 Grad)
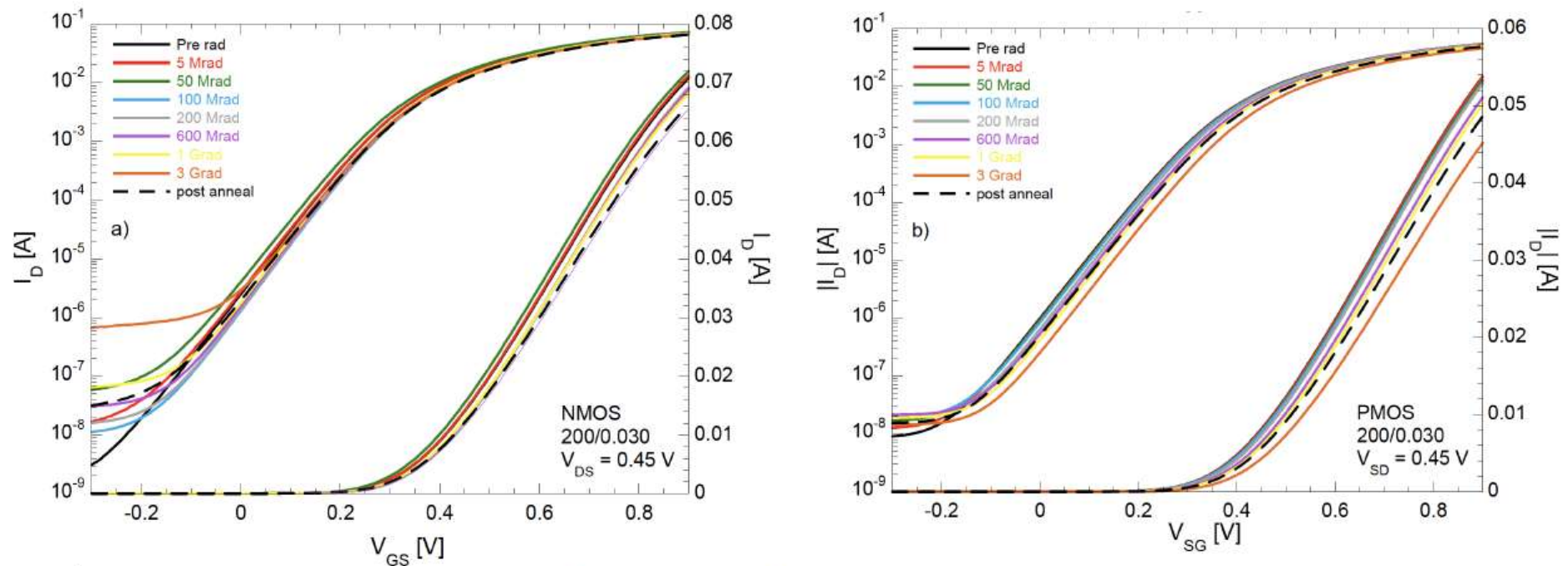
- Investigated devices **irradiated up to 3 Grad(SiO_2)** total dose with X-rays (5.5 Mrad/h dose rate)
- MOSFETs biased during irradiation in the **worst-case condition**
- Moderate increase in drain leakage current after irradiation (much more pronounced for NMOS devices)
- **Limited threshold voltage changes** (depending on MOS polarity and geometry)

G. Traversi et al., **Ionizing Radiation Effects of 3 Grad TID on Analog and Noise Performance of 28nm CMOS Technology**, IEEE Transactions on Nuclear Science, 10.1109/TNS.2025.3542230

Flash ADC based front-end

10
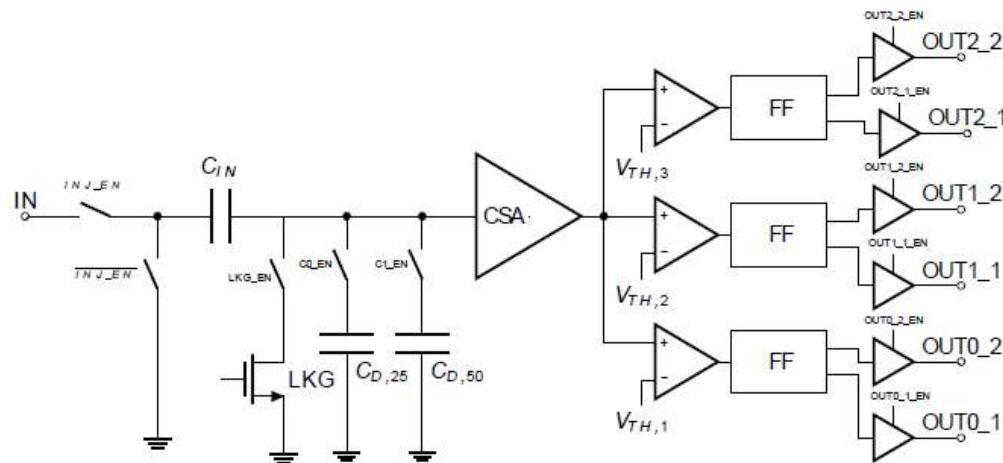
- Preamp (**regulated cascode**) two independent feedbacks
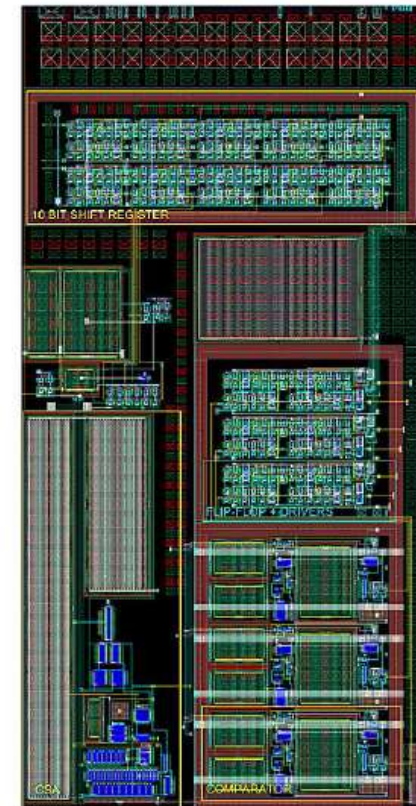
- Ancillary blocks for **detector emulation**

- **AC coupled, auto-zeroed comparators**, operated with 40 MHz clock, implementing a **2-bit flash ADC.** The design is ideally insensitive to device threshold voltage mismatch → threshold tuning DAC not required

- Overall **current consumption**: 5.4 uA → 4.9 µW **power consumption** @ V_{DD}=0.9 V

- Elementary cell size: 25 x 50 µm² (analog+digital)

- Submitted in a **8x4 matrix**

Fast ultra-low power 10-bit SAR ADC in 28nm MiniAsic
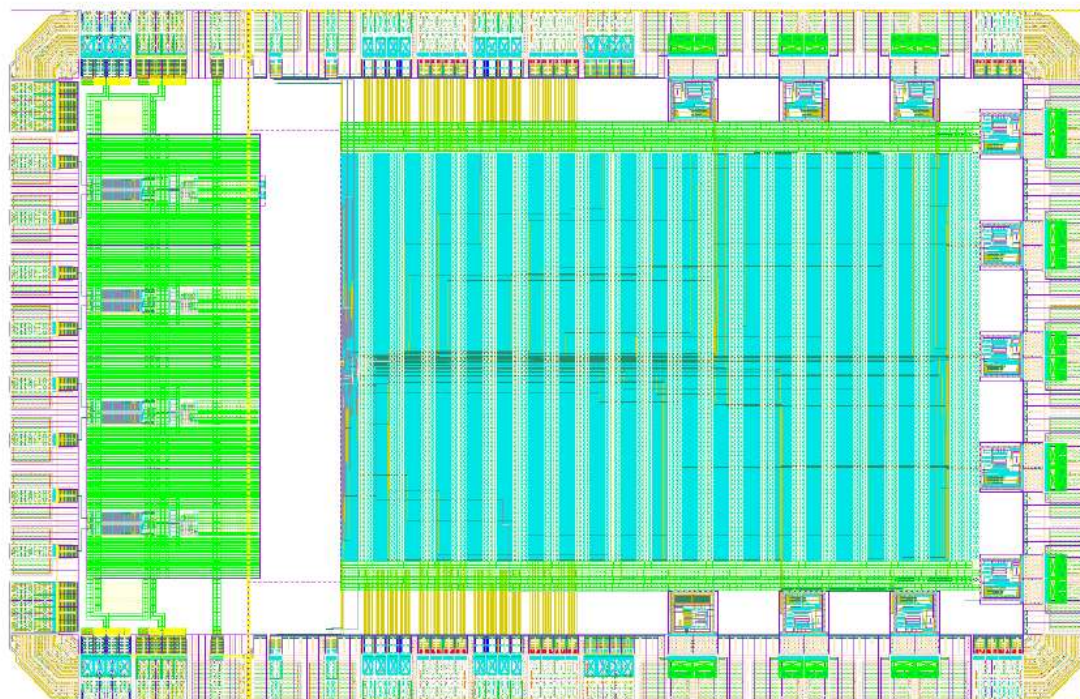
1750um x 1120um

- 4-channel ADC ASIC designed and submitted to production
- Prototypes produced at the end of 2024

5

- Optimization of SAR ADC architecture

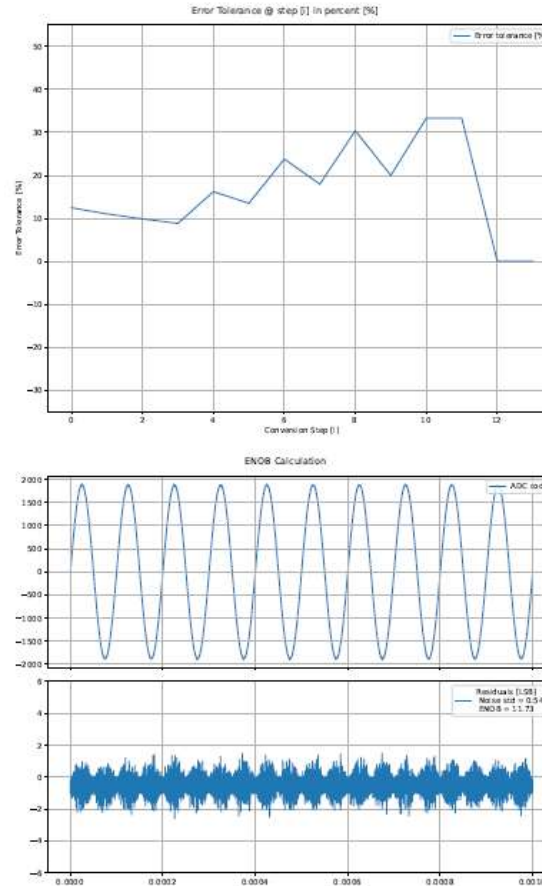| Design	CORDIA	FRIDA
ADC resolution	10-bit	10/12-bit
Conversion rate	2.5MHz	10 MHz
Area of one ADC	80x330 μm^2	50x200 μm^2
Power of one ADC	30 μW	100 μW
FOM_csa (conv/sec/area)	95 Hz/μm^2	5000 Hz/μm^2
FOM_epc (energy/conv)	12 pJ	10 pJ
FOM_ppa (power/area)	0.11 W/cm^2	5.0 W/cm^2
ADC qty Mpix @ 100 KHz	40000	10000
ADCs total pixel rate	100 Gpx/s	100 Gpx/s
ADCs total data rate	1 Tb/s	1 Tb/s
ADCs total area	10.5 cm^2	0.2 cm^2
ADCs total power	1.2 W	1.0 W

65nm → 28nm

12-bit w/ device noise, mismatch, etc

AIDA innova

Design in CMOS 130nm
Fast ultra-low power 10-bit SAR ADC...

This ADC is already used in:

- HGCROC for HGCAL in CMS Upgrade and HKROC ASICs
  (few publications prepared by OMEGA group)
- TOFHIR for MTD in CMS Upgrade

  TOFHIR2: the readout ASIC of the CMS barrel MIP Timing Detector, E. Albuquerque et al (M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek), Journal of Instrumentation 2024 vol. 19 art. no. P05048, https://arxiv.org/abs/2404.01208
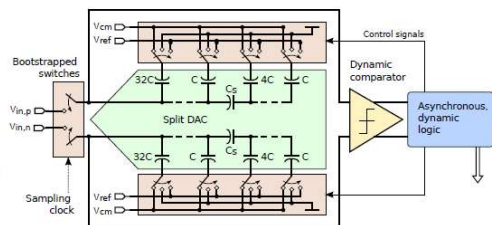- FLAME and FLAXE ASICs for electromagnetic calorimetry

R&D in CMOS 130nm
New 10-bit ADC with internal threshold

Basing on existing 10-bit ADC
- power 680uW@40MSps
- works up to 50MSps

- To decrease power consumption even further (~250uW@40MSps), full conversion is done only for signals above configurable threshold
- Design completed and ready for submission

Design and simulation results in:

Development of a 10-bit ultra-low power SAR ADC with programmable threshold in 130 nm CMOS technology, P. Prus, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, Journal of Instrumentation 2025 vol. 20 art. no. C01009,

Design in CMOS 65nm
Fast ultra-low power 10-bit SAR ADC

Few slightly different versions of 10-bit SAR ADC. Design in 65nm based on 130nm ADC

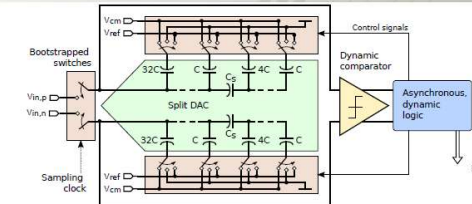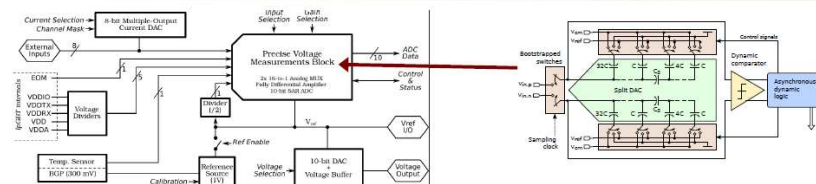- power ~500uW@40MSps
- works up to 90MSps
- ENOB ~9.2 bits

Results in:

Ultra-low power 10-bit 50-90 MSps SAR ADCs in 65 nm CMOS for multi-channel ASICs, M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, Journal of Instrumentation 2024 vol. 19 art. no. P01029

Design in CMOS 65nm
lpGBT monitoring system comprising fast ultra-low power 10-bit SAR ADC

- Monitoring system for lpGBT high speed transceiver

An lpGBT subsystem for environmental monitoring of experiments, M. Firlej, T. Fiutowski, J. Fonseca, M. Idzik, S. Kulis, P. Moreira, J. Moroń, K. Świentek, Journal of Instrumentation 2023 vol. 18 art. no. P06008

lpGBT: low-power radiation-hard multipurpose high-speed transceiver ASIC for high-energy physics experiments, P. Moreira et al (M. Firlej, T. Fiutowski, M. Idzik, J. Moroń, K. Świentek, IEEE Transactions on Nuclear Science 2025 vol. 72 no. 1,

- 10-bit ADC will be used in PACIFIC++ for SciFi and MS in LHCb Upgrade

AIDA INNOVA bEngineering run submitted in April 2023

Layout Draft of E-ITO-TMSS02-001
(As of 2023-08-08 21:50:08 GMT+8)

- TSMC 130 nm
- 10 chips have been submitted
  - From OMEGA, AGH, IJCLAB, WEEROC
  - C4 (16 wafers) and WB (4 wafers), 90 chips/wafer
  - In fab at TSMC in November 2023 only!
    - Reticle completion , payment, …
  -
- For OMEGA : EICROC0 and CPROC (deliverables

chip	x	y		lab
HKROC1B	5,96	6,16	C4	OMEGA
LADOC2B	3,243	2,142	WB	IJCLAB
LIROC2	11,244	4,919	C4	OMEGA
POPROC	11,244	4,919	C4	WEEROC
PSIROC	11,244	4,919	C4	WEEROC
RADIOROC2	11,244	4,919	C4	WEEROC
TEMPOROC2	11,244	4,919	C4	WEEROC
FLAXE	4,02	3,7	WB	AGH
EICROC0	2,89	3	WB	OMEGA
CPROC	3,243	2,142	WB	OMEGA
Total				

WP11 OMEGA 5 may 2025

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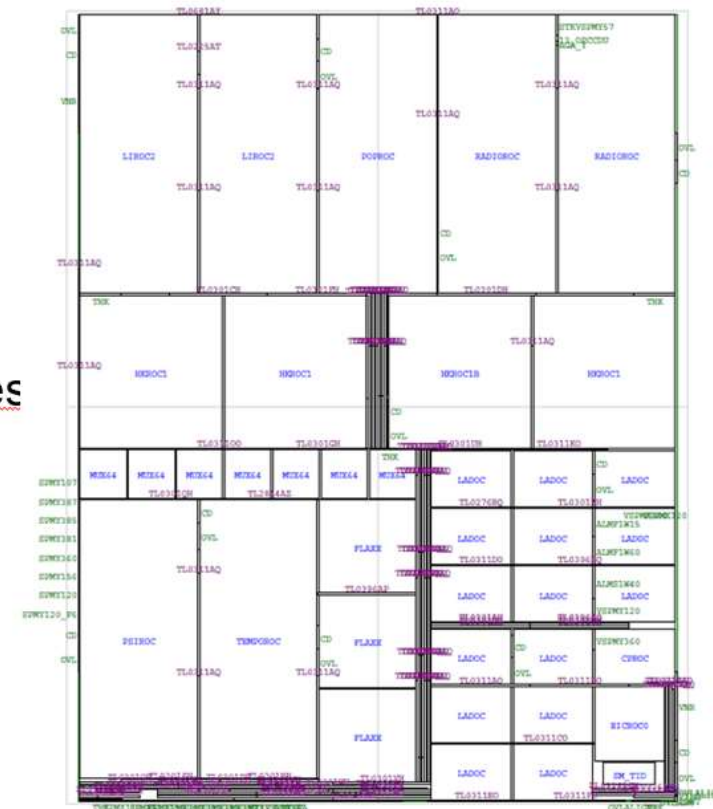
CPROC

- CPROC (Central Processing unit in ReadOut Chip)
  - TSMC 130 nm
  - Exploratory R&D: programmable, needs of more and more intelligence in chip
  - Based on the RISC-V

- Presented at TWEPP 2024

WP11 OMEGA 5 may 2025

10
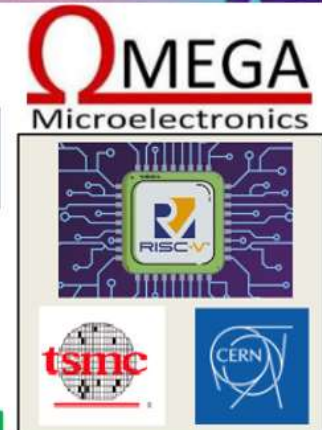
First protoype developed **in DS20k R&D**

Evolutions designed for the readout of the **EIC ePIC dRICH** SiPM sensors

- **32-pixel** matrix (8x4) mixed-signal ASIC

- **SiPM readout**: single-photon time tagging + Time-over-Threshold measurement or SR mode tagging.

- 32-bit (64-bit in ToT mode) event word generated on-pixel and propagated down the column

- **Fully digital output**: 4 LVDS 320 MHz DDR Tx links
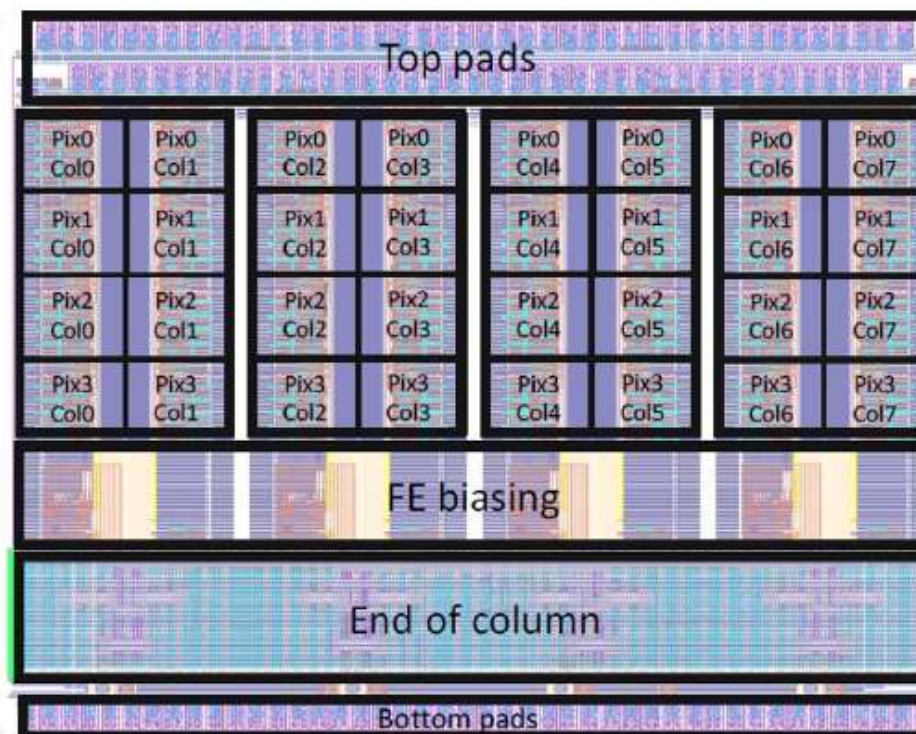
- Oct 2023 CERN PS beam test: dRICH detector for ePIC experiment at EIC
- SiPM: Hamamatsu S13360-3050, 3x3 mm², AC coupling readout
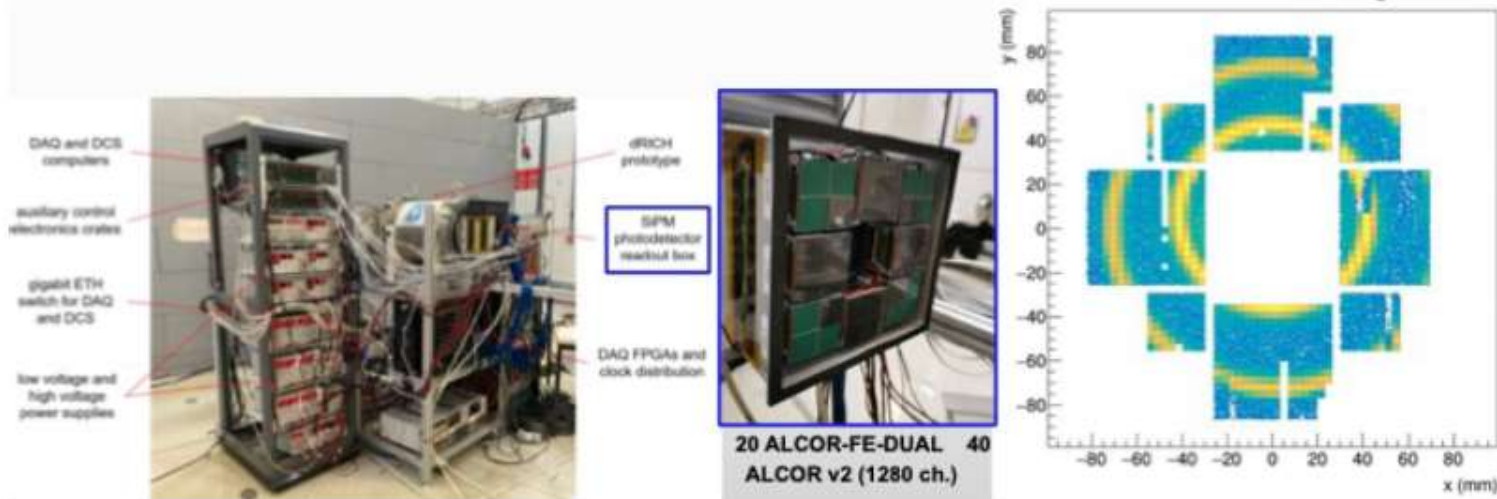
- **Chosen to readout dRICH at ePIC**
- **Final version: 64 channel in BGA packaging**

5 design taped-out

- Time of flight measurement for all kind of photodetector, 64 channels
  - Radioroc2 : SiPM dual modality (photon counting + charge integration)
  - Psiroc : low gain detector dual modality dual polarity
  - Poproc : PMT, MCP read-out, photon counting
  - Liroc2 : SiPM photon counting (collaboration Omega)
  - Temporoc2 : SiPM read-out, internal ADC and TDCs
- Last year, presentation of measurements, this year presentation of systems and applications

Application 1 : SPC LIDAR with Liroc

- Single Photon Counting LIDAR for spaceborne atmospheric measurement
- Single Photon Counting LIDAR for topographic airborne measurement

Application 2 : PET with Temporoc

- Temporoc 2 ASIC, Retimager collaboration
- Coincidence & Energy measurement, scalable to large system

Application 3 : RICH detector (Alice)

- Collaboration with INFN Bari (Nicola Mazziotta & Al)

Radioroc 2
- Discriminator output width scaling with the numbe of photo-electrons
- Operation threshold at single p.e.

PicoTDC
- Operation in ToA and ToT mode
- ToA LSB ≈ 3.05 ps
- ToT LSB ≈ 195.20 ps
- Acquisition window of 200 ns

Limitation
- SiPMs connected to the electronics through longer than 1 meter cables

In collaboration with Weeroc

Nicola Nicasolo – University and INFN Bari, Italy

Application 4 : TRNG

- QUANTUM : True Random Number Generation : Random Power spa
- Timing resolution on SPTR (dark noise)

Summary

- 2 main pillars in AIDA INOVA
  - Explore 28 nm technology performance for HEP
  - Provide readout ASICs in 130nm for other WPs

- 2 fabrications done in 2023 to match these objectives
  - Milestones MS45/46 and deliverables 11.2/11.3
  - Final deliverable was report on test results

- Good results shown at the meeting
  - More designs also continuing…

- Many publications (AGH record holder !)

backup

- **Task 11.1. Coordination and Communication [CNRS+INFN]**

- **Task 11.2. Exploratory study of advanced CMOS (28 nm)**
  - <u>INFN PV</u>, AGH, CNRS CPPM, UBONN
  - Explore advanced 28 nm CMOS for future trackers AGH, CNRS CPPM
  - Design and test front-end prototypes INFN PV, UBONN

- **Task 11.3. Networking and ASICs for other WPs (65/130 nm)**
  - AGH, <u>CNRS OMEGA,</u> IP2I, DESY, INFN (BA, BO, PV, TO) Uni Heidelberg, WEEROC (industry)
  - Cold and timing ASICs in 65/130nm CMOS : CNRS OMEGA, IP2I
  - MPGD readout ASICs : INFN (BO, TO)
  - Silicon and SiPM readout ASICs for future colliders and timing applications : AGH, CNRS OMEGA, DESY, UniH, WEEROC

- D11.1 : MPW in 28 nm

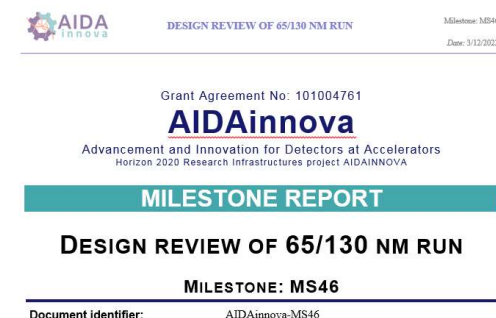# WP11.3 Deliverable
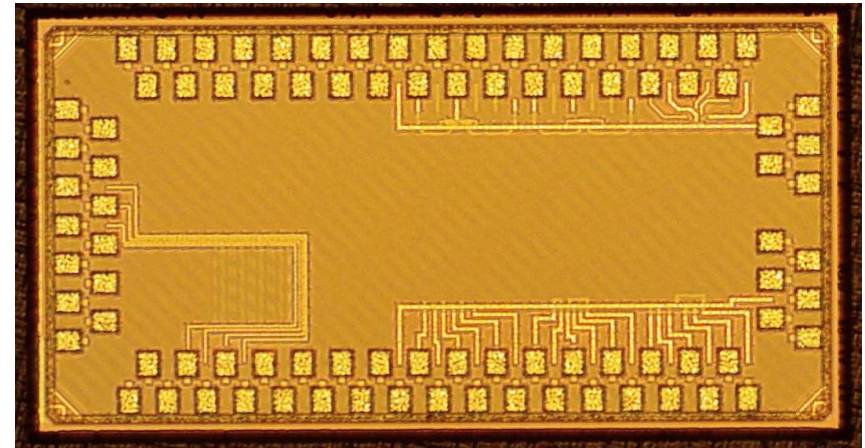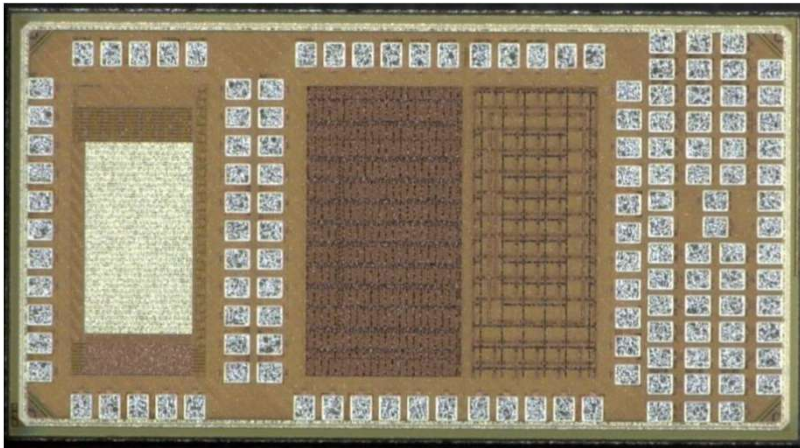
- D11.2 : MPW in 130 nm

- 5 chips from AIDA :
  - FLAXE (AGH) : Si/GaAs readout
  - EICROC (OMEGA/AGH/CEA) : LGAD readout
  - CPROC (OMEGA) : RISC5
  - LIROC (WEEROC) : SiPM timing
  - PSIROC (WEEROC) : Si readout

Layout Draft of E-ITO-TMSS02-001

(As of 2023-08-08 21:50:08 GMT+8)

AIDA engineering run
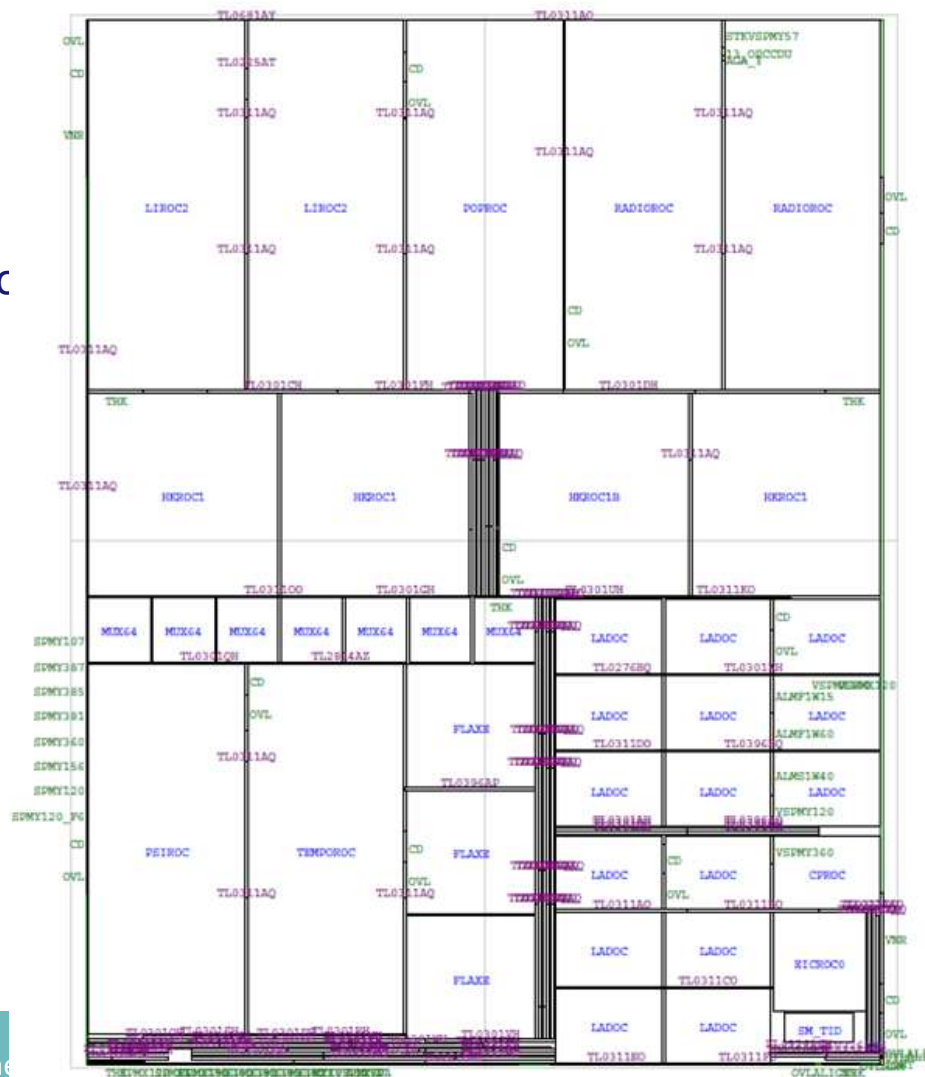
- AIDA participation in a 130nm engineering run constitutes D1.1
  - ~25% of the reticle area = 25% of the total cost (250k€)

- 4 chips from AIDA-INNOVA partners on this run
  - FLUXE (AGH)
  - EICROC (OMEGA/AGH/CEA)
  - LIROC (WEEROC/OMEGA)
  - PSIROC (WEEROC)
  - Submission scheduled jan 2023
  - Several hundreds of chips will be available

- Chips reviewed in november 2022
  - Constitutes Milestone MS46

Deliverables/Milestones
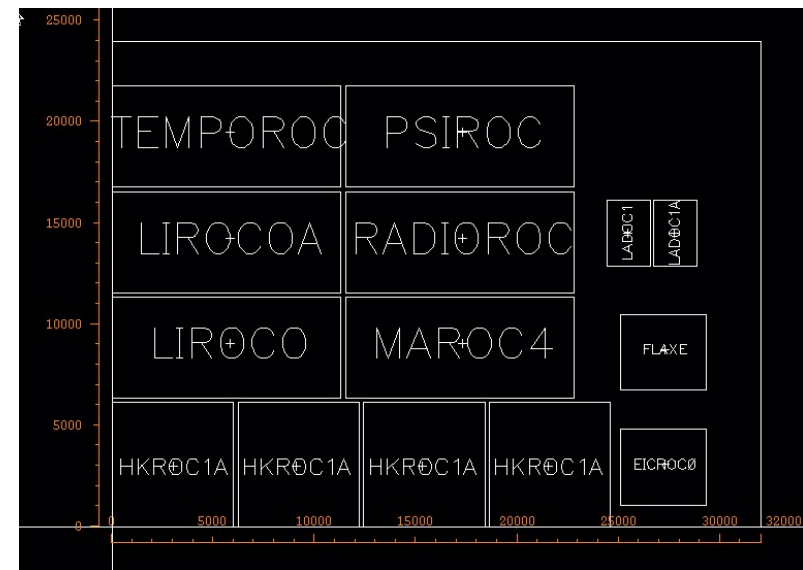
- **2 Milestones and 2 deliverables**
  - MS 11.1 and 11.2 (MS45 MS46) passed end 2022
  - D11.1 and 11.2 are the corresponding chips

MS11.1	**Design review of 28 nm MPW**	**11.2**	**18**	**report**
MS11.2	design review of 65/130 nm run	11.3	18	report

Deliverables related to WP11	
D11.1: MPW 28 nm *The deliverable is a multi-project wafer fabrication with the different test ASICs in CMOS 28 nm*	24
D11.2: MPW 65/130 nm *The deliverable is a multi-project wafer fabrication with ASICs in CMOS 65 and/or 130 nm that can be used to readout detectors from the other WPs and in particular WP8*	24
D11.3: Measurement reports *Each of the ASIC fabricated in the 2 previous deliverables will have its design and performance documented in a report*	42