WP10 – CSIC report

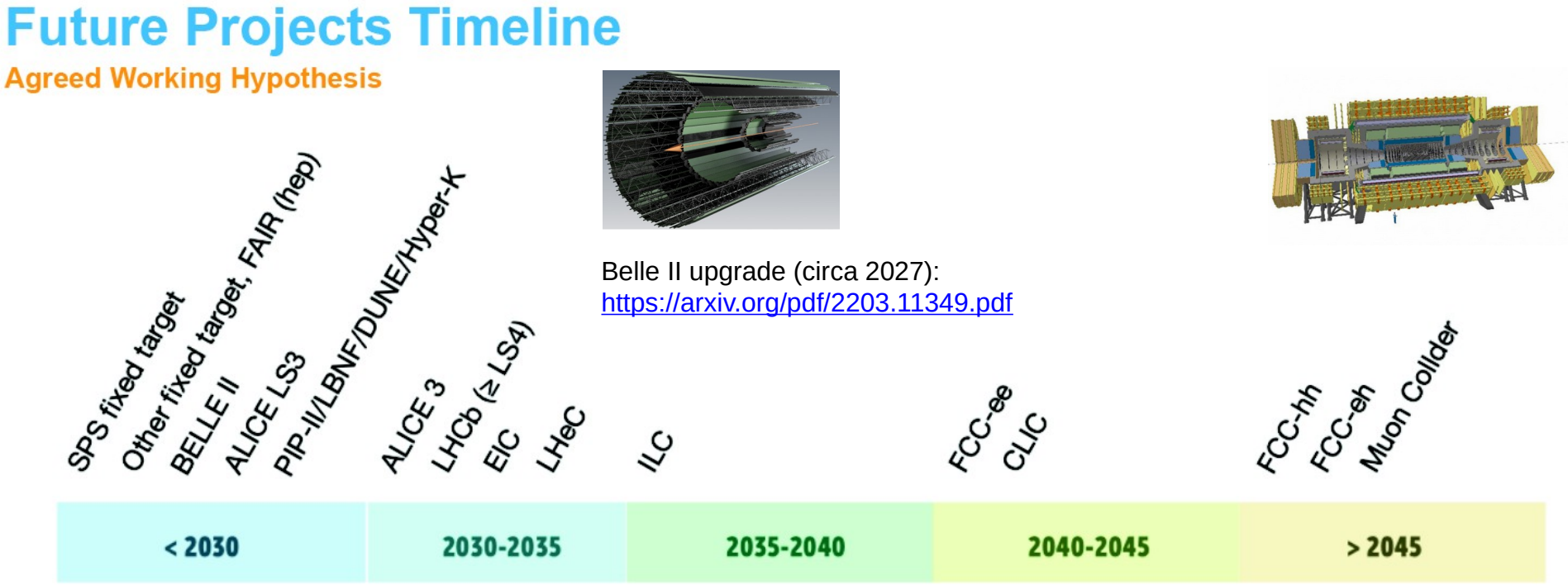

Carlos Marinas, Carlos Orero, Marcel Vos (IFIC – UVEG/CSIC – Valencia),

AIDAinnova annual meeting, Prague, May 2025

This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 101004761.

Global R&D landscape

- detector R&D time-line



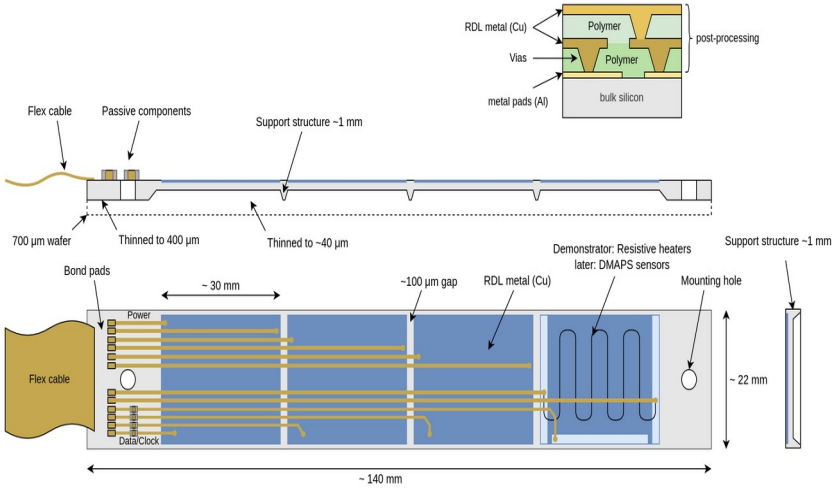
Belle II upgrade (circa 2027):
https://arxiv.org/pdf/2203.11349.pdf

- aim at the vertex detectors of Belle 2 and the Higgs factory
- intermediate-timescale projects are stepping stones

iVTX Inner Layer Concept

All-silicon module < 0.15 % X_0

4 contiguous sensors diced as a block from the wafer
Redistribution layer for interconnection
Heterogeneous thinning for thinness & stiffness

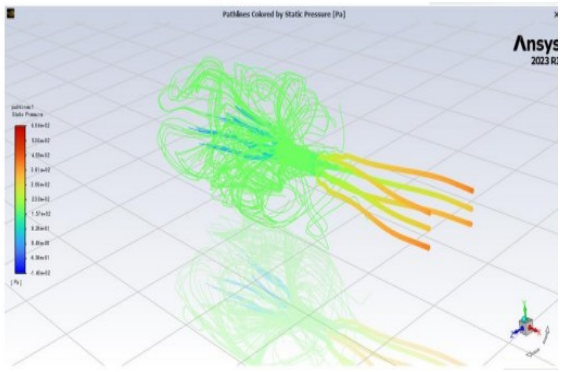


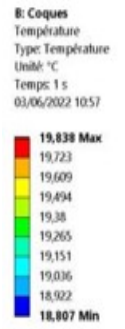
Prototyping

First real-size ladders at IZM-Berlin with dummy Si
True iVTX geometry available

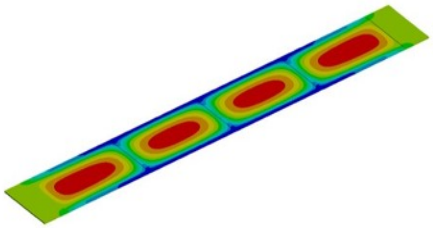
Simulation on cooling

Dry air cooling 15°C
Assume 200 mW/cm^2

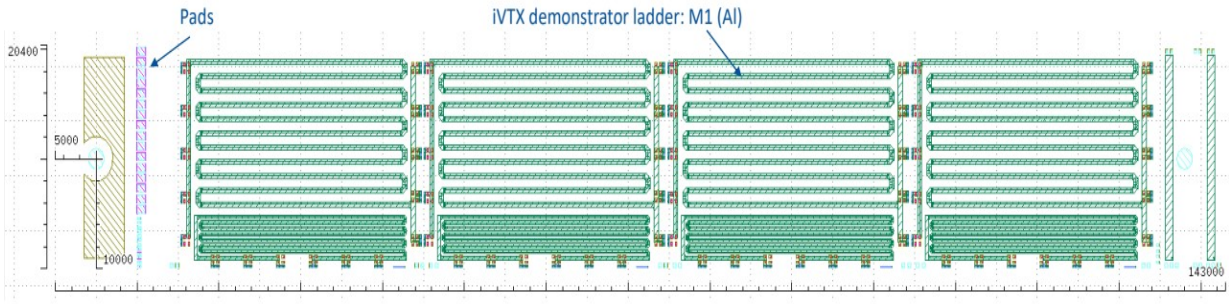


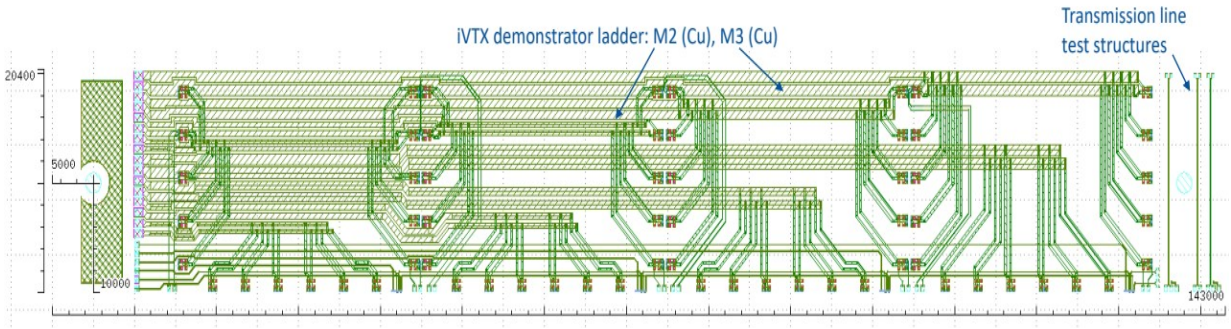


T_{MAX} ~ 20°C
ΔT < 5°C



iVTX Ladder Demonstrator





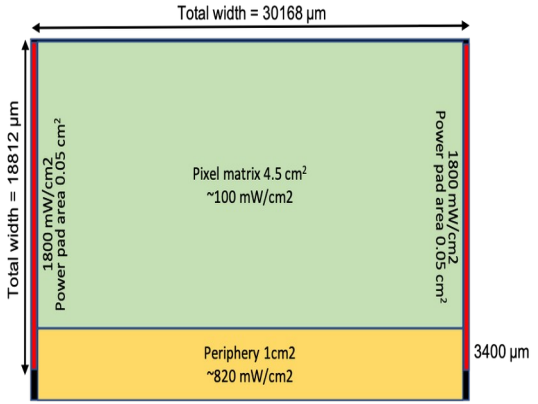
Metal system:

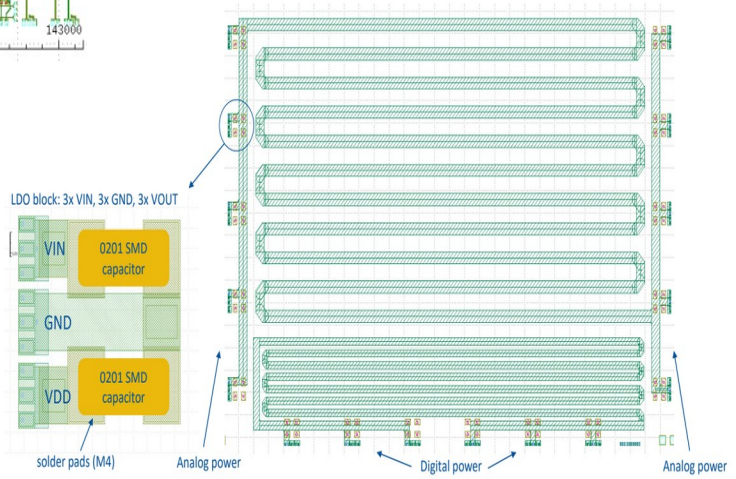
- Resistive heaters: 1.5 um Al (M1)
- 2 RDL metal layers: 3 um Cu (M2, M3)
- Top metal finish: NiAu (M4)

Wirebonding, SMD soldering

Final ladder dimension: 143 x 20.4 mm^2
Dummy heaters: 30 x 20 mm^2
Prepared for 1.7 mm mounting hole

Characterization of electrical, mechanical and thermal performance of iVTX ladders



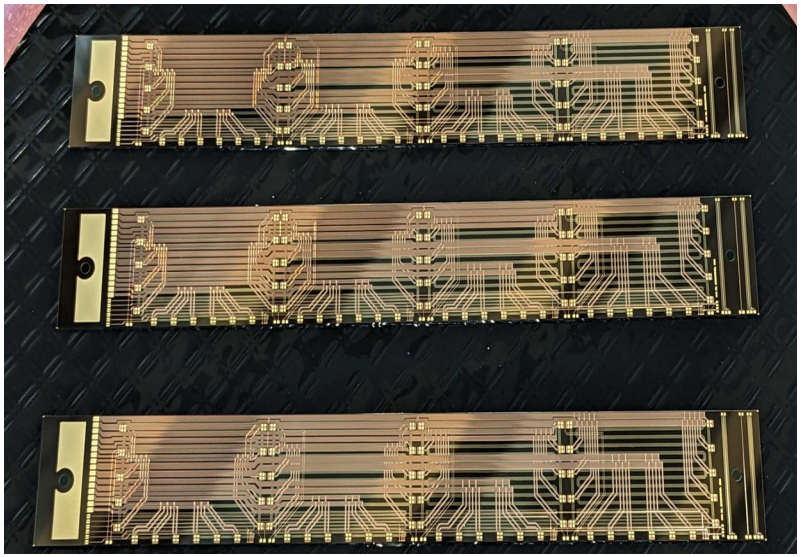


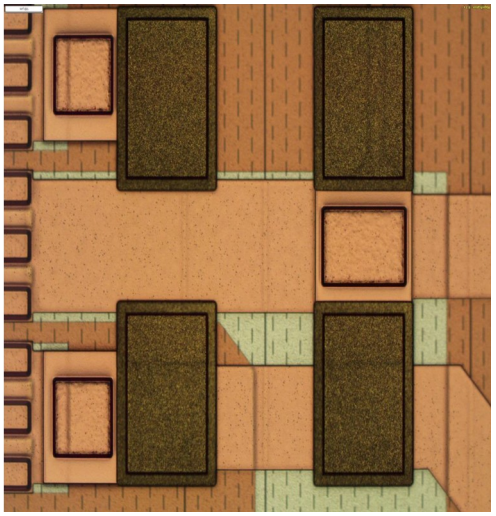
iVTX Ladder Demonstrator

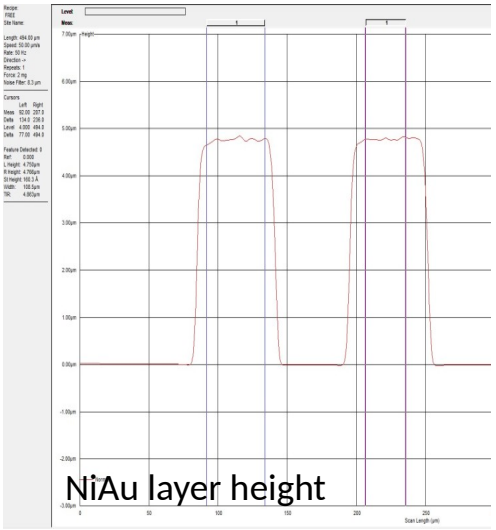
First demonstrators arrived at IFIC:
8 Wafers (725 µm, 400 µm, 300 µm)

Production at IZM finished smoothly

Characterization starting



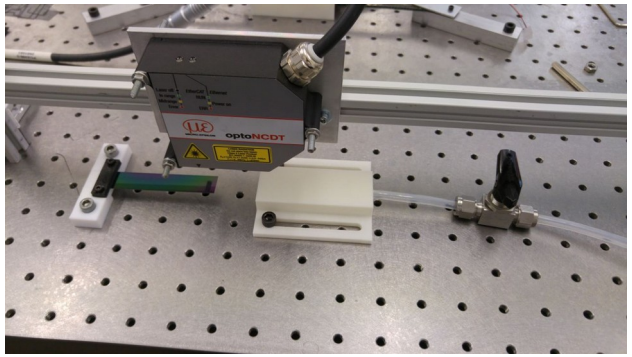




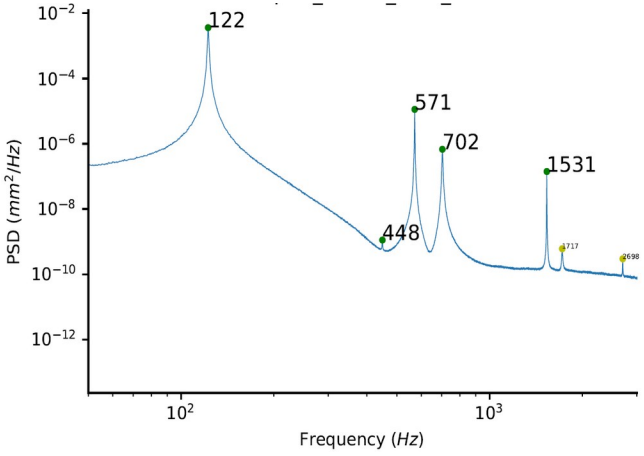
NiAu layer height

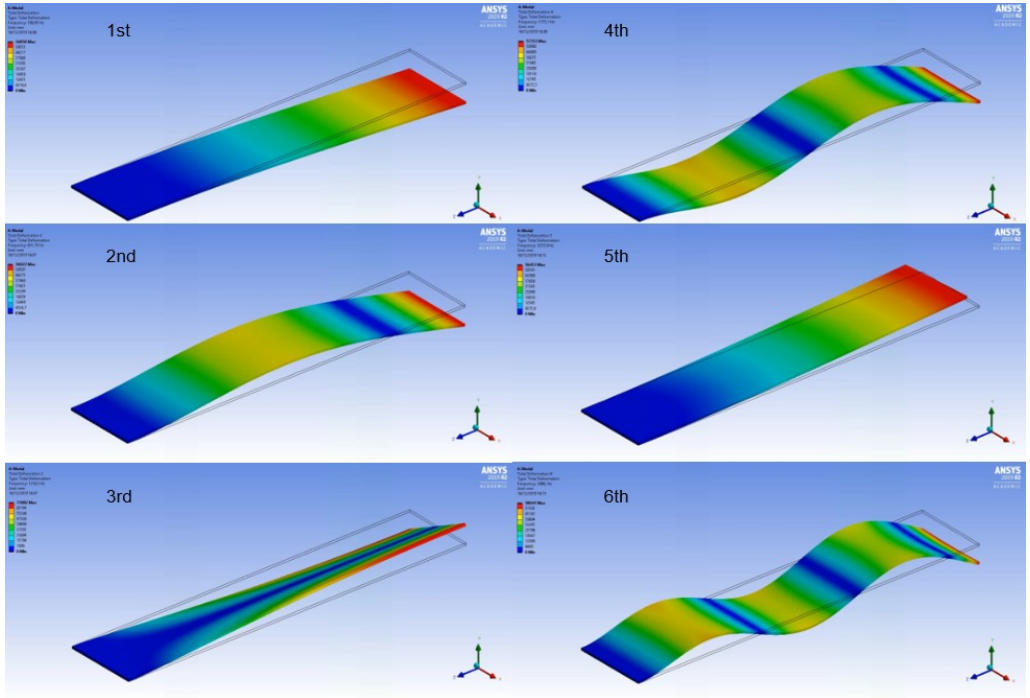
Measurements

Multiple silicon structures measured in Oxford and Valencia

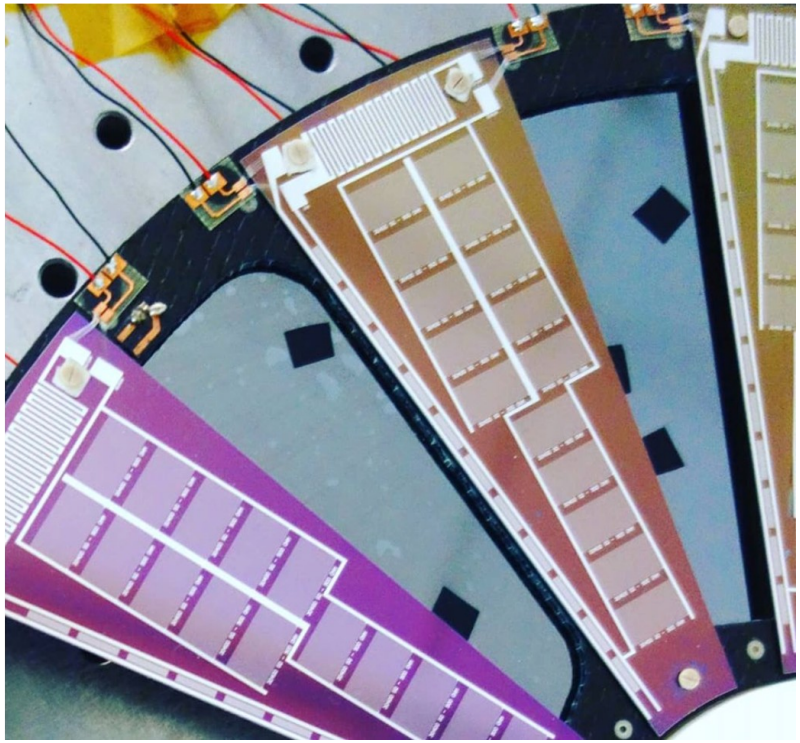


Vibration Setup – IFIC Valencia





Vibration analysis



Master's thesis Yamal Naser Requena

Analytical expressions

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ANSYS FEA

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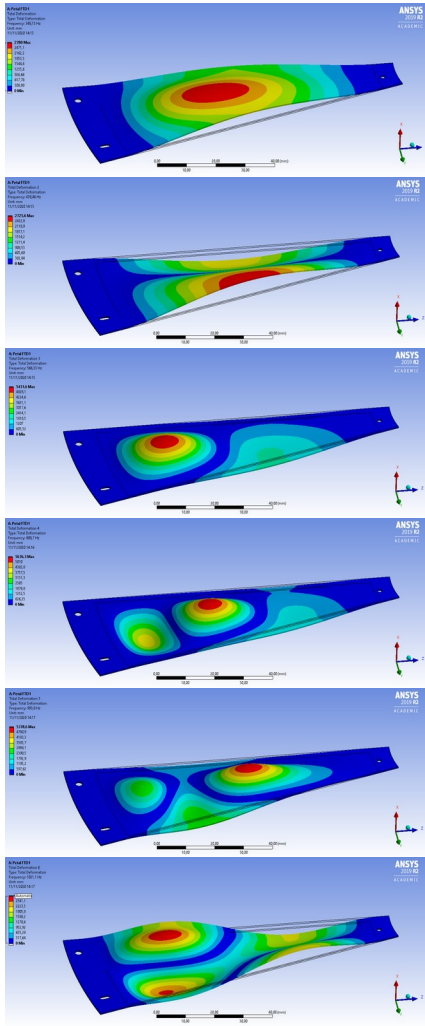
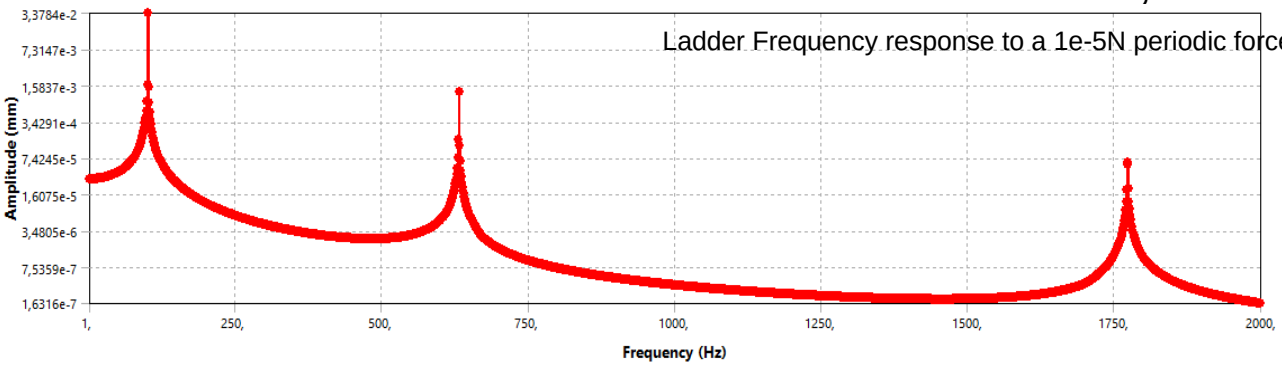
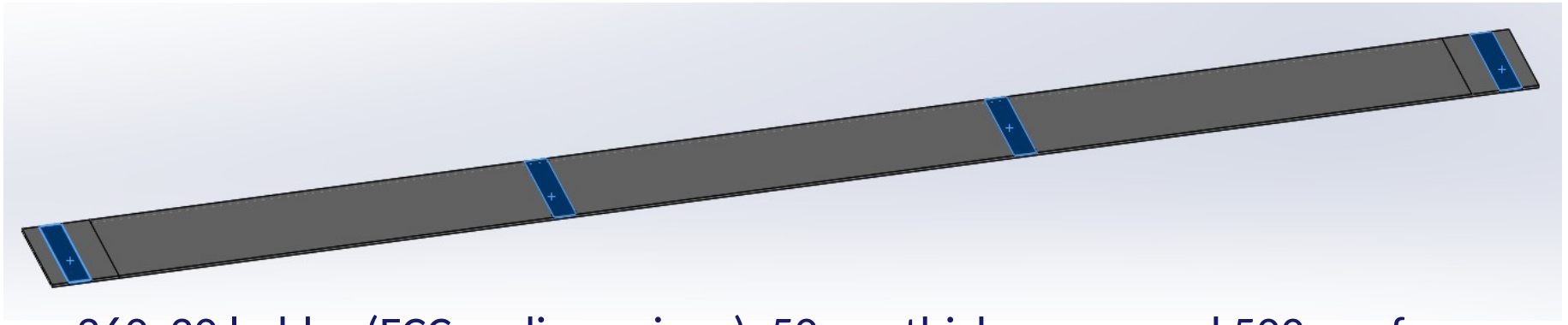
Measurements

Extend to more realistic vibration loads (air flow, cavern floor, earthquake)





Support structures



260x20 ladder (FCCee dimensions), 50 um thick sensor and 500 um frame

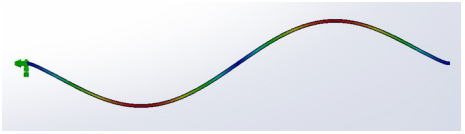
Use eigenfrequencies as figure-of-merit for mechanical stiffness

Conclusion: need reinforcement from out of the ladder plane

ALICE's bent vertex detector achieves a similar rigidity as the solution with 4 support points

	IT01	IT02 – 3ps	IT03 – 4ps
Mode 1	67	264	584
Mode 2	184	270	589
Mode 3	212	447	608
Mode 4	356	447	799
Mode 5	380	713	814
Mode 6	575	722	837

Eigenfrequencies (in Hz)

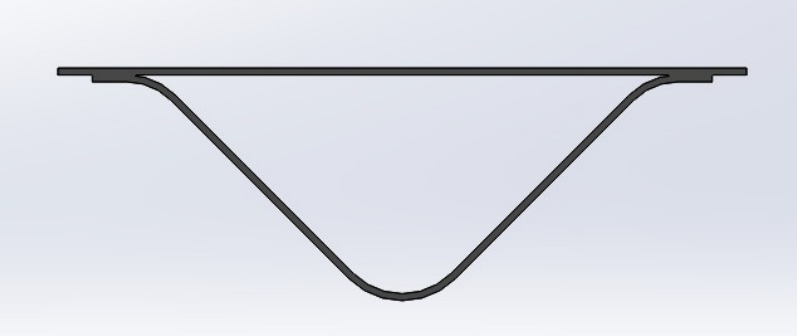


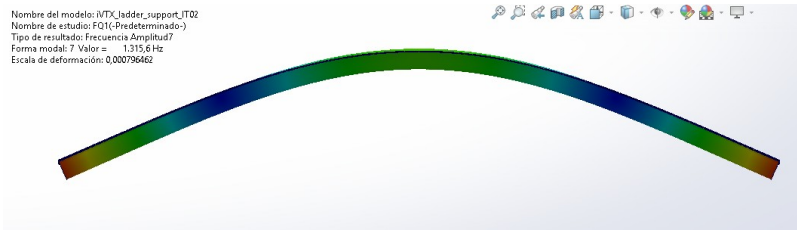
2-3-4 points of support

Support structures

Carbon laminate support structure (0,2 mm thickness)

- Silicon ladder to be glued on top.
- Natural frequencies are very high. Excellent stiffness.





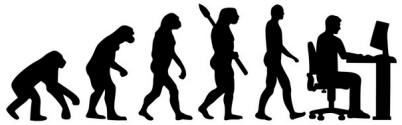
Modos de lista

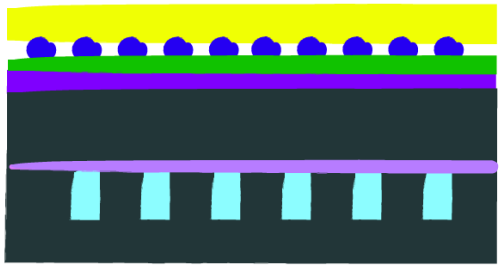
Nombre de estudio:FQ1

Nº de modo	Frecuencia(Rad/seg)	Frecuencia(Hertz)	Período(Segundos)
7	8.266,1	1.315,6	0,00076011
8	19.836	3.157	0,00031675
9	21.502	3.422,2	0,00029221
10	35.472	5.645,6	0,00017713
11	39.861	6.344,1	0,00015763
12	42.683	6.793,2	0,00014721

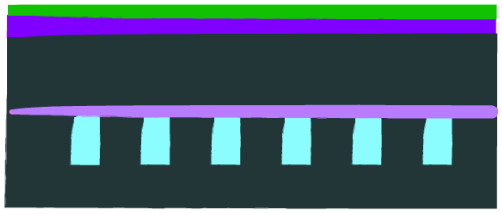
Cerrar Guardar Ayuda

MCC evolution: integrated cooling

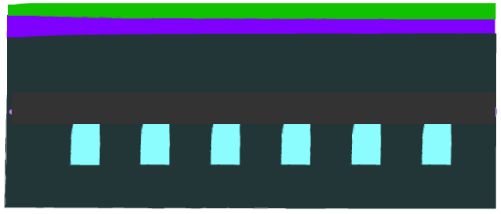




Hybrid pixel detector &
micro-channel cooling plate

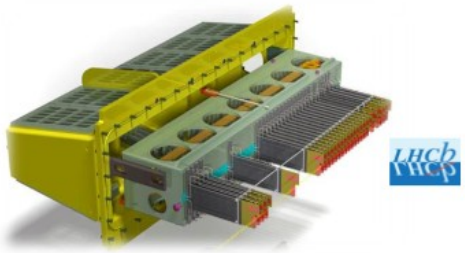


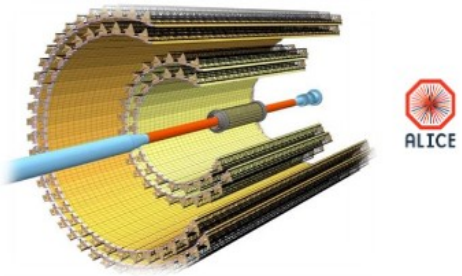
Monolithic CMOS detector

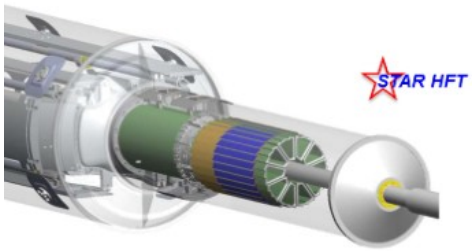


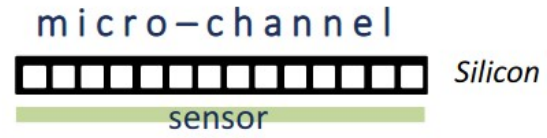
Monolithic CMOS detector
with integrated micro-channels

Ultra-light cooling









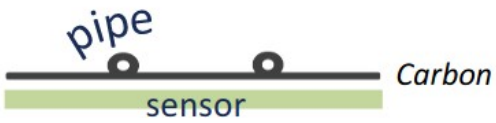
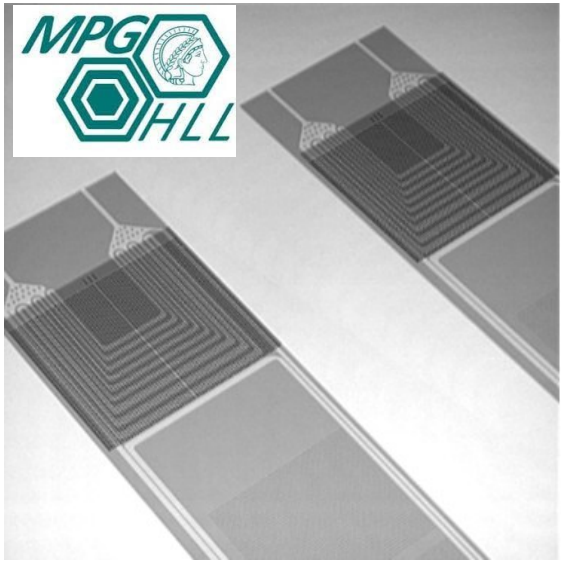
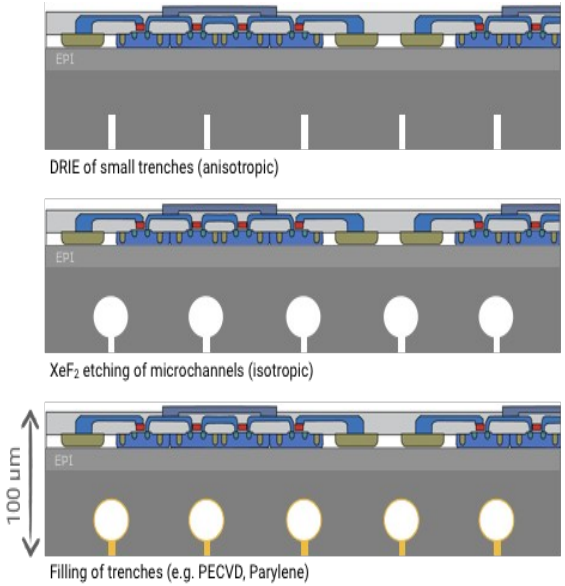


Image from Corrado Gargiulo

Integrated micro-channels

- 2016: Developed process to integrate micro-channels in DEPFET Silicon sensor (with MPG-HLL, JINST11(2016) 06)





M. Boscardin et al., NIM A, 2013
C. Lipp, MSc Thesis, EPFL, 2017
I. Berdalovic et al., JINST 13 C01023, 2018

2019: Buried micro-channels in working MALTA CMOS sensor (CERN, EPFL)

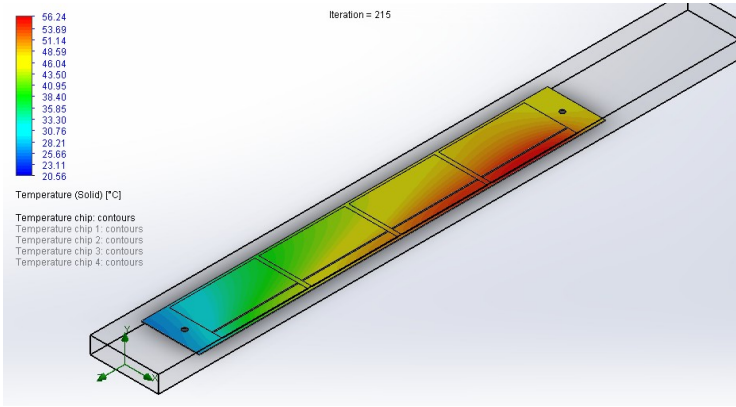
Who needs μ-channels?

The FCC-hh vertex detector and tracker operate in extreme radiation levels and rate environment; would definitely benefit from minimal thermal gradient between sensor and heat sink (but 2073 is a long time from now)

STAR and ALICE can safely operate with air cooling. Belle 2 has a hybrid system with active elements in the high-power area and air cooling over the sensor area.

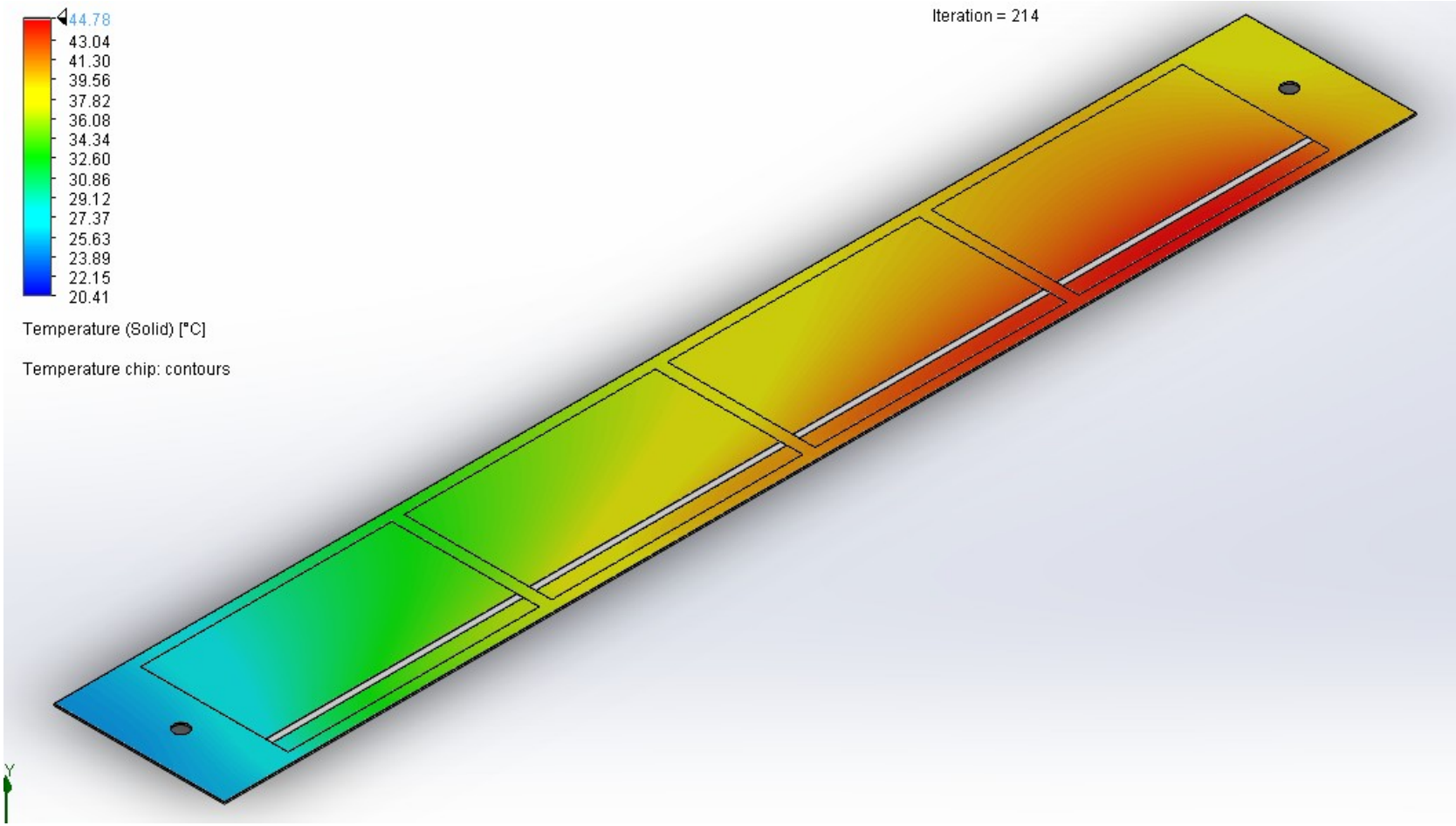
What about the Higgs factory?
- Linear Colliders have power pulsing; probably OK with just air flow
- Circular Collider is a DC machine; on the edge?

Simulate All-Silicon ladder
- dimensions as per iVTX for Belle 2:
--- 143 x 20,4 mm^2, to compare with measurements
- power consumption:
--- average 200 mW/cm2
--- nearly 1 W/cm2 in chip periphery
(note: ALPIDE consumption is significantly less;
reasonable estimate for the FCC environment?)

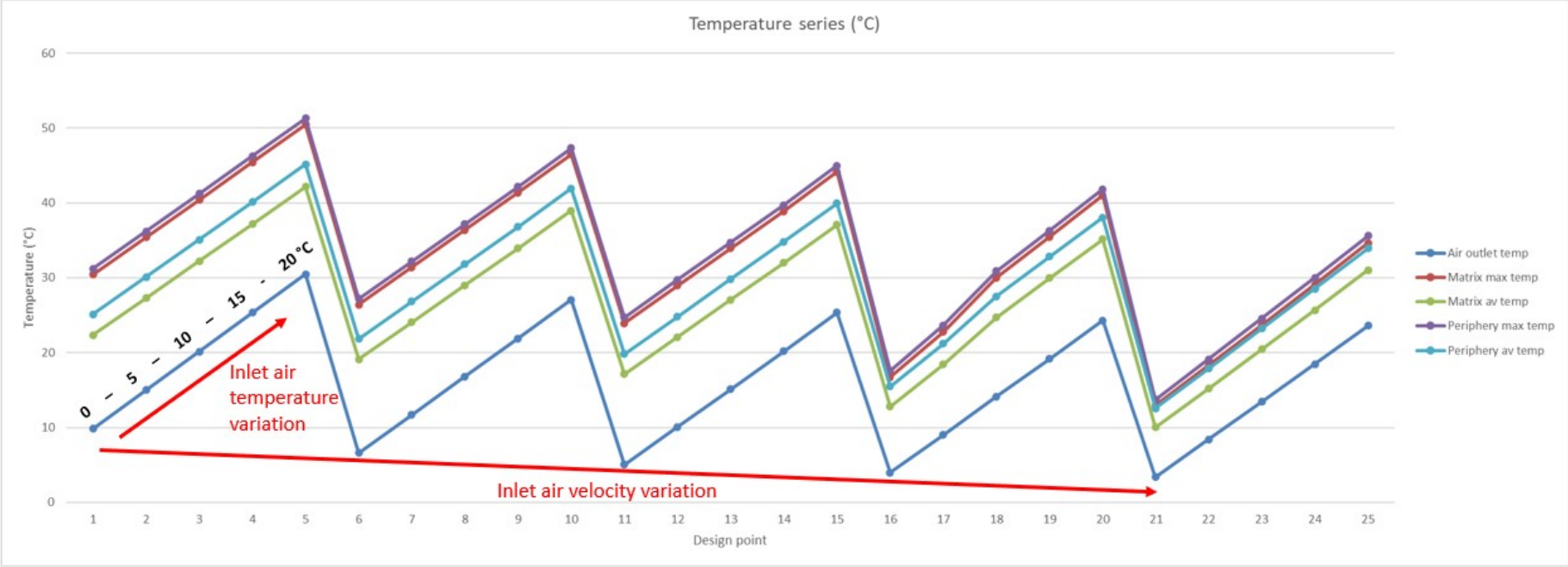


Design point - 20 °C - 8 m/s

iVTX ladder temperature. Inlet temperature 20 ºC at 8 m/s. Tmax = 45 ºC.



Results – parametric study



- Air inlet temperature: 0 – 5 – 10 – 15 - 20 °C (bottom to top trend)
- Air inlet velocity: 4 – 6 – 8 – 10 – 12 m/s (left to right trend)

  Apparently, none of the combinations satisfy the requirement of $\Delta T < 5^{o}$ C

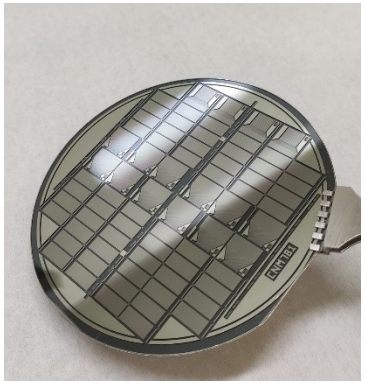
Micro-channels

- PRELIMINARY: A solution based on micro-channels and air cooling, with a single micro-channel with monophase liquid cooling along the chip periphery and a gentle flow of air over the sensor seems to meet our cooling requirements, even with a 200 mW/cm2 power consumption
- At FCCee, also the beam pipe is cooled. Should we aim for an integrated solution with FCCee beam pipe?
- Will develop a complete and near-optimal design, discuss with the relevant people (Fabrizio Palla, DRD8.1), and produce a prototype at CNM in Barcelona

WP10 – CSIC - NEWS

Deliverable D10.1 due this summer!!

Contributions on Silicon Micro-channels:
- CNM anodic/eutectic bonding (see M. Ullan)
- HLL direct bonding (see L. Andricek)
- INFN effort on CoolFPGA (see L. Bosi)
- buried channels currently uncovered



To be merged with material from others on 3D-printed structures

Grant Agreement No: 101004761

AIDAinnova

Advancement and Innovation for Detectors at Accelerators

Horizon 2020 Research Infrastructures project AIDAINNOVA

MILESTONE REPORT

COMBINED WORKPLAN WITH OBJECTIVES AND TEST DEFINITION FOR ALL TECHNOLOGIES

MILESTONE: MS41

Document identifier:	AIDAinnova_MS41.docx
Due date of milestone:	End of Month 11 (February 2022)
Justification for delay:	[if delays occurred]
Report release date:	07/03/2022
Work package:	WP10: Advanced mechanics for tracking and vertex detectors
Lead beneficiary:	CERN
Document status:	Draft

CSIC-IFIC summary

Aim: integrate support structures and micro-channel cooling in “large” CMOS ladders for Belle 2 upgrade and Higgs factories

Development of low-temperature bonding compatible with CMOS post-processing ongoing at CNM and HLL (see talks by L. Andricek and M. Ullan)

IFIC hired Carlos Orero (industrial engineer) with AIDAinnova funding and Adrian Irles’ “proyecto de consolidación”; currently starting a 3-year contract!

New Finite-Element simulations to study Higgs factory cooling and mechanical solutions: comparison with mechanical prototypes is ongoing and a cooling prototype is being designed for production at CNM.