Update from CERN and UniUD

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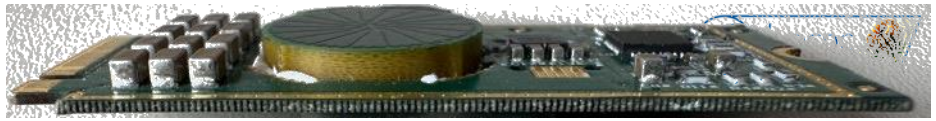
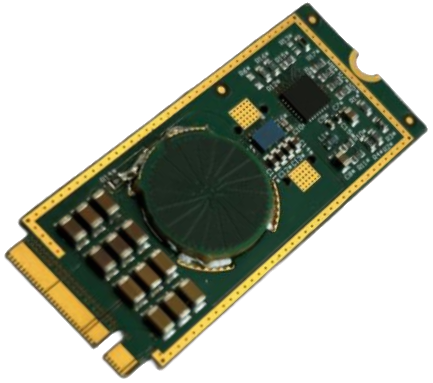
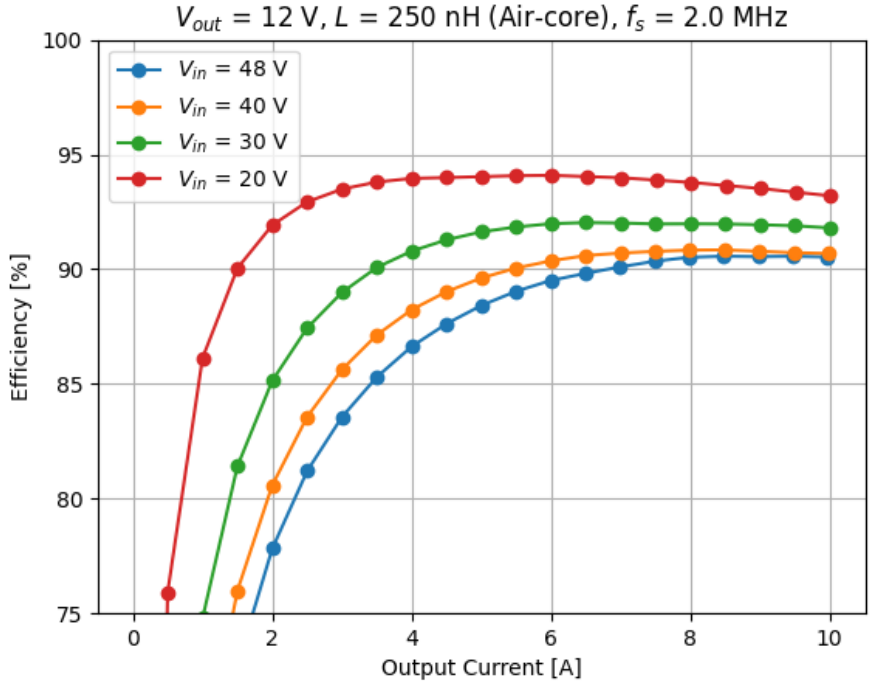
bPOL48V: some important news

- Industrial testing is under development, tested chips will be available in Feb 2025
- EPC released the final version of the EPC2152, tested with TID up to 400Mrad w/o issues
- production ready modules have been presented at TWEPP, 300 modules are in production (with PCB inductor as well)
  50 samples in travel to CERN this week

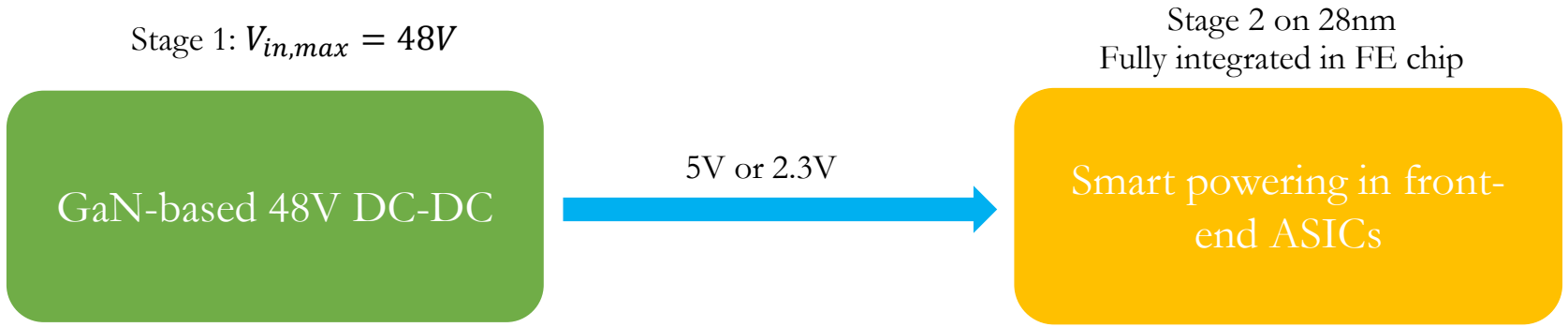




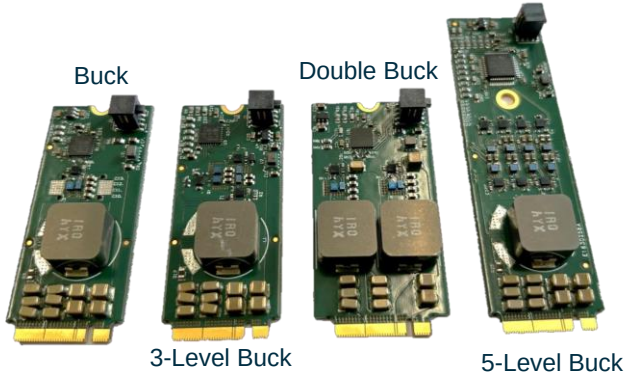
55mm x 24mm x 3mm



On-going RD


Stage 1: $V_{in,max} = 48V$
GaN-based 48V DC-DC
5V or 2.3V
Stage 2 on 28nm
Fully integrated in FE chip
Smart powering in front-end ASICs

GaN based 48V DCDC



48V Converters

TECHNOLOGY

- Currently using OnSemi I4T
- Investigation a new technology (BCD8s from ST) for radiation tolerance: 3 testchips submitted in Nov24

TOPOLOGY

Several converter topology are investigated for evaluating the best efficiency for high conversion ratio (48V -> 5V and 48V->0.9V)

DESIGN

Currently on a new controller + power stage that can replace both bPOL12V and bPOL48V

TESTING

- A new compact test board has been developed to perform testing of DCDCs (functional + TID)
- A more advanced board has been also developed for SEE testing

Smart powering in 28nm front-end ASICs

TESTING

Big testing campaign in 2024 on the 3 prototypes

- iPOL5V
- iPOL2V3
- linPOL1V2

28nm Converters

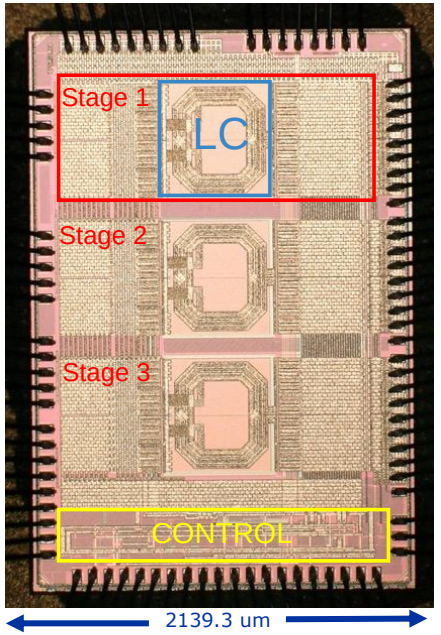
TEST SETUPs

A rack is under development for reliability, hosting 60 iPOLs converters in a stand-alone modules.
They will be running at max Vin and max Iout

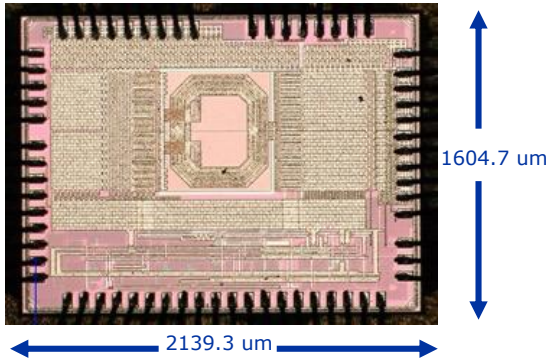
DESIGN

iPOL2V3 re-submitted in Nov24 along with the SoC, first real application.
Few improvements done and added linear regulators from 2.3V or 5V down to 0.9V + test structures (UniUD)

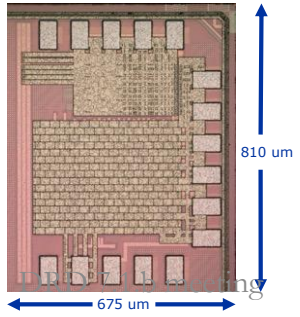
iPOL5V (5V -> 0.9V) max 400mA



iPOL2V3 (2.3V -> 0.9V) max 200mA

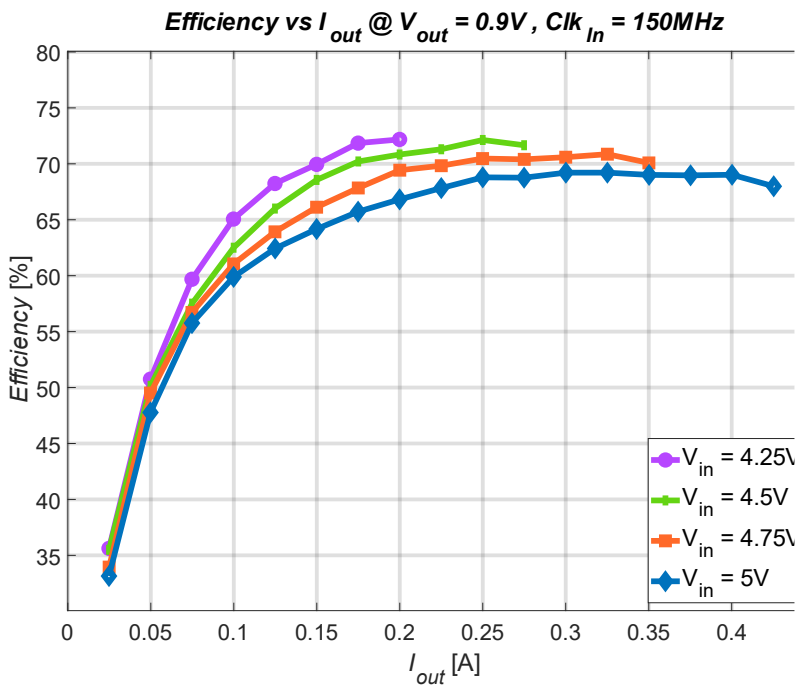


linPOL1V2 (1.2V -> 0.9V) max 200mA

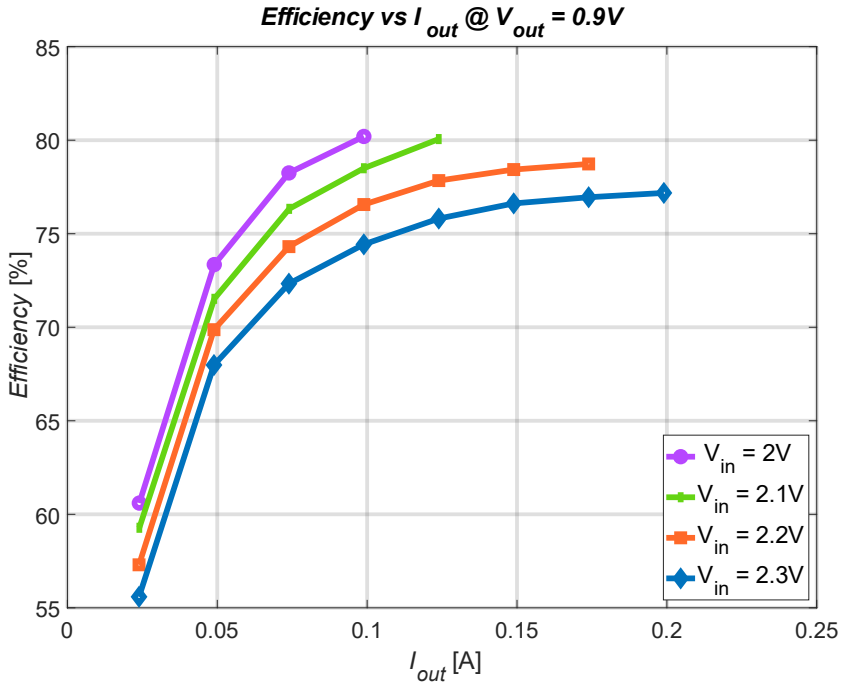


Electrical performance of 28nm ASICs

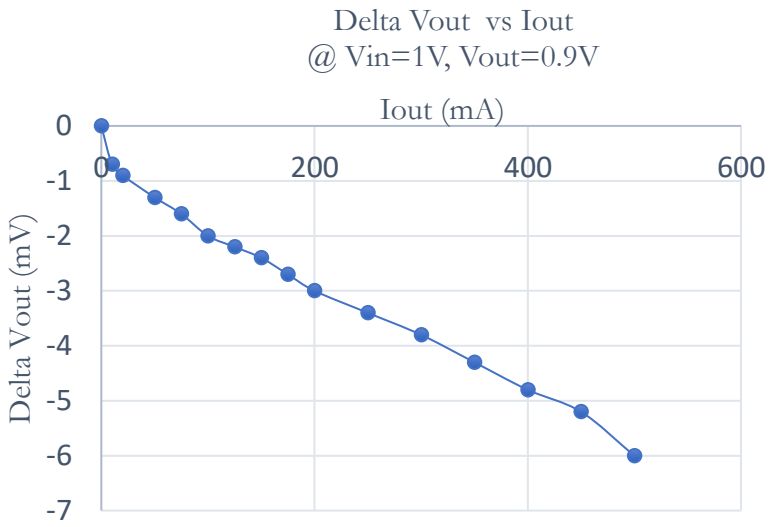
iPOL5V



iPOL2V3

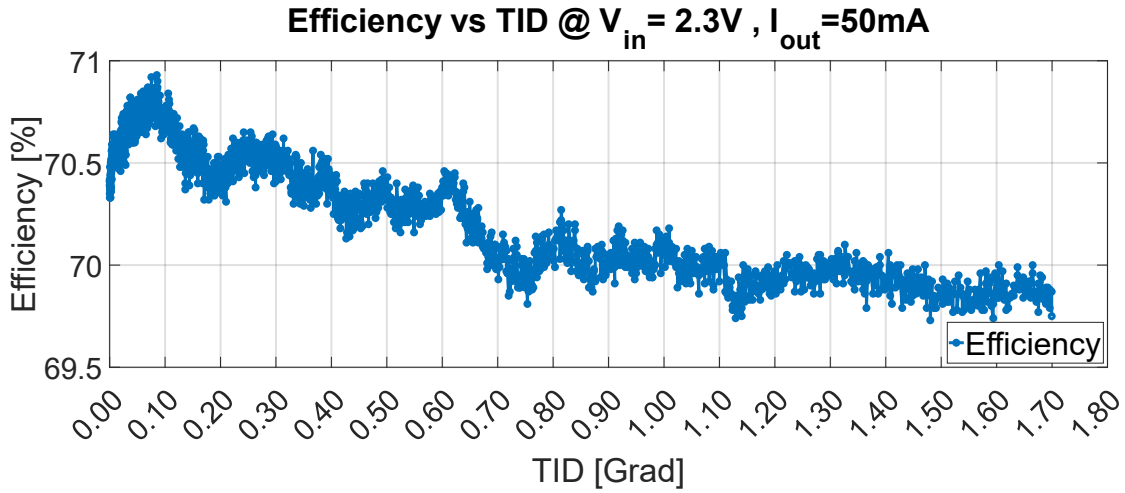


linPOL1V2

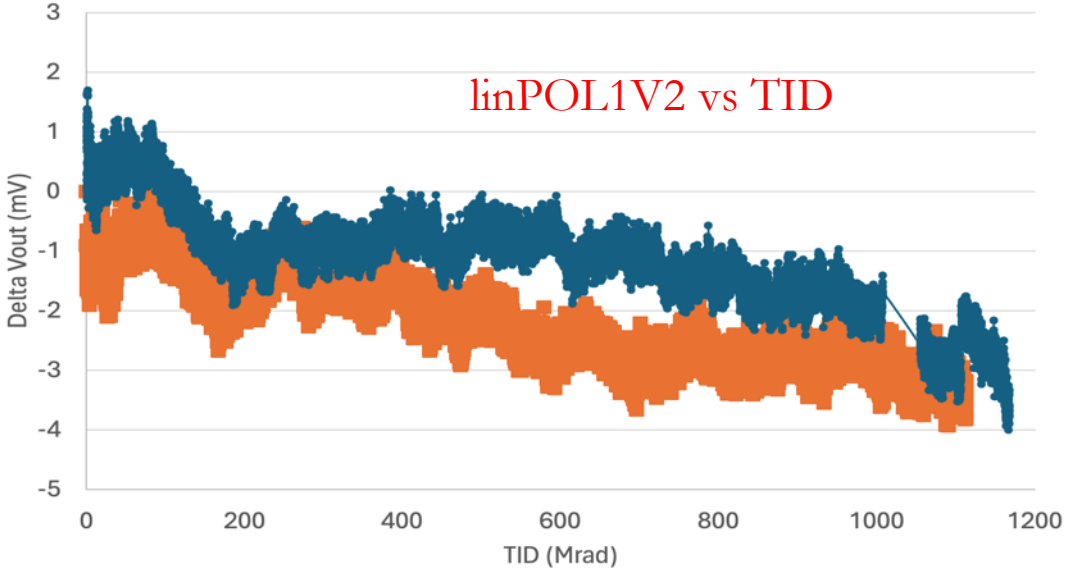


TID testing of 28nm ASICs

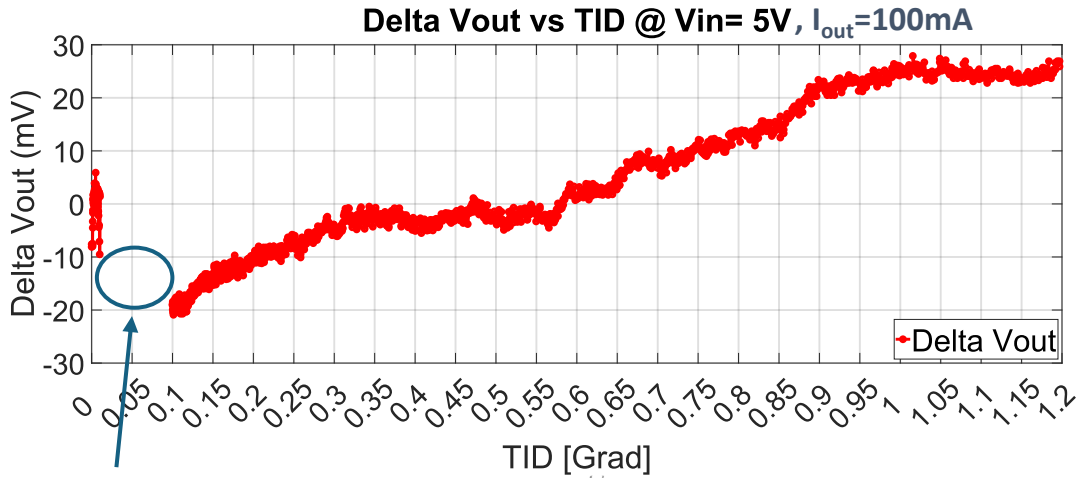
iPOL2V3 vs TID



linPOL1V2 vs TID



iPOL5V vs TID



Functional issue due to 5V Nwells-Psub leakage

Contribution of UniUD

University of Udine (UniUD) contributed with the idea of the topology used for iPOL5V and iPOL2V3 and its improvement for HEP applications

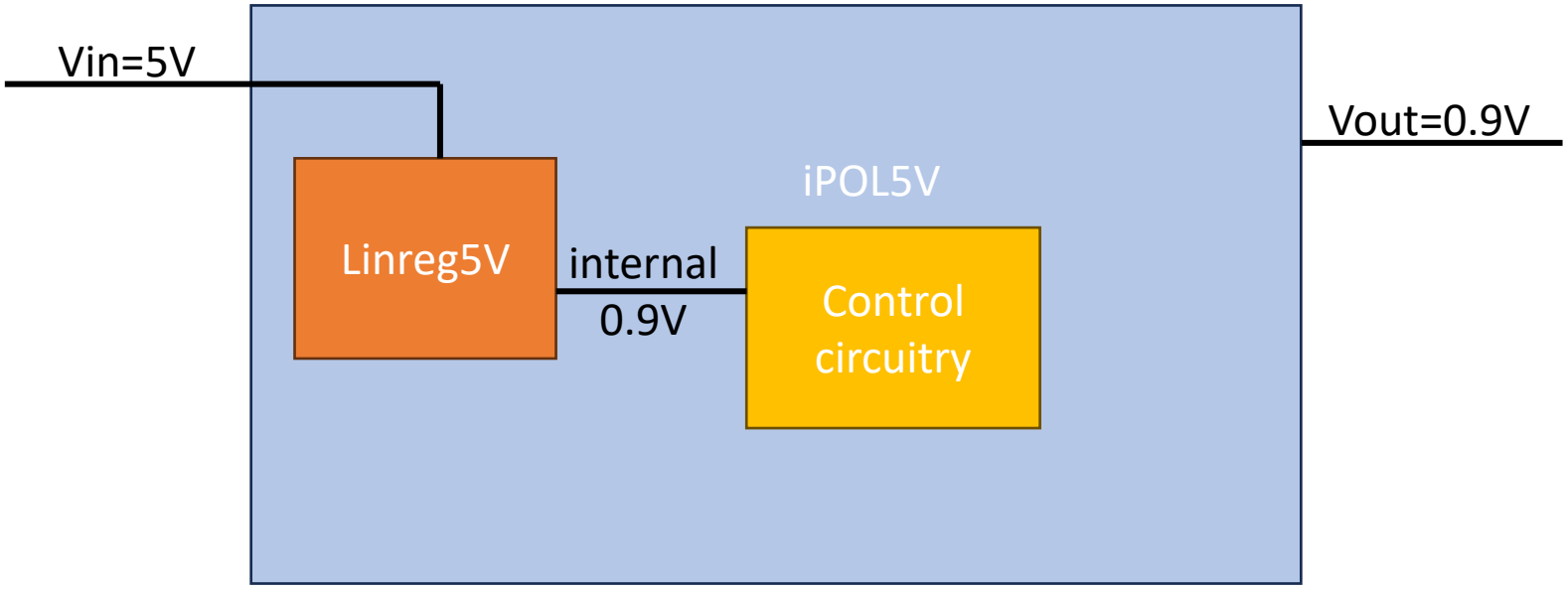
In the first prototype iPOL5V and iPOL2V3 have the control circuitry supplied by an external 0.9V.

Stefano Saggini designed for this purpose two linear regulators to supply the 0.9V from the input line.

from 5V to 0.9V (Linreg5V) for iPOL5V

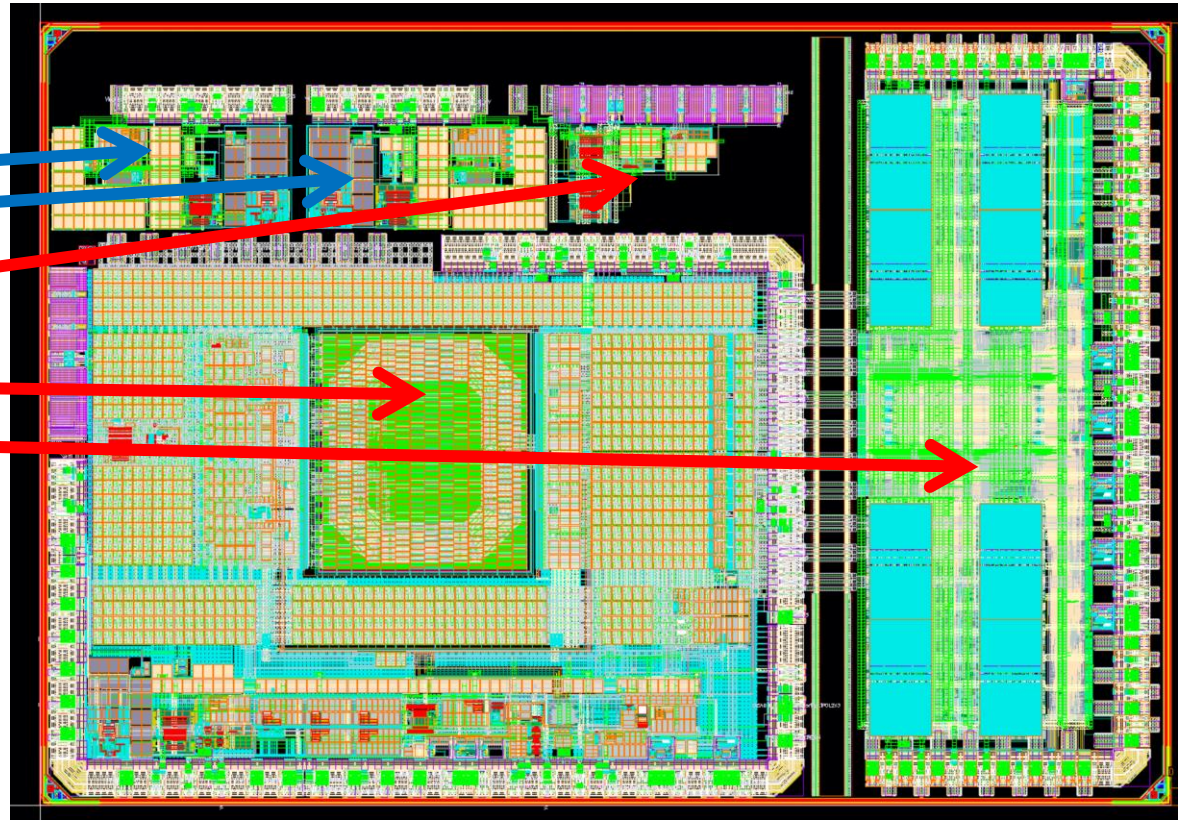
2.3V to 0.9V (Linreg2V3) for iPOL2V3

The two designs have been integrated in the Nov 2024 submission



Plans for 2025

1) Testing of the chips in the Nov 2024 submission
   Large MPW composed of
      Linreg2V3
      Linreg5V
      testchip for the Nwell leakage current
      iPOL2V3 (with fix for the Nwell leakage current)
      SOC from RD5.4 (microcontroller)
   First use of iPOL2V3 for supplying a 28nm chip



2) We are aiming a submission in I4T of a controller + power stage for replacing in long term bPOL12V and bPOL48V

Conclusions

Legacy converters bPOLs:

- New modules of bPOL48V available
- Gan_Controller for bPOL48V will be industrially tested, ASICs available on Feb 25

New RD on going

- 2 stage based
- 48 to 2.3V/5V under development in a new HV technology exploring new architecture as well
- 3 POL have been developed in 28nm technology: iPOL5V, iPOL2V3 and linPOL1V2. All three working fine, tested up to levels above 1Grad. We found a TID on iPOL5V, it has been corrected and re-submitted.