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DEGLI STUDI
DI UDINE**

Update from CERN and UniUD

Stefano Michelis, on behalf of the CERN power distribution team

Stefano Saggini, University of Udine

07/02/2025

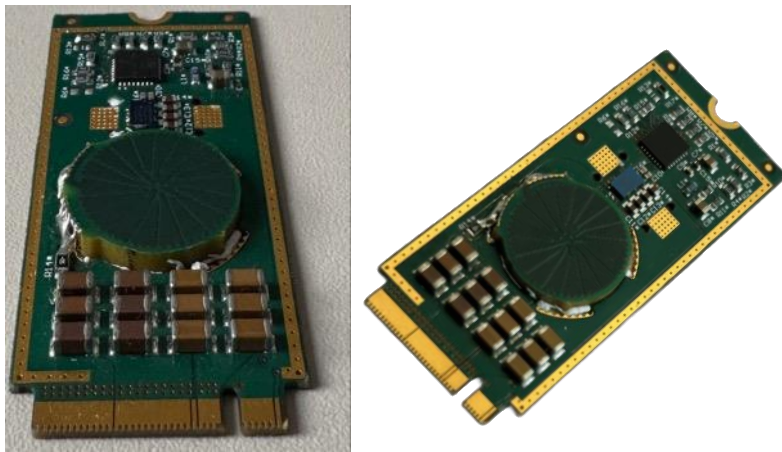
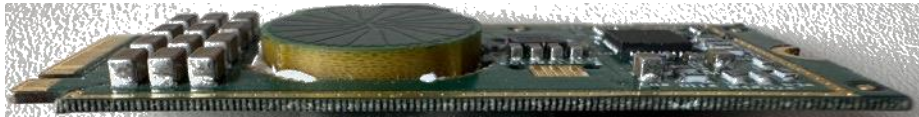
Status of the funds



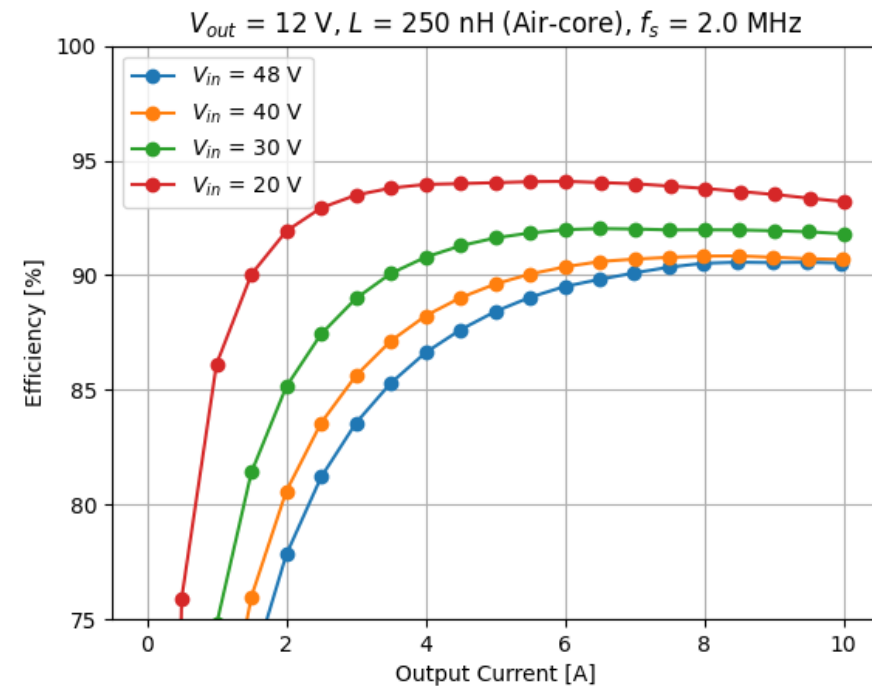
- CERN has the funds from EP RD 5.4 package, for the next 3 years. Equivalent is around 100KCHF/year + 2 Students
- UdiUD has been participating with internal funds in the framework of a collaboration in place for 15 years. UniUD is looking for funds from INFN for a PhD student.

bPOL48V: some improvements

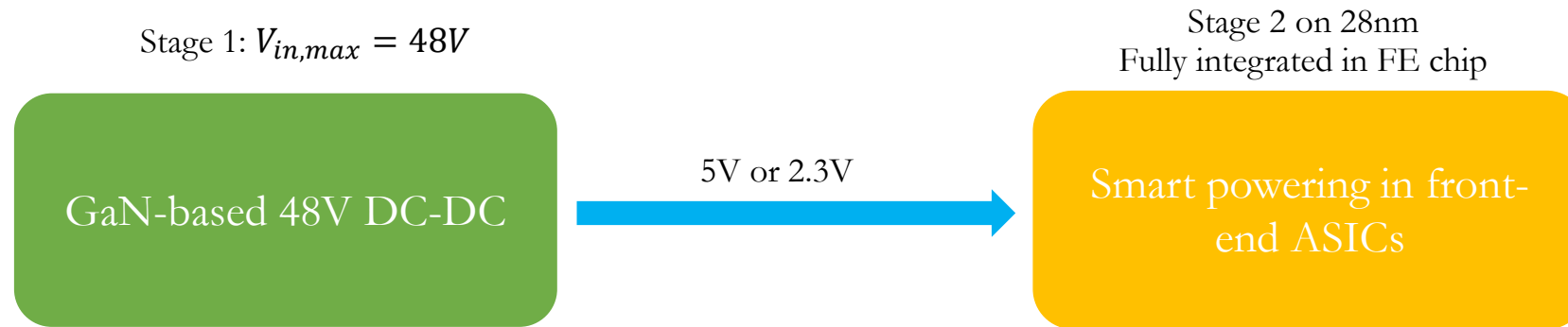
- Industrial testing is under development, tested chips will be available in Feb 2025
- EPC released the final version of the EPC2152, tested with TID up to 400Mrad w/o issues
- production ready modules have been presented at TWEPP, 300 modules are in production (with PCB inductor as well)
50 samples in travel to CERN this week



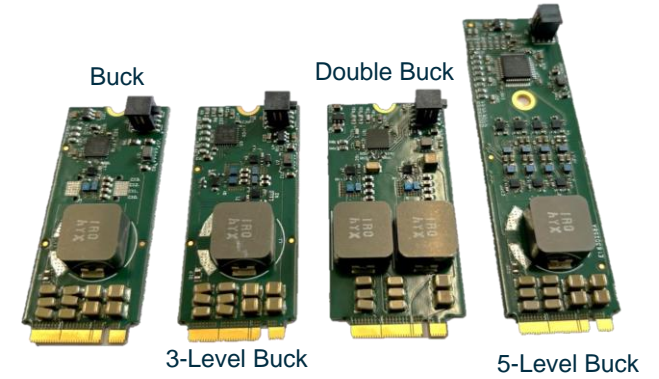
55mm x 24mm x 3mm



On-going RD



GaN based 48V DCDC



TECHNOLOGY

- Currently using OnSemi I4T
- Investigation a new technology (BCD8s from ST) for radiation tolerance: 3 testchips submitted in Nov24

TOPOLOGY

Several converter topology are investigated for evaluating the best efficiency for high conversion ratio (48V -> 5V and 48V->0.9V)

DESIGN

Currently on a new controller + power stage that can replace both bPOL12V and bPOL48V

TESTING

- A new compact test board has been developed to perform testing of DCDCs (functional + TID)
- A more advanced board has been also developed for SEE testing

Smart powering in 28nm front-end ASICs

TESTING

Big testing campaign in 2024
on the 3 prototypes

- iPOL5V
- iPOL2V3
- linPOL1V2

TEST SETUPs

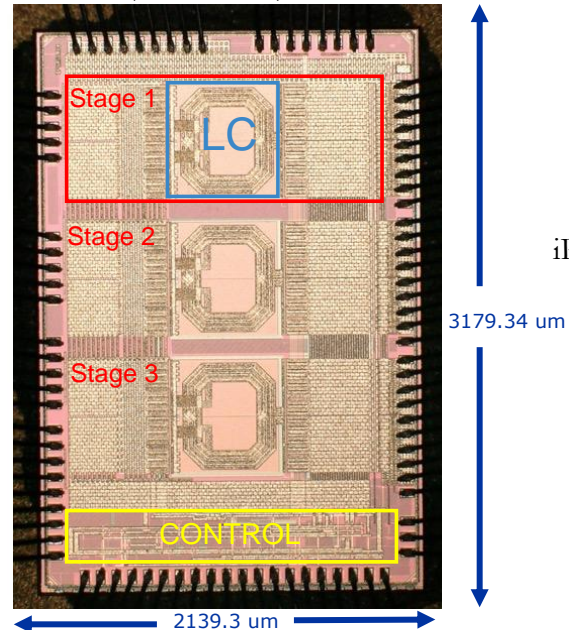
A rack is under development for reliability,
hosting 60 iPOLs converters in a stand-
alone modules.
They will be running at max V_{in} and max
 I_{out}

28nm Converters

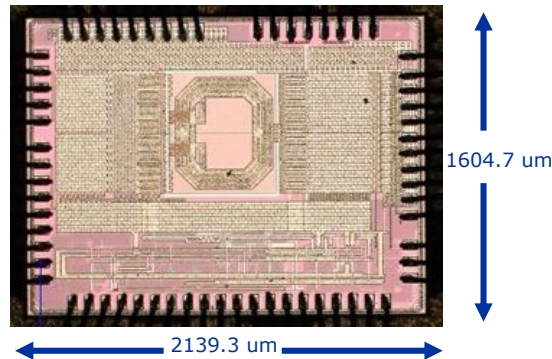
DESIGN

iPOL2V3 re-submitted in Nov24 along
with the SoC, first real application.
Few improvements done and added
linear regulators from 2.3V or 5V
down to 0.9V + test structures
(UniUD)

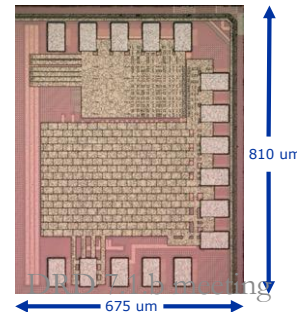
iPOL5V (5V \rightarrow 0.9V) max 400mA



iPOL2V3 (2.3V \rightarrow 0.9V) max 200mA



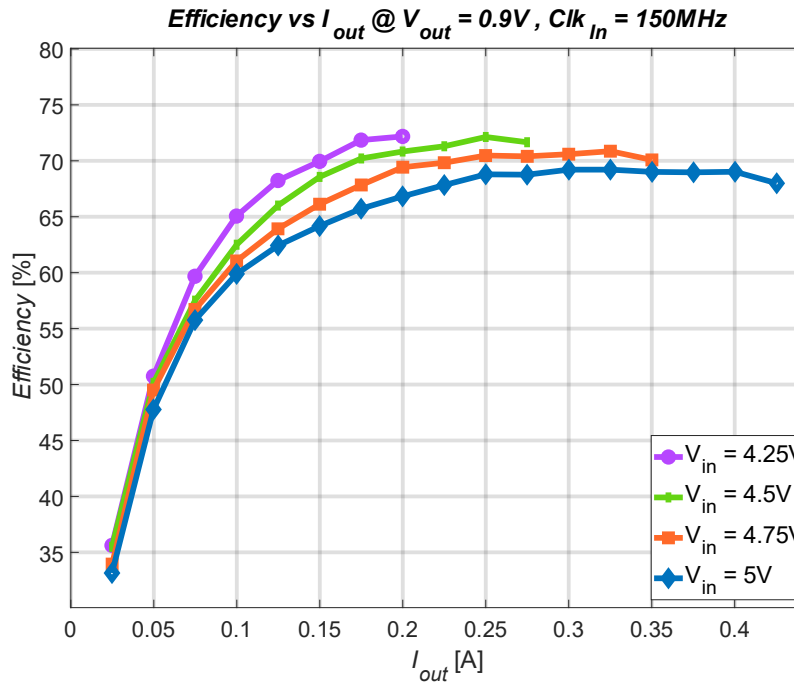
linPOL1V2 (1.2V \rightarrow 0.9V)
max 200mA



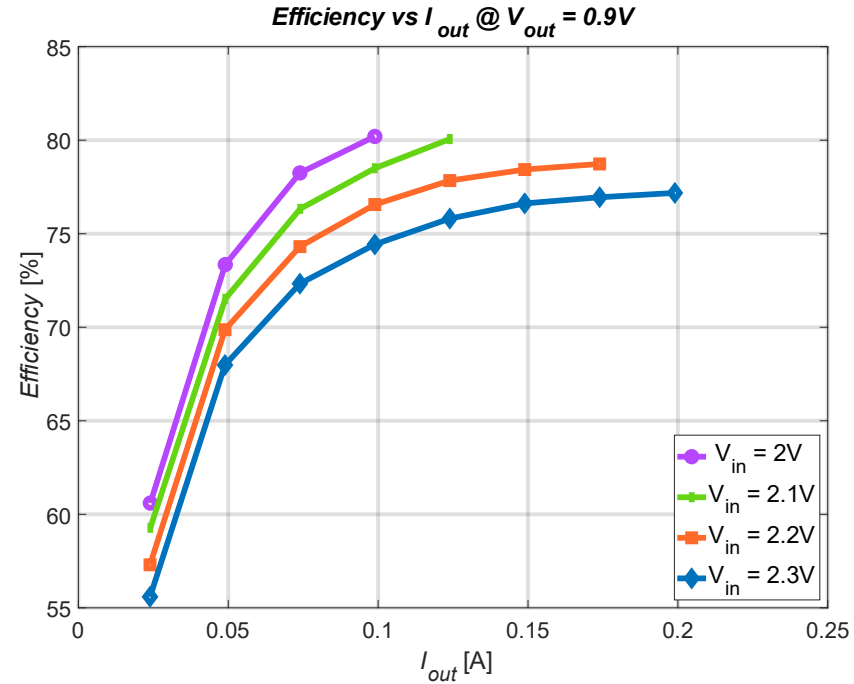
Electrical performance of 28nm ASICs



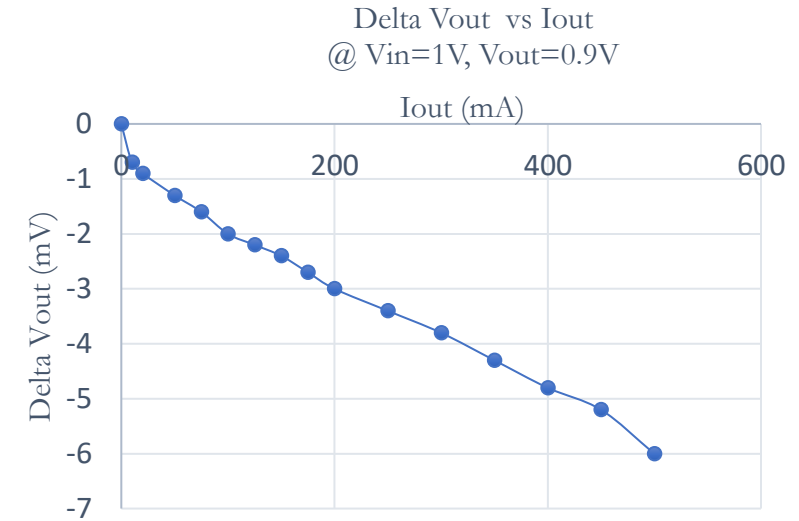
iPOL5V



iPOL2V3



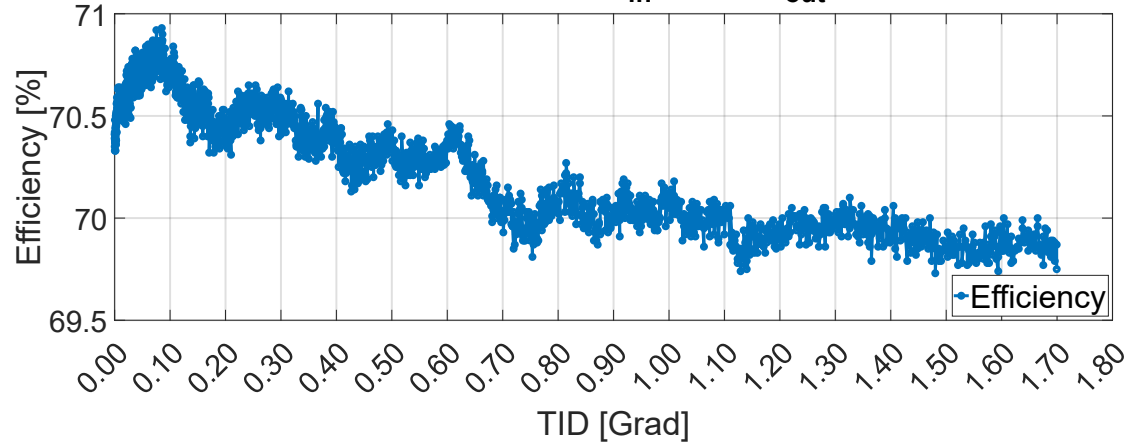
linPOL1V2



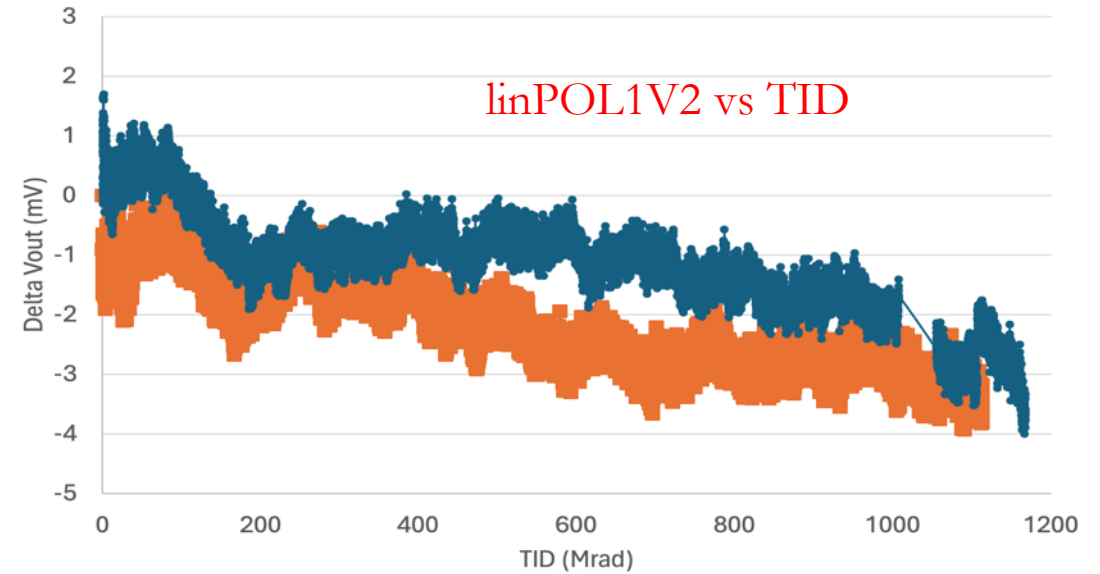
TID testing of 28nm ASICs

iPOL2V3 vs TID

Efficiency vs TID @ $V_{in} = 2.3V$, $I_{out} = 50mA$

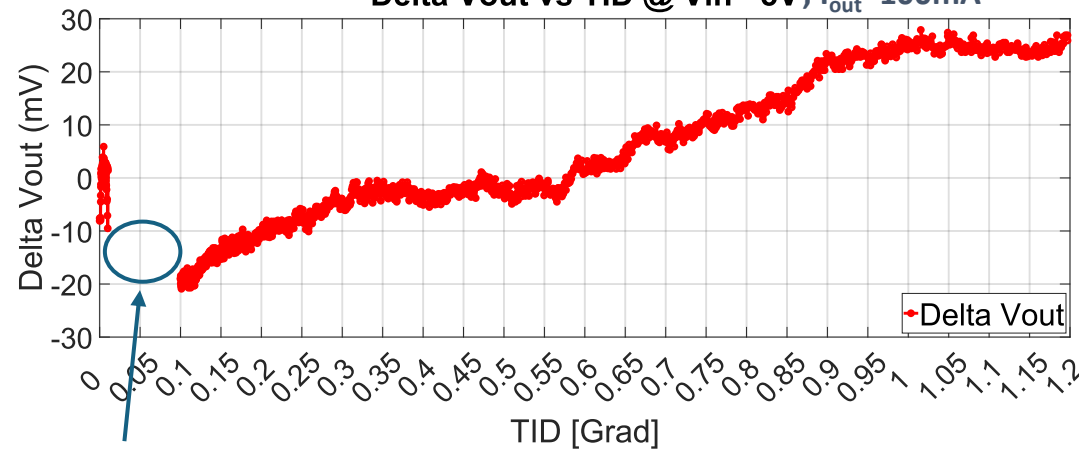


linPOL1V2 vs TID



iPOL5V vs TID

Delta Vout vs TID @ $V_{in} = 5V$, $I_{out} = 100mA$



Functional issue due to 5V Nwells-Psub leakage

Contribution of UniUD

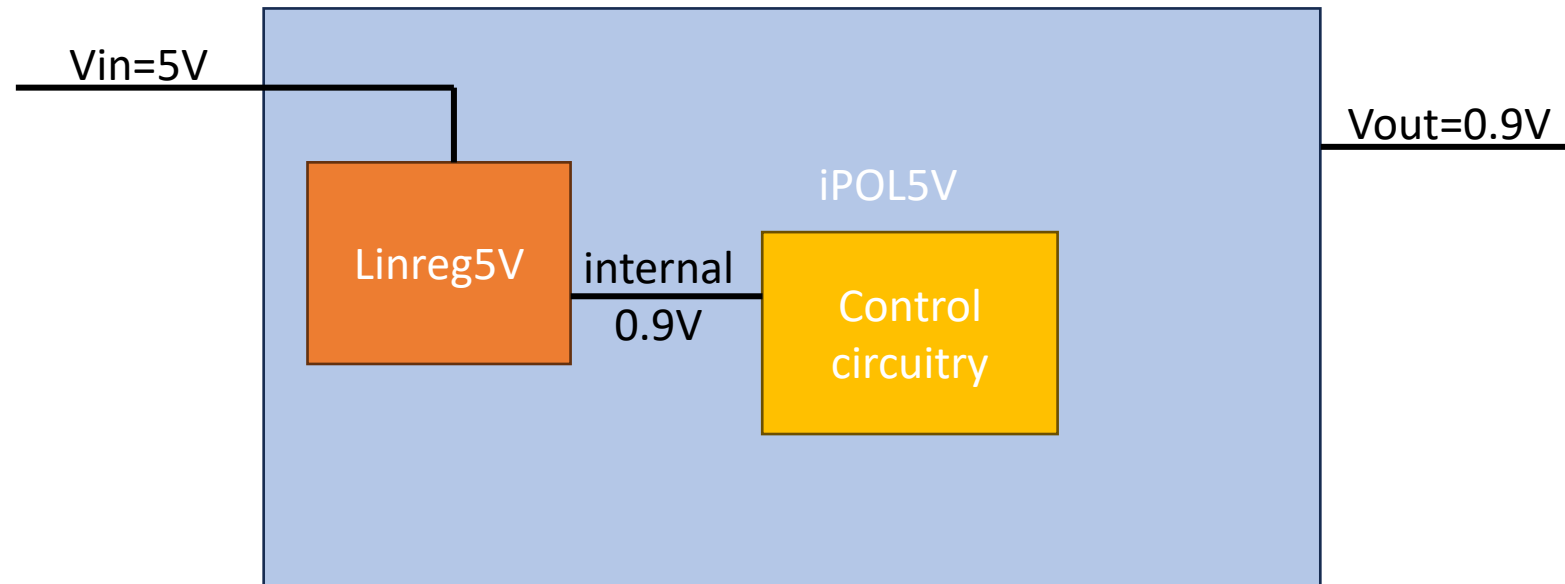


University of Udine (UniUD) contributed with the idea of the topology used for iPOL5V and iPOL2V3 and its improvement for HEP applications

In the first prototype iPOL5V and iPOL2V3 have the control circuitry supplied by an external 0.9V.

Stefano Saggini designed for this purpose two linear regulators to supply the 0.9V from the input line.
from 5V to 0.9V (Linreg5V) for iPOL5V
2.3V to 0.9V (Linreg2V3) for iPOL2V3

The two designs have been integrated in the Nov 2024 submission



Plans for 2025



1) Testing of the chips in the Nov 2024 submission

Large MPW composed of

Linreg2V3

Linreg5V

testchip for the Nwell leakage current

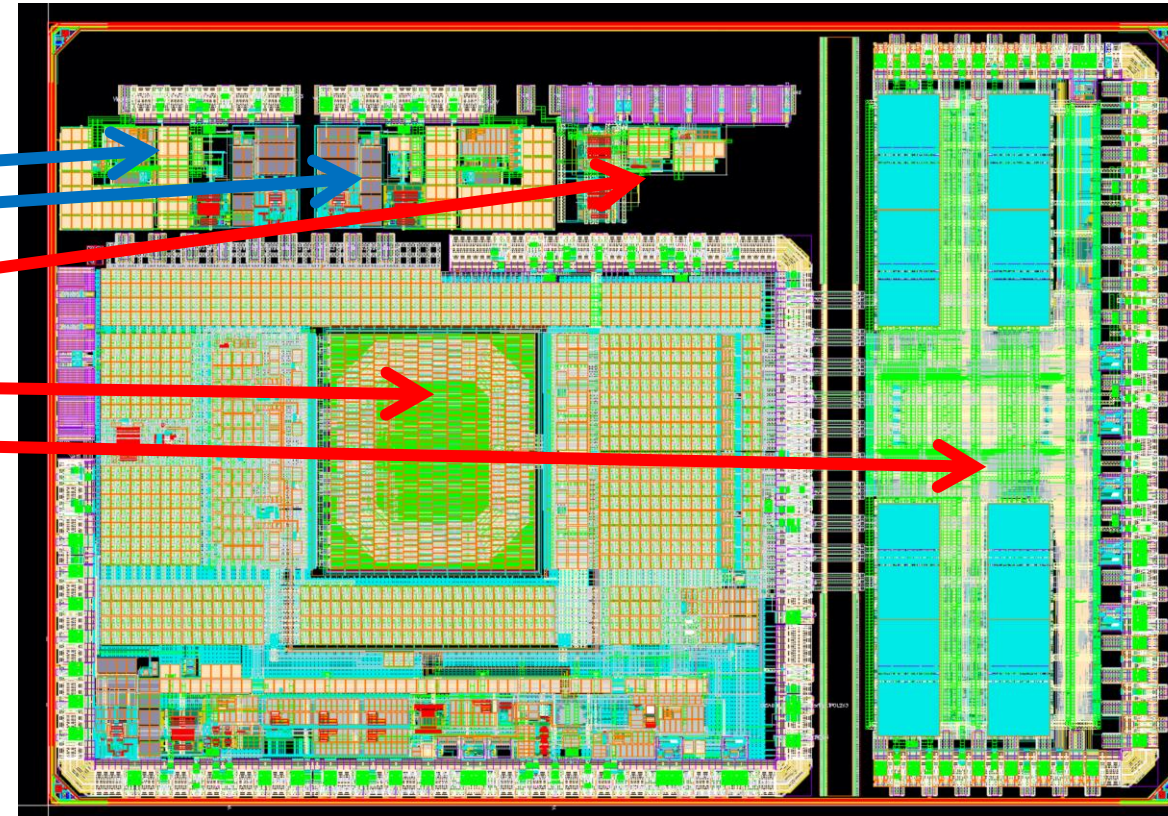
iPOL2V3 (with fix for the Nwell leakage current)

SOC from RD5.4 (microcontroller)

First use of iPOL2V3 for supplying a 28nm chip

UniUD

CERN



2) We are aiming a submission in I4T of a controller + power stage for replacing in long term bPOL12V and bPOL48V

Conclusions



Legacy converters bPOLs:

- New modules of bPOL48V available
- Gan_Controller for bPOL48V will be industrially tested, ASICs available on Feb 25

New RD on going

- 2 stage based
- 48 to 2.3V/5V under development in a new HV technology exploring new architecture as well
- 3 POL have been developed in 28nm technology: iPOL5V, iPOL2V3 and linPOL1V2. All three working fine, tested up to levels above 1Grad. We found a TID issue on iPOL5V, it has been corrected and re-submitted.
- Linear regulators for start-up have been developed and integrated in silicon, testing will happen in 2025