ATLASPIX3.1 Serial Power Modules

DRD 7.1.b Project Meeting
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Activity in close collaboration with KIT,
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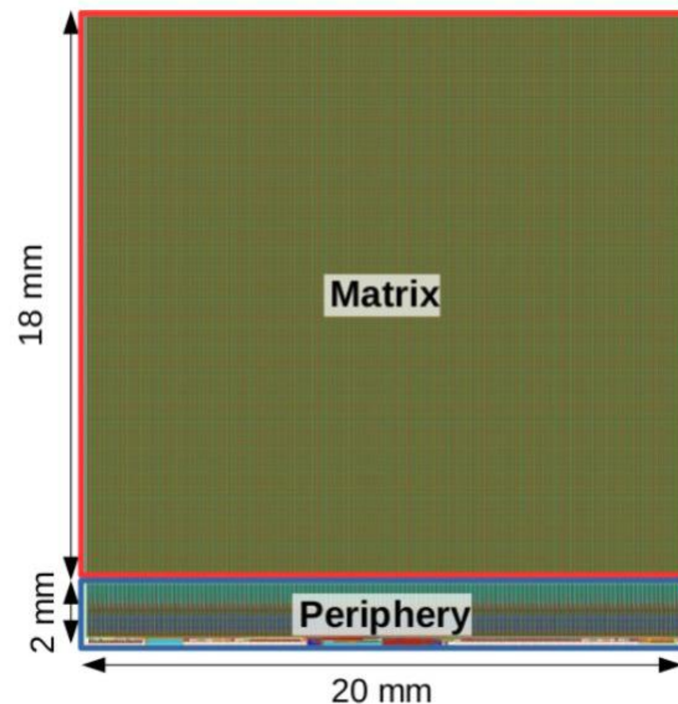
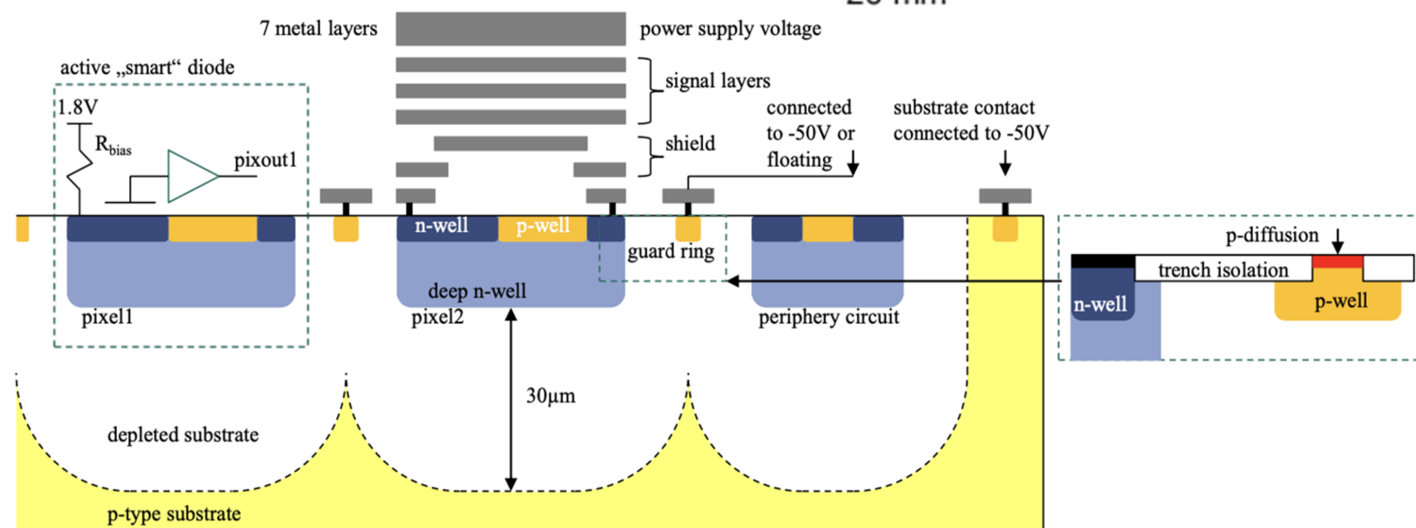
Introduction

- The Milano group is involved in the design of the silicon tracker for experiments at FCCee
  - multiple scattering is an issue for the high precision tracking of FCCee experiment
  - minimizing service material: low detector power consumption (monolithic pixel detectors) and serial power distribution
- Goals in DRD 7.1b
  - build a serial power chain of HV-CMOS monolithic pixel modules
  - realistic end-user test bench for the components developed within the project
  - possibility to build also a second chain with low performance ITk pixel hybrid modules
- Presented today
  - studies of ATLASPIX3 performances in serial power mode
  - steps towards a multi chip module assembly and serial-power chain

ATLASPIX3

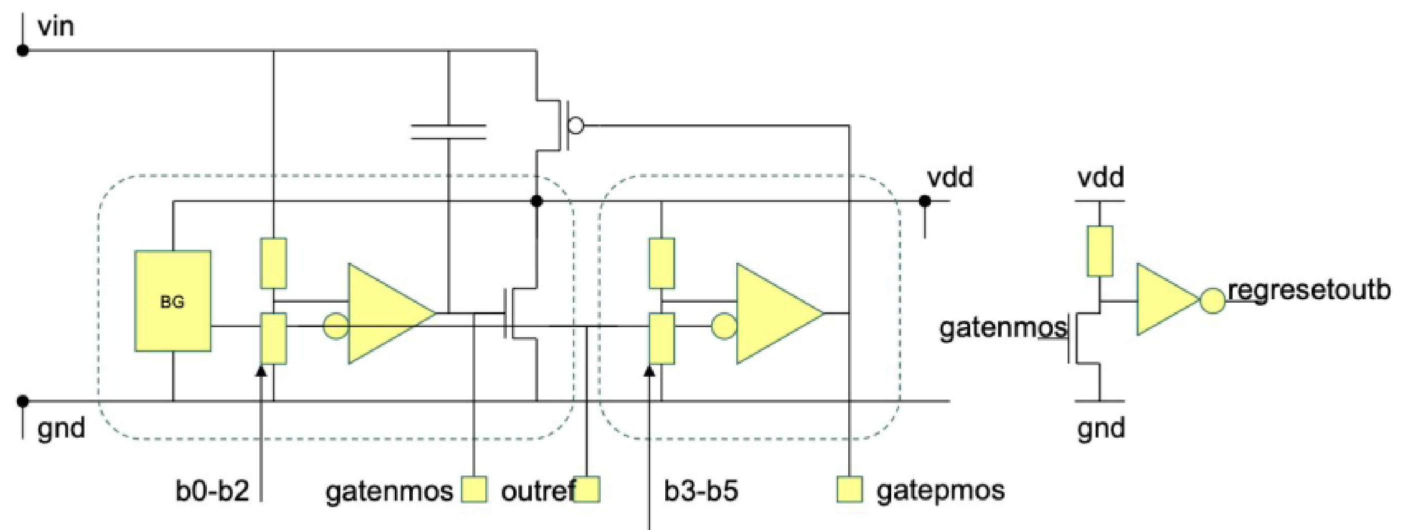
- **ATLASPIX3 general features**
  - **TSI 180 nm HVCMOS** technology
  - full-reticle size **20×21 mm²** monolithic pixel sensor
  - 200 Ωcm substrate (other substrates up to 2 kΩcm also possible)
  - **132 columns of 372 pixels**
  - **pixel size 50×150 μm²** (25×150 μm² on recent prototypes)
  - **breakdown voltage ∽-60 V**
  - up to **1.28 Gbps downlink**
  - **25 ns timestamping**
  - analog pixel matrix, digital processing in periphery
- Both **triggerless** and **triggered** readout modes:
  - two End of Column buffers
  - 372 hit buffers for triggerless readout
  - 80 trigger buffers for triggered readout

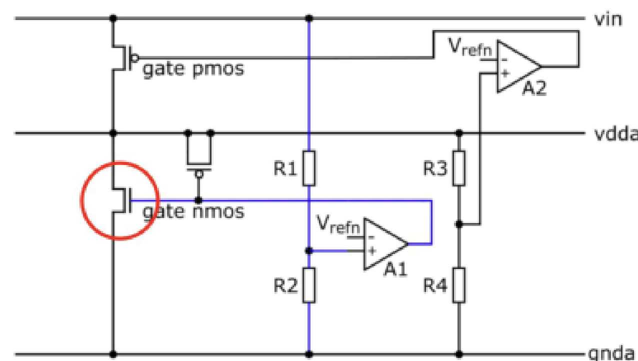


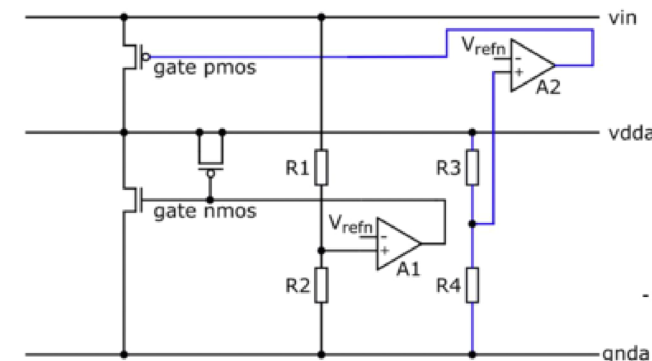


ATLASPIX3 Serial Powering

- Version **ATLASPix3.1** has possibility for **serial powering** through **two shunt/low dropout regulators**
  - **digital** and **analog** (VDDD/A)
  - **3 bits** to tune threshold of shunt regulator
  - **3 bits** to tune VDD
  - gatenmos, outref, gatepmos are for monitoring
  - regresetoutb can be used as power on reset
- Possibility to use a **single power supply for all the 6 alimentation needed to operate the chips**



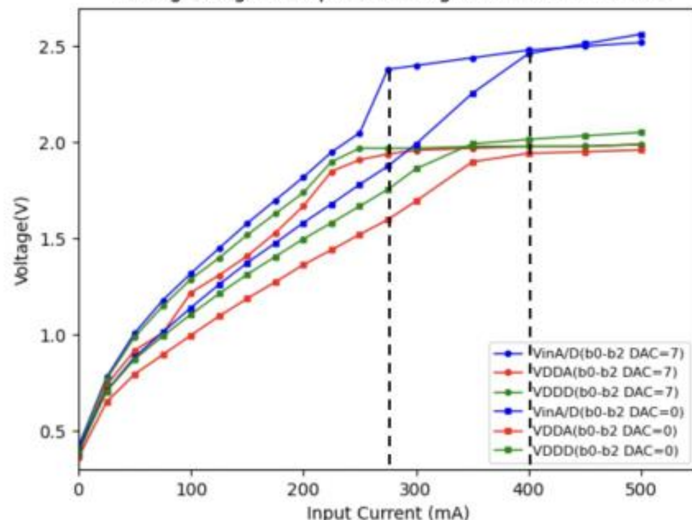


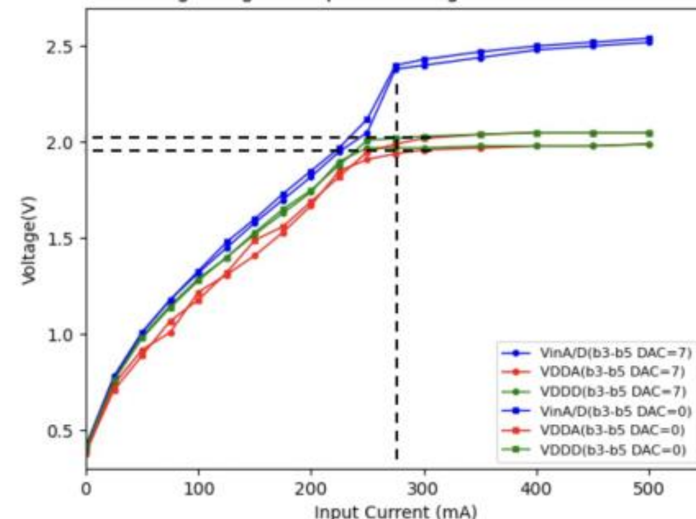


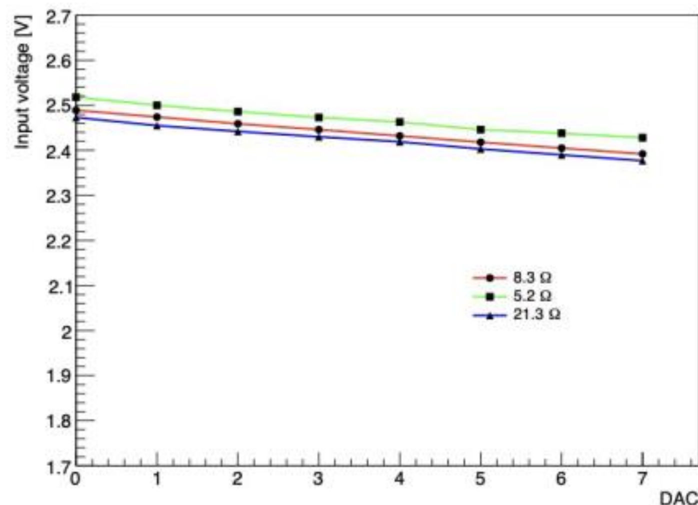
- First loop defines **shunt regulators**
- Second loop **regulates VDDD/As**

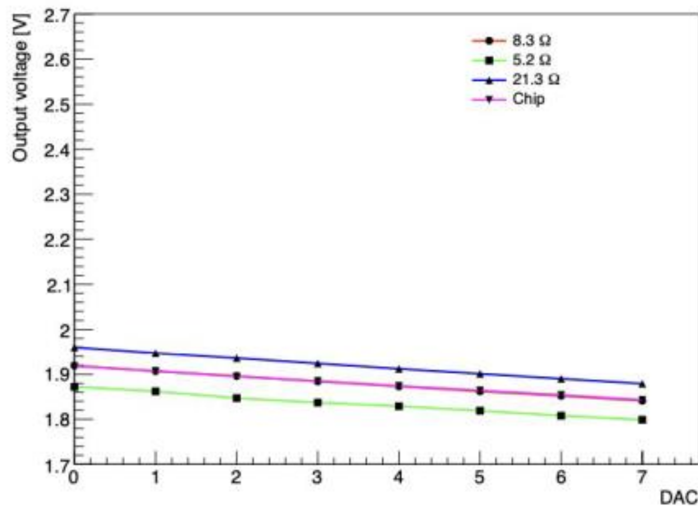
Serial Powering – Single chip

- **Turn-on curves** studies
  - **Vin** and **VDDD/A** for the two **extreme DAC values**
  - turn-on point from 275mA for DAC=7 to 400mA for DAC=0
  - VDDD/A from 2.1V for DAC=0 to 1.9 for DAC=7





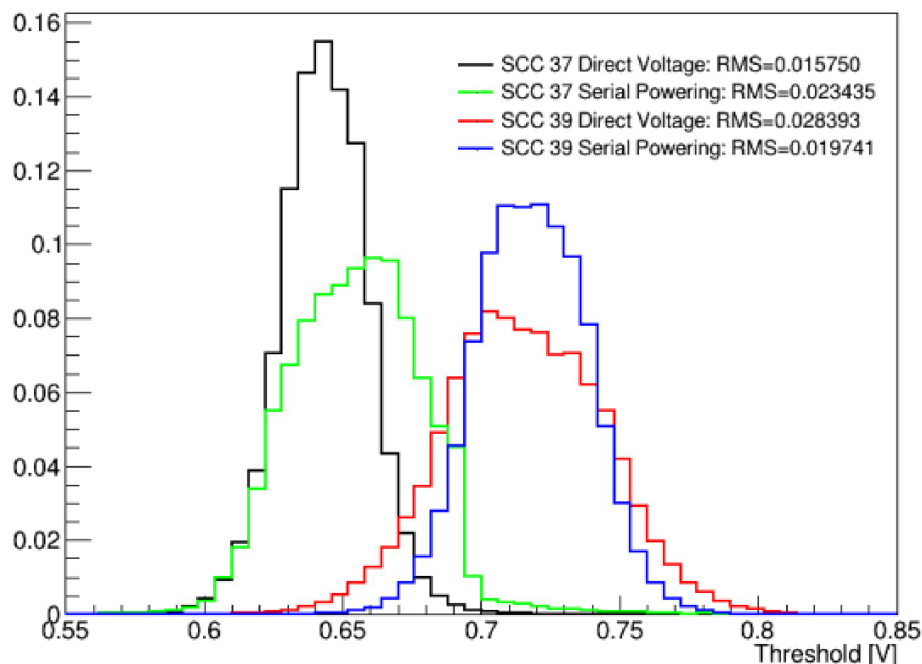


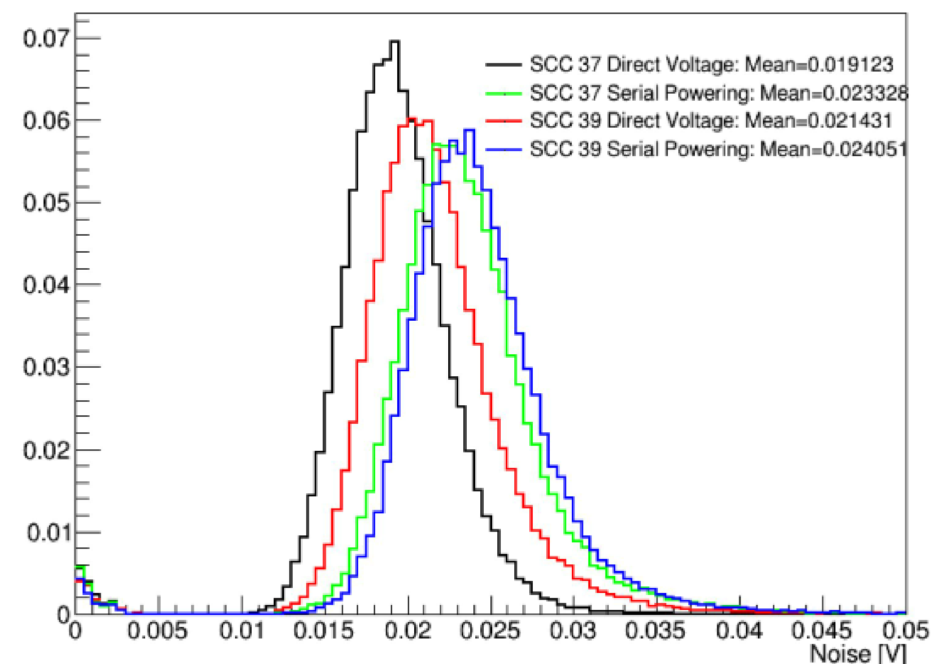


- **Tuning range** studies
  - **DAC scan** at a fixed input current for Vin and VDD/A and different loads
  - **linearity** of regulation but very **low range** (different from module on the right)

Serial Powering – Single chip

- **Tuning performance** and **noise** comparison for two SCCs in DV (Direct Voltage) and SP (Serial powering) powering mode
- **No degradation of performances**



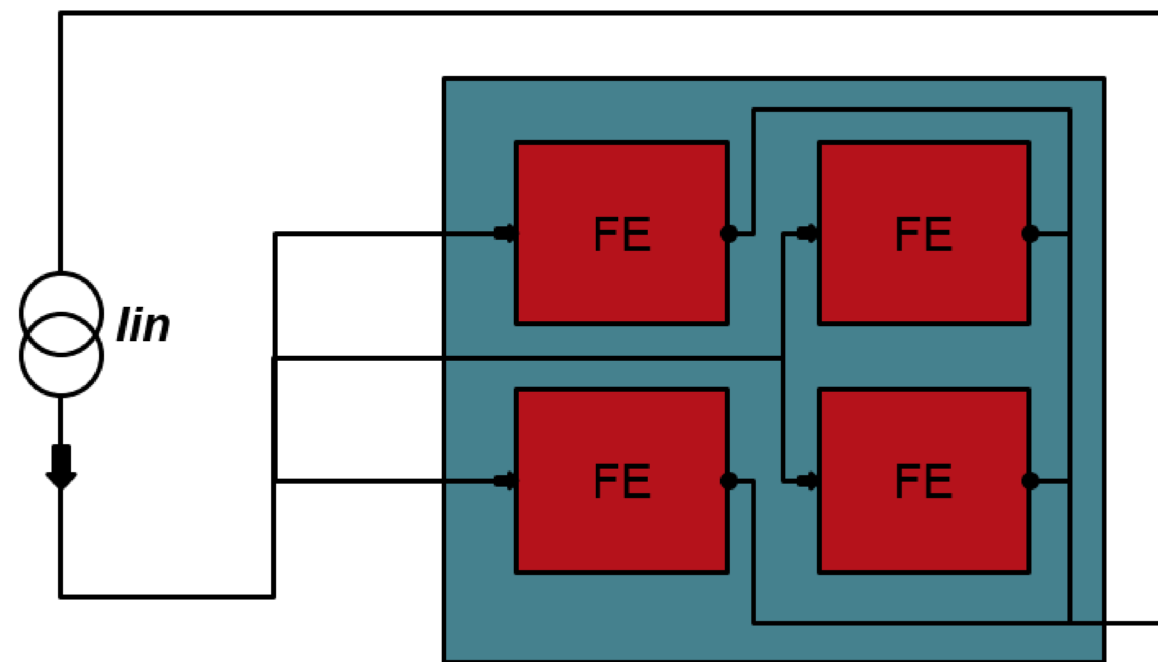


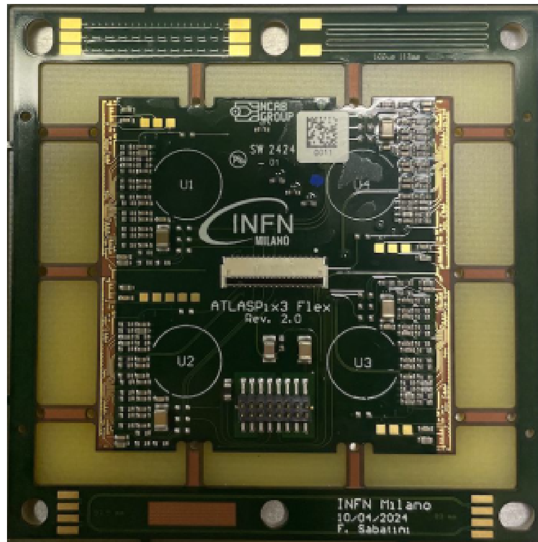
	DV (tuning)		SP (tuning)	
	Threshold [V]	Noise [V]	Threshold [V]	Noise [V]
SCC37	0.644±0.016	0.019±0.003	0.654±0.023	0.023±0.003
SCC39	0.715±0.028	0.021±0.003	0.718±0.020	0.024±0.003

Serial Powering – Quad modules

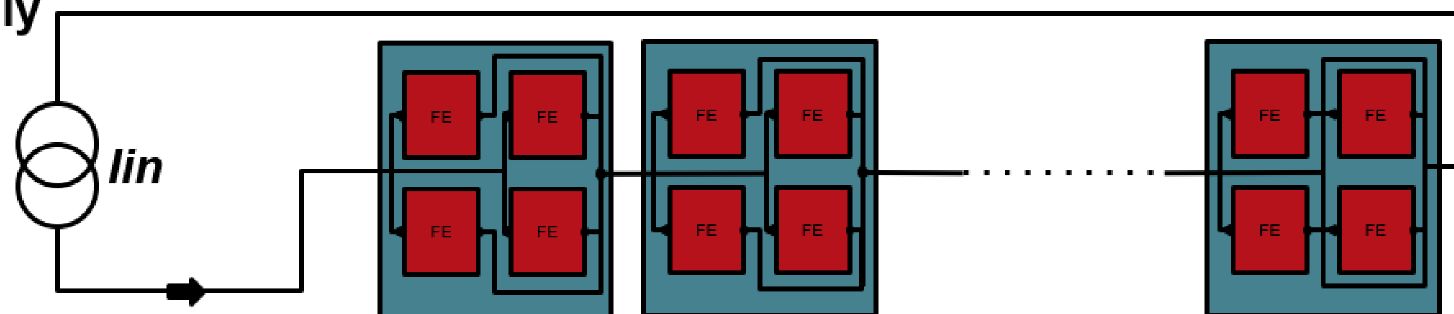
- Developed a **new flex PCB** which implements **serial powering** for **quad modules**
  - 4 FE **regulators** are connected in **parallel**
  - powered with a **constant current**
  - big differences in the behaviour of the 4 FE regulators can be problematic
- **20 flexes** have been **produced**

Tests presented in the next slides



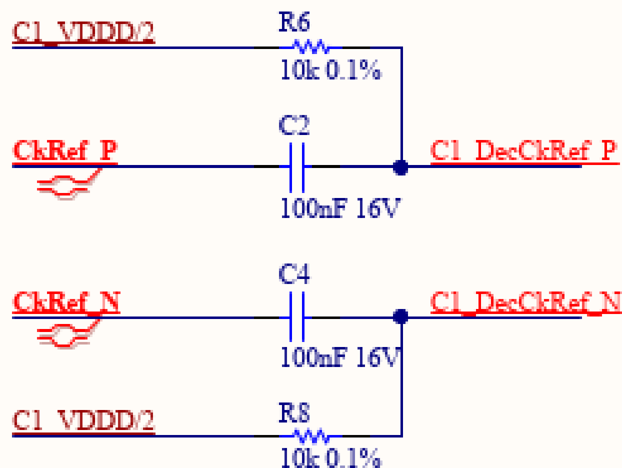


- Future step will be to build **chain of quad modules serially connected**



Quad modules with direct powering have been already produced in 2022 and tested on beam in 2022 and 2024

Input lines



Long lines distributing inputs to all 4 FE chips
AC coupling at chip inputs
DC level set by pull up resistors to VDDD/2

Chip U1

Chip U4

Chip U2

Chip U3

100 Ohm line terminations

SynRst

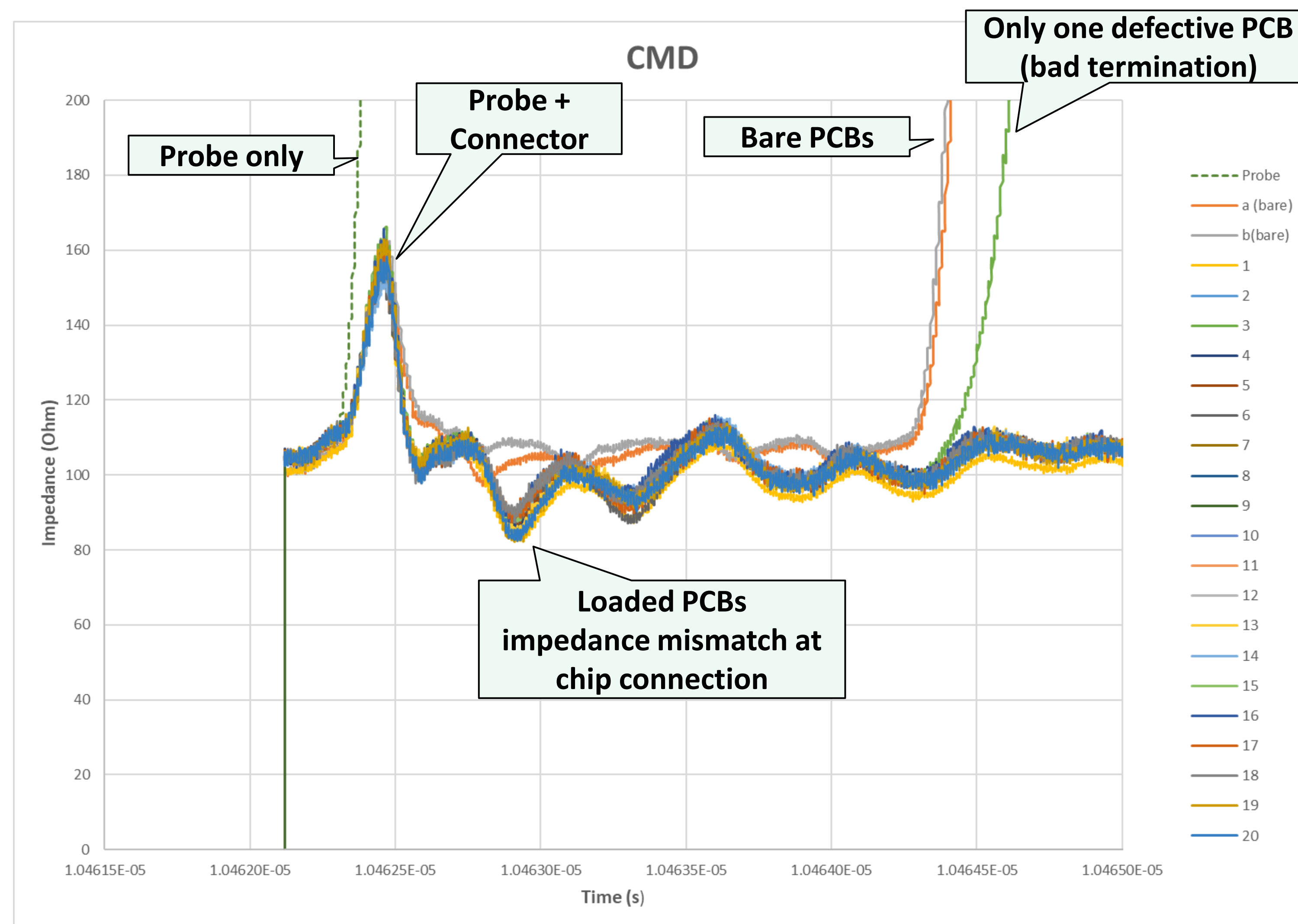
ExtTrigger

Cmd

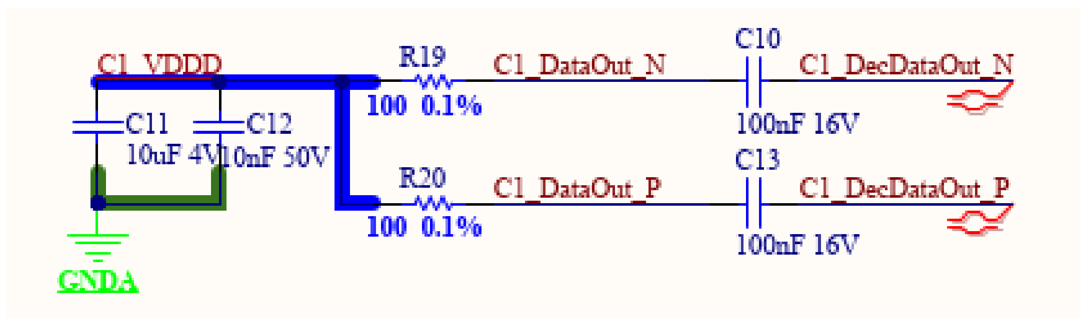
CkExt

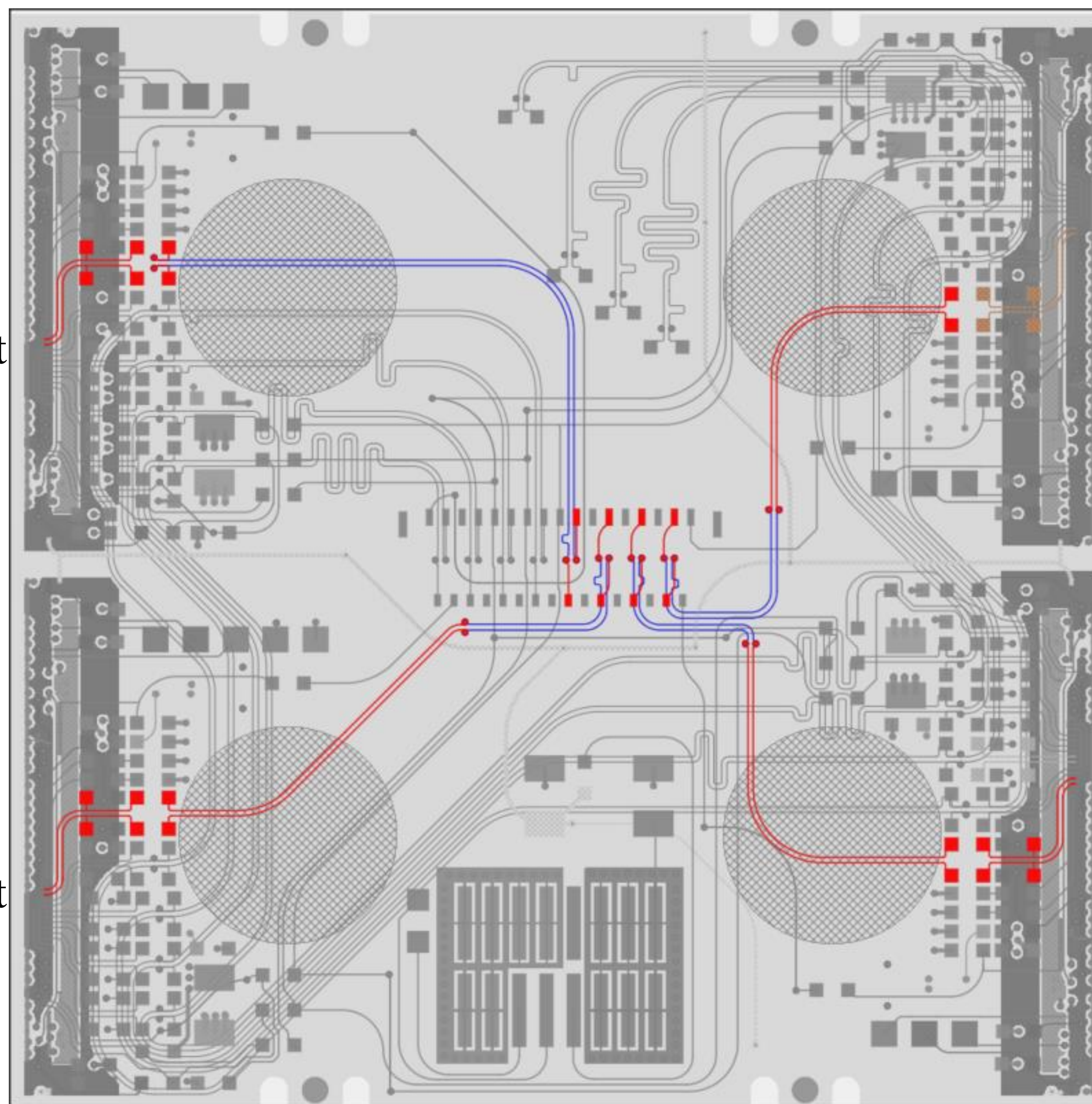
Input lines impedance verification

- Tektronix DSA8200 oscilloscope equipped with the 80E04 TDR (Time Domain Reflectometer) was used for impedance measurements.
- Lecroy SDA 808Zi-A 8 GHz Oscilloscope with D830 differential probe was used for eye measurements
- HP 81130-A 660 MHz pulse generator



Output lines





Short lines
AC coupling at chip outputs
Pull up resistors to VDDD:
ATLASPIX3 serializers can only drain current

Output lines impedance verification

- Tektronix DSA8200 oscilloscope equipped with the 80E04 TDR (Time Domain Reflectometer) was used for impedance measurements.
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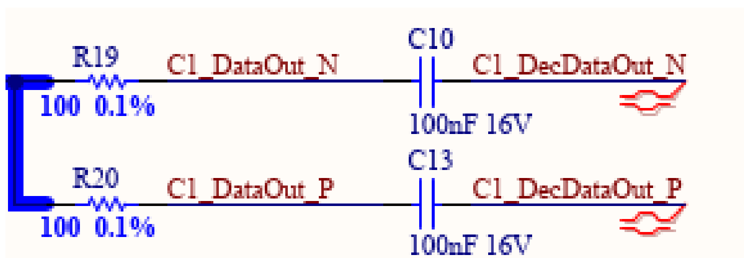
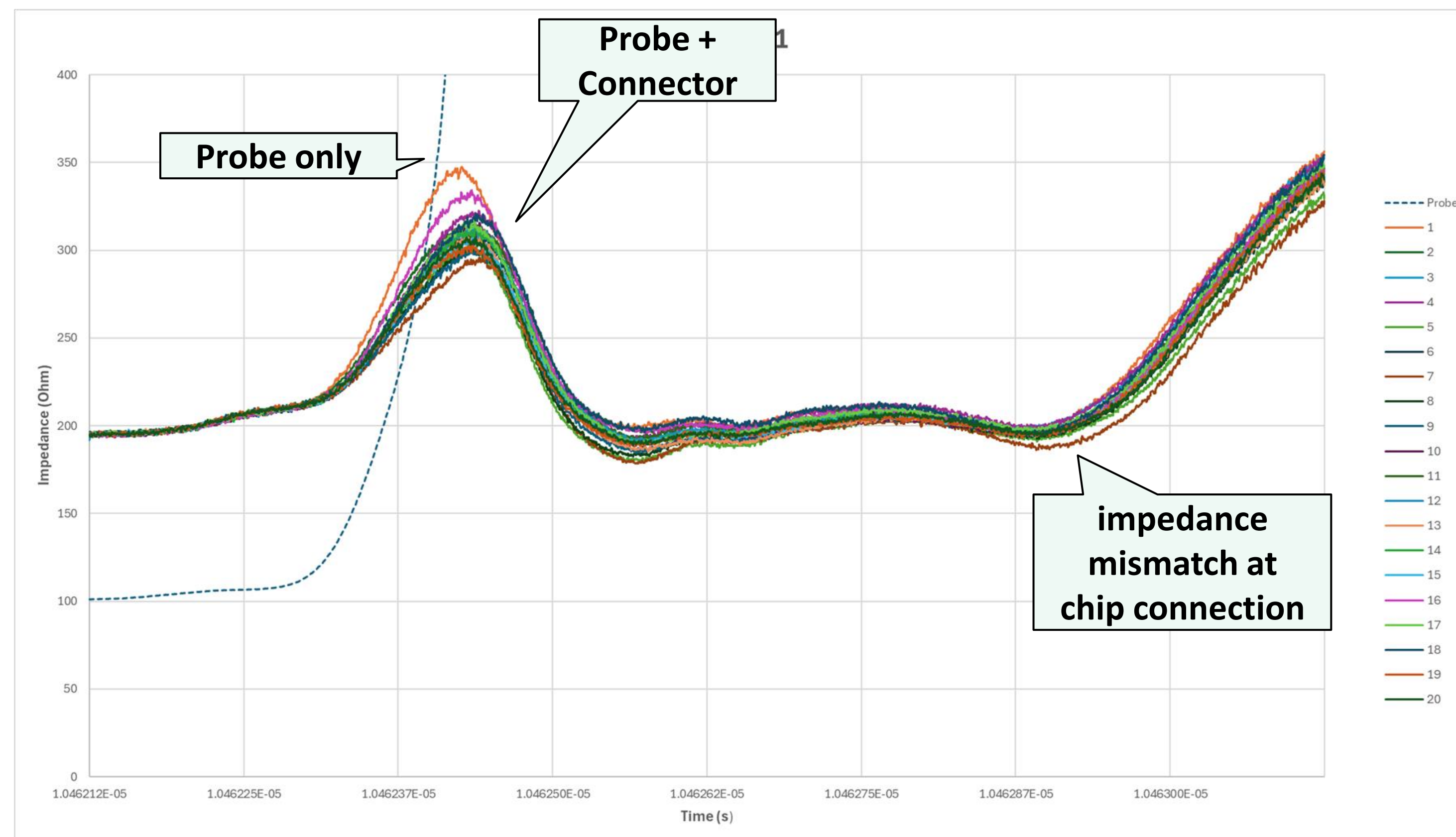
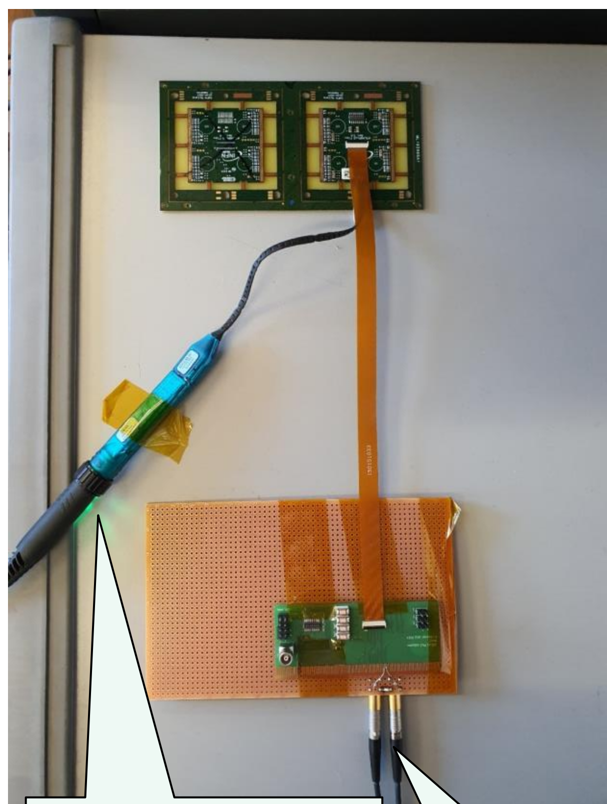
- **Measured value is 200 Ohms**
  - offset is an artefact of the decoupling circuit
  - same behaviour observed with a replica of the circuit with discrete components





Check on signal quality



Differential probe

640 MHz Pseudorandom bit generator

Cursors	X1	X2	DeltaX	Y1@X1	Y2@X2	DeltaY	Y3	Y4
value	0 ps	1.000 ns	1.000 ns				125.2 mV	-101.8 mV

350mV

1ns

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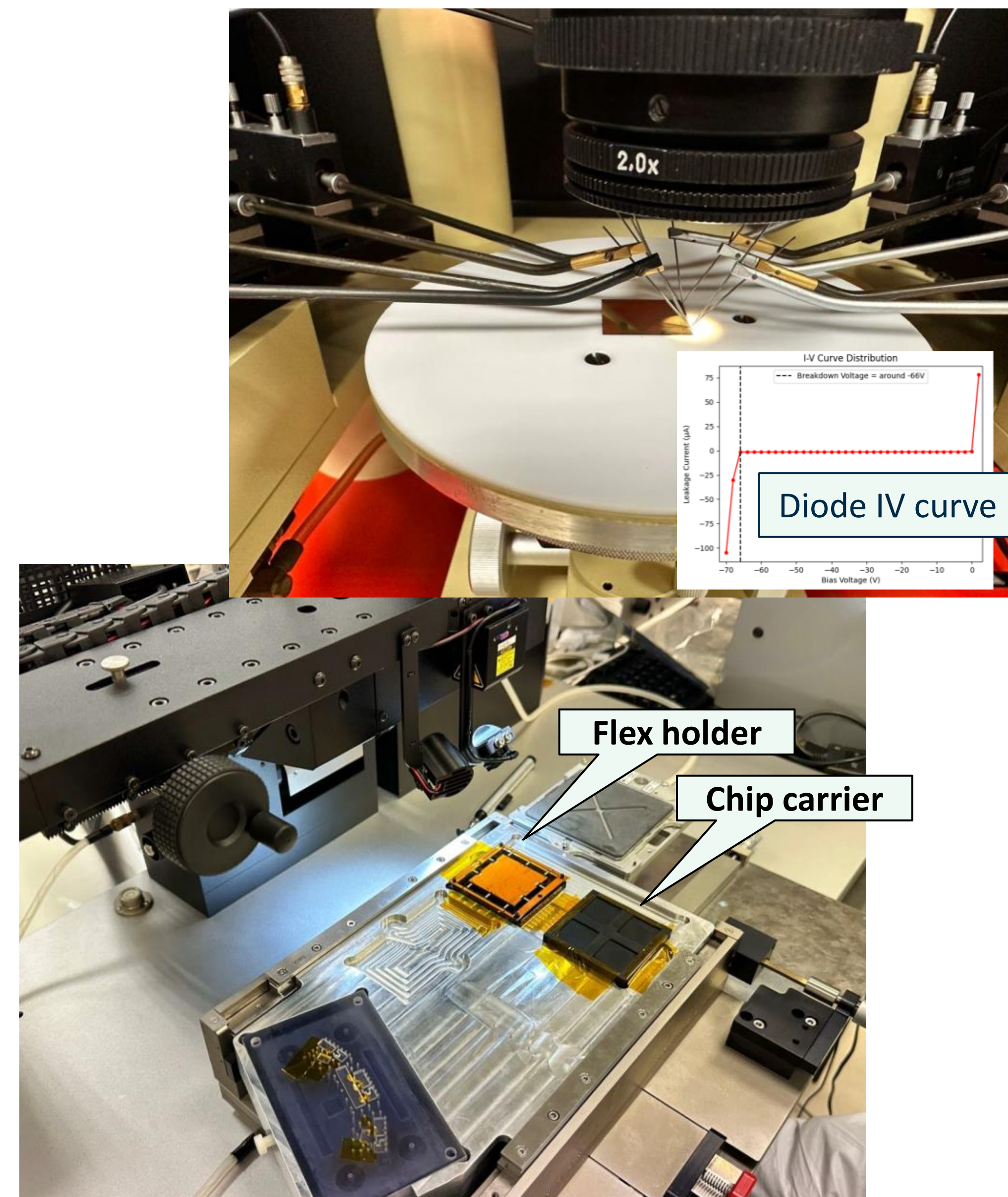
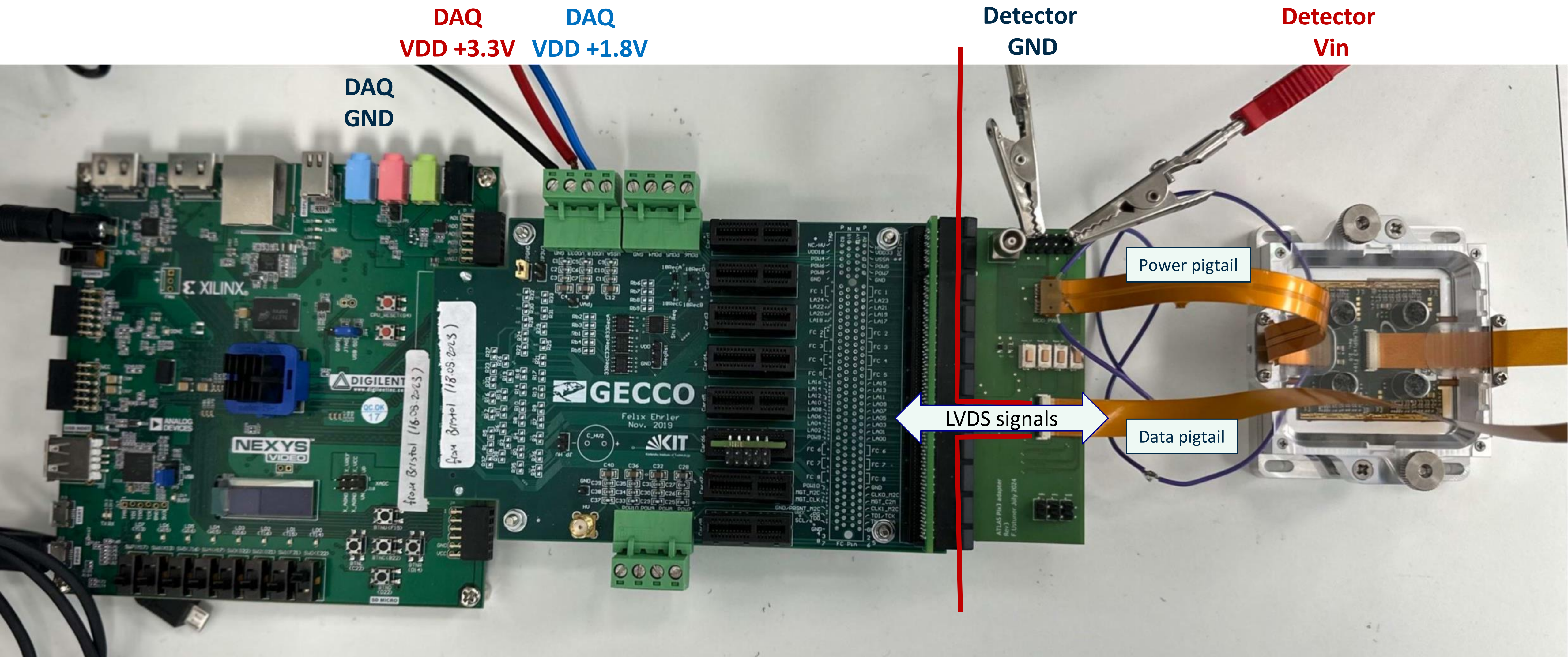
Module assembly

- I-V test for HV functionality under probe station before assembly
  - failure mode observed during the production of quad modules with direct powering
  - a short on one chip may jeopardize the operation of the other chips in the module
- Finetech pico die bonder
  - used also for the assembly of ATLAS ITk 3D modules
  - manual optical alignment between chips and flex-hybrid
- Araldite 2011 deposited by stamps method on flex backside



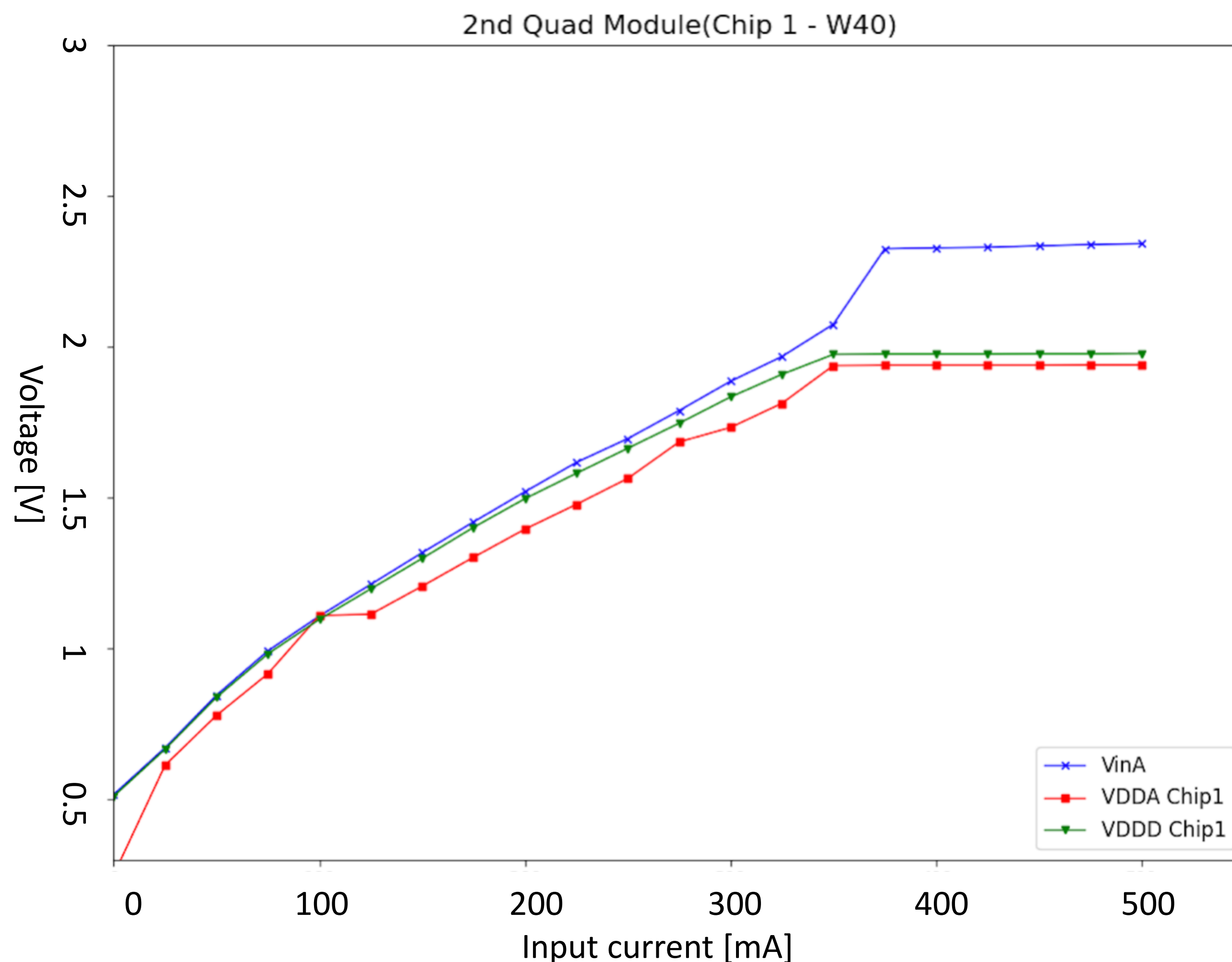
Module testing setup



- GECCO, flexible readout system developed by KIT
- Firmware and sofware adapted to module operation
- Adapter card splitting the two power domains
- LVDS signals decoupling on the flex PCB

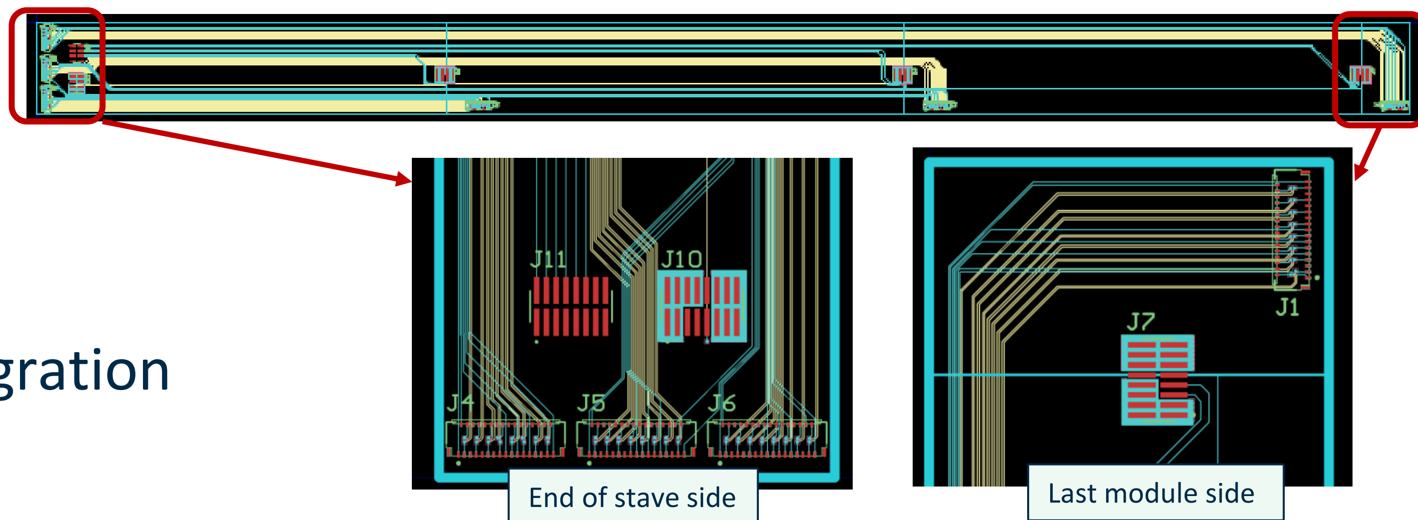
Module Bias

- Tests with a single chip bonded to the flex circuit
  - verify connectivity and settings of configuration pins
- On chip regulators:
  - turn-on at about 350 mV input current
  - VDDD/VDDA regulated at ~1.9 V
  - Consistent with observations on single chip carriers
- Module configuration
  - configuration pins were programmable from the FPGA in direct power quad-modules
  - needed to be fixed by wire-bonding to local VDDD/GND in serial power quad-modules
  - found some inconsistency in the propagation of settings between the direct-power and serial-power modules
  - debugging is ongoing, it is likely it can be fixed by modifying the wire bond diagram



Conclusions and Outlook

- The operation of the ATLASPix3.1 HV-CMOS monolithic pixel detector in serial power mode has been investigated
- Assembled the first multi-chip detector module in a configuration suitable for serial powering
  - currently debugging the FE configuration pins (set by wire bonding)
- Designed a power bus to test a multi-module serial power chain
  - Aluminium conductor to reduce thickness in radiation lengths
  - Ready to start production when module operation issues are solved
- Preparing a DRD3 common project to pursue also other aspects of detector integration



BACKUP

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Flex Stackup

- 4-layer PCB
  - 2 signal planes
  - Ground and Vin
- Line impedance checked with vendor provided manufacturing information

Basic | Dielectric | Metal | Z0 Planning | Manufacturing | Custom View

	Layer Name	Usage	Thickness um	Er	Diff Z0 ohm	Width um	Gap um	Z0 Curve
1	Solder_Mask	Solder Mask	20	4.4				
2	FCCL(L1)	Plating	25	<Auto>				
3	FCCL(L1)	Signal	18	<Auto>	100	93	100.727	
4	FCCL(L1)_PI	Substrate	100	3.5				
5	ADH(1)	Adhesive	25	3.5				
6	FCCL(L2)	Plane	18	<Auto>	1	10	<Error>	
7	FCCL(L2/L3)_PI	Substrate	100	3.5				
8	FCCL(L3)	Signal	18	<Auto>	100	82	116.491	
9	ADH(2)	Adhesive	25	3.5				
10	FCCL(L4)_PI	Substrate	100	3.5				
11	FCCL(L4)	Plane	18	<Auto>	1	10	<Error>	
12	FCCL(L4)	Plating	25	<Auto>				
13	ADH(3)	Adhesive	35	3.6				
14	PI	Cover Layer	25	3.6				

Solder_Mask
FCCL(L1)
FCCL(L1)
FCCL(L1)_PI
ADH(1)
FCCL(L2)
FCCL(L2/L3)_PI
FCCL(L3)
ADH(2)
FCCL(L4)_PI
FCCL(L4)
FCCL(L4)
ADH(3)
PI

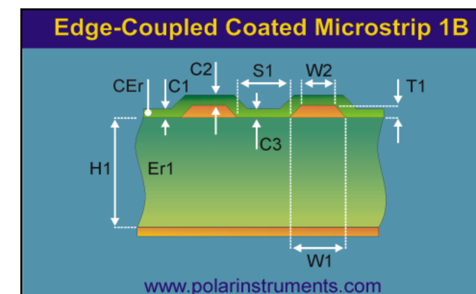
☑ Draw proportionally Total thickness: 552 um
☑ Use layer colors

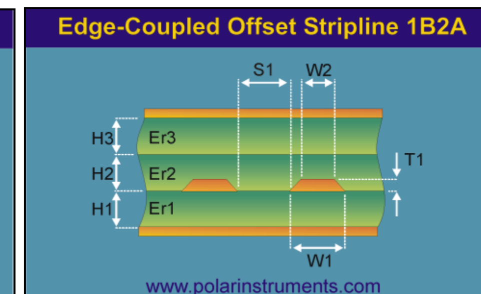
No errors found in stackup.

Plan for: Differential pair | Apply as Test Width
Strategy: Solve for separation | Hint: Move mouse over cell with <Error> for details.

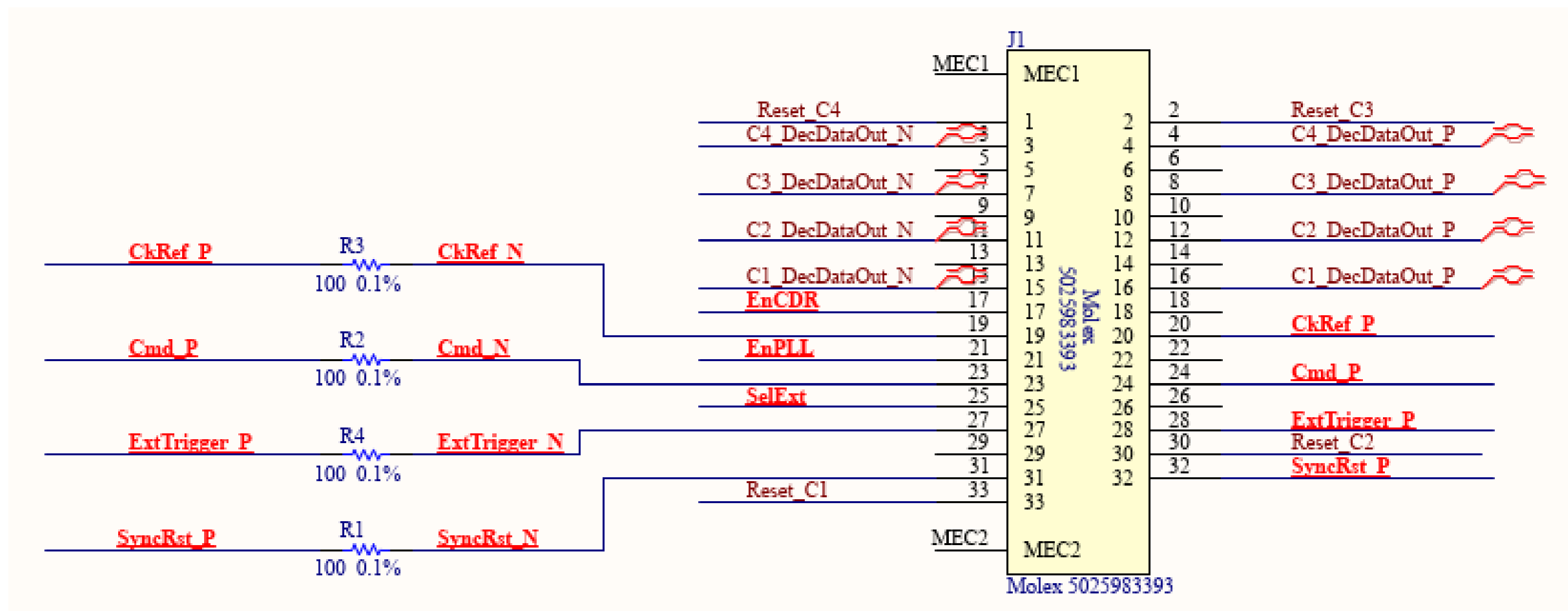
STACK-UP for 4L

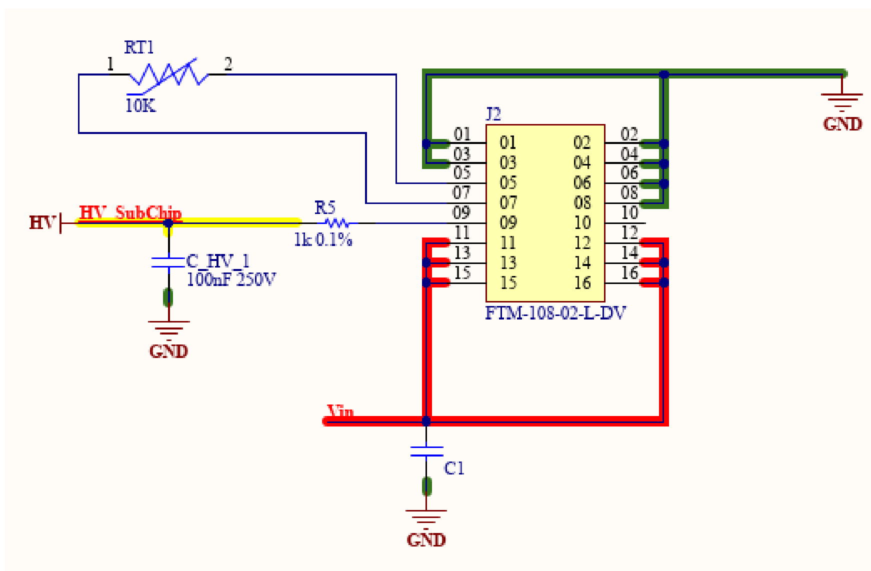
Material		Thickness(um)	Brand	DK
Solder Mask	Green ink	20	PSR-9000-FLX501	4.4
Plating	Plating Cu	25		
FCCL(L1)	Cu (RA)	18	Allstar AS2L-ADA00BU	3.5
	PI	100		
ADH	adhesive	25		3.5
FCCL(L2/L3)	Cu (RA)	18	Allstar AS2L-ADA00BU	3.5
	PI	100		
	Cu (RA)	18		
ADH	adhesive	25		3.5
FCCL(L4)	PI	100	Allstar AS2L-ADA00BU	3.5
	Cu (RA)	18		
Plating	Plating Cu	25		
Coverlay	adhesive	35	Shengyi SF305C1035N	3.6
	PI	25		





Data and Power Connectors





Input lines impedance verification

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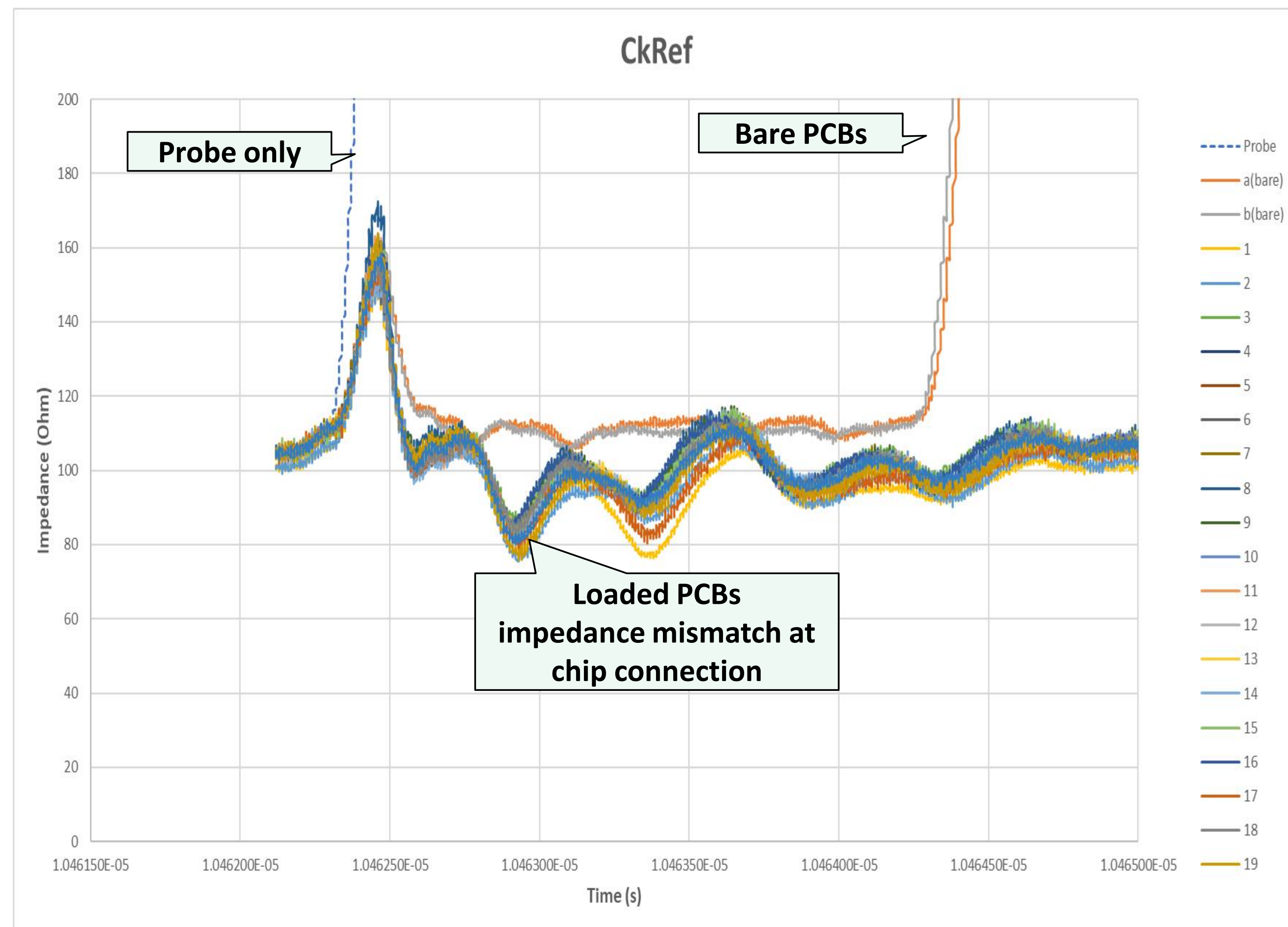

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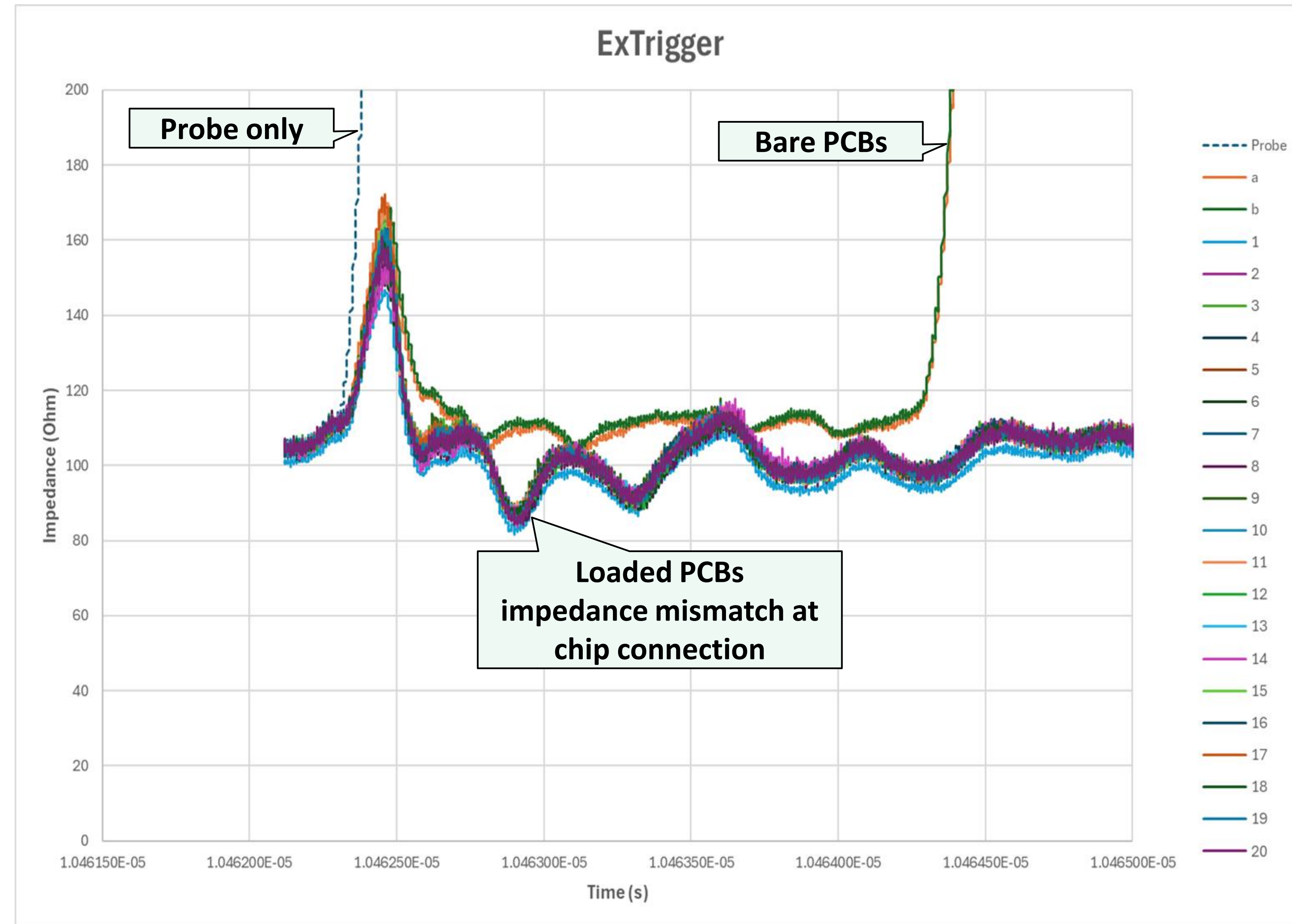

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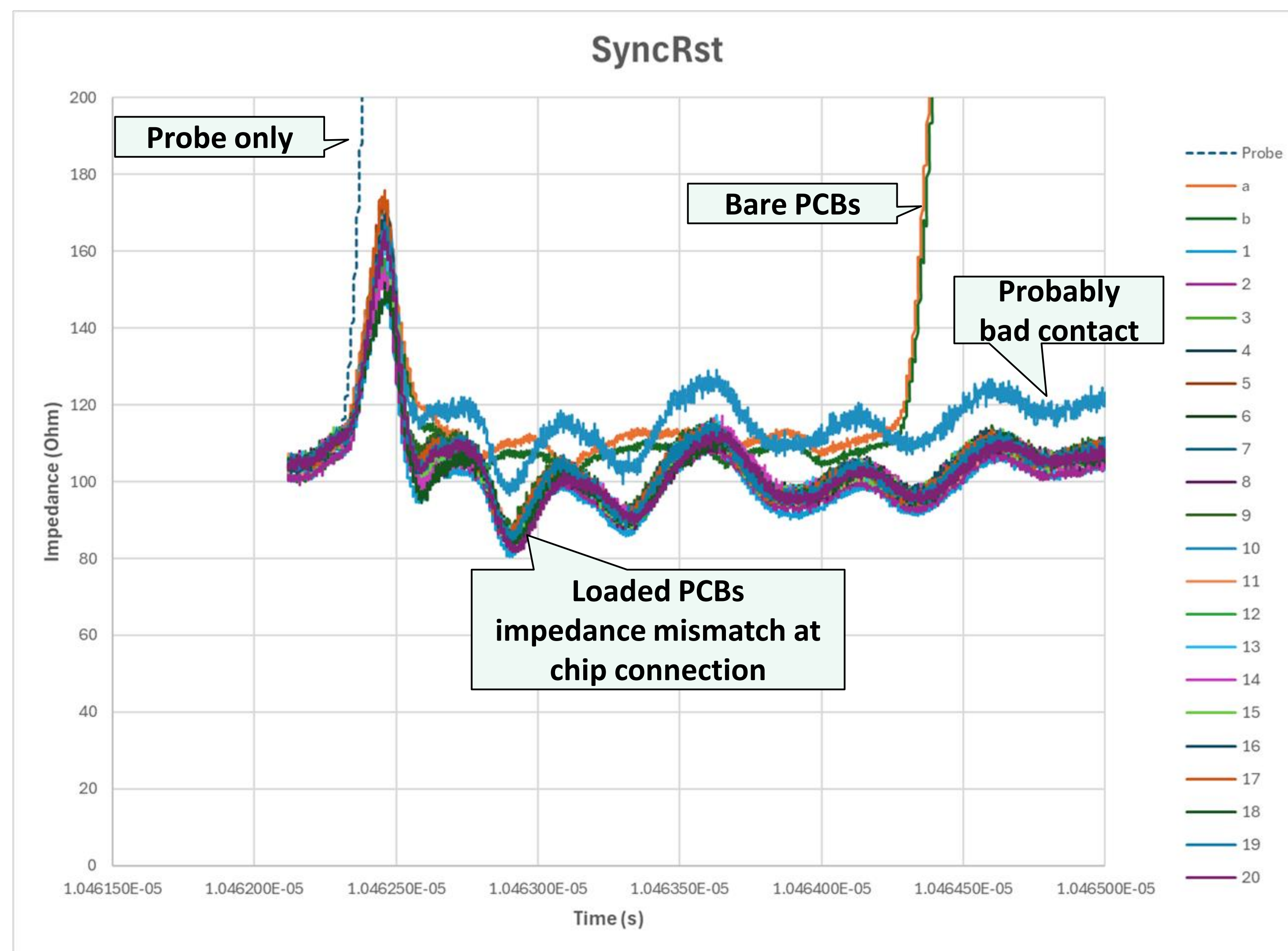

Output lines impedance verification