Fachhochschule
Dortmund
University of Applied Sciences and Arts

Project Status Report

DRD 7.2b Meeting

07-February-2025

Michael Karagounis

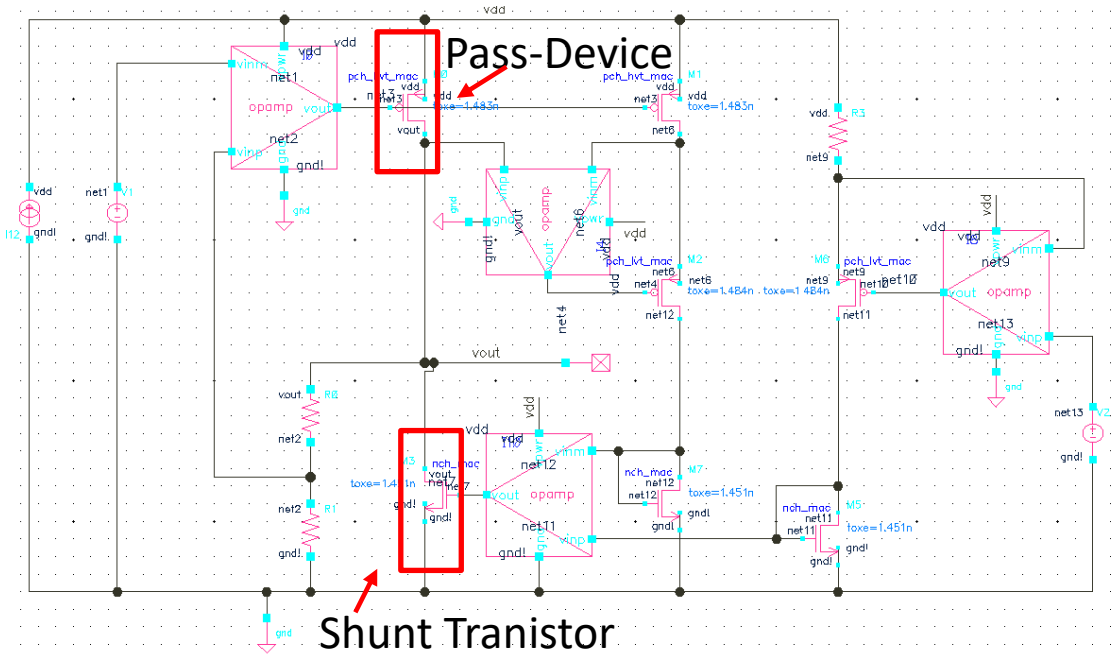
Funding Situation

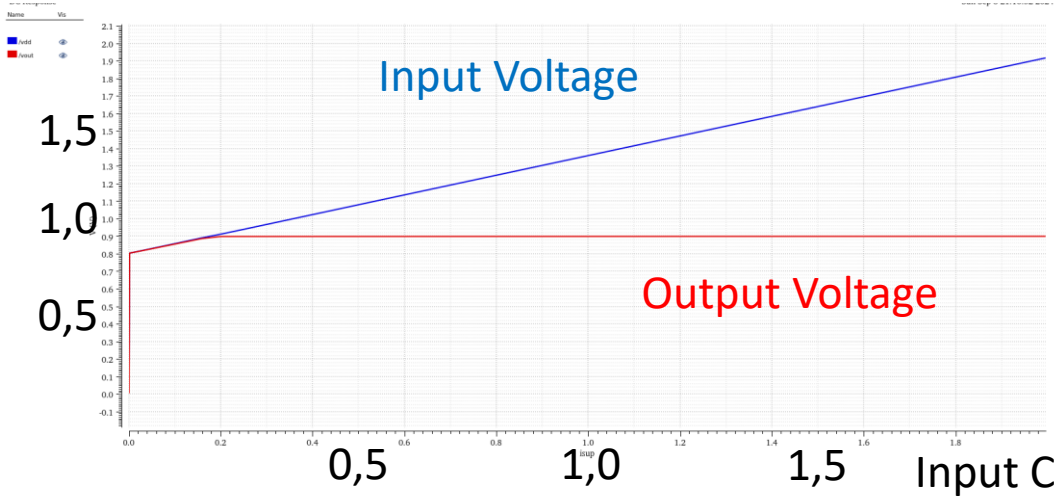
- Man Power
  - 1 PhD Student (1.7.24-30.6.27)
  - 1 PostDoc (1.12.24-30.11.27)
- Chip Submissions
  - 32k €
- Devices
  - 30k €

Project Status

- No Man Power available for real design work at the moment
  - Future PostDoc Jermias Kampkötter was writing his PhD thesis
  - Failed to hire domestic PhD student
  - "Foreign" PhD student Hossein Tavakoli currently stuck in VISA process
- Situation is improving now
  - PhD thesis submitted in December
  - PhD student should be in lab in spring

Shunt-LDO Design in 28nm





- First simulation studies performed in 28nm based on Verilog-A amplifier models
- Devices types and dimensions studied for shunt and pass-device
- Studies show SLDO thin-gate oxide core transistor implementation feasible in 28nm
- Technology limits maximum input voltage to 1.8V with overvoltage tolerant design (2V @ 65nm)
- Full transistor level implementation ongoing