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Investigating the performance of CMSSW on the AMD Bulldozer micro-architecture

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The density of rack-mount computers is continually increasing, allowing for higher performance processing in smaller and smaller spaces. With the introduction of its new Bulldozer micro-architecture, AMD have made it feasible to run up to 128 cores within a 2U rack-mount space. CPUs based on Bulldozer contain a series of modules, each module containing two processing cores which share some resources, while also having dedicated versions of other resources. As the LHC luminosity increases, in turn increasing pile-up, more and more computing power will be needed to reconstruct and analyse each event. In-order to provide this increase in computing power without a large increase in space, higher density computing must be used.

In this paper we explore the possibilities of running the CMS software stack, CMSSW, on one implementation of this new architecture. Initially we look at running traditional single core jobs within the architecture in such a way that it is directly comparable to jobs run on older architectures. We then go on to explore the possibility of multi-core and whole-node processing within CMSSW, which would allow for much better memory utilisation. Using less memory in any large job has the advantage of allowing the CPU to churn less data through the memory caches while analysing data, resulting in better overall performance.

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