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Track finding and fitting on GPUs, first steps toward a software trigger

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The high data rates expected from the planned detectors at FAIR (CBM, PANDA) call for dedicated attention with respect to the computing power needed in online (e.g. High level event selection) and offline analysis. The graphics processor units (GPUs) have evolved into high performance co-processors that can be easily programmed with common high-level language such as C, Fortran and C++. Todays GPUs greatly outpace CPUs in arithmetic performance and memory bandwidth, making them the ideal co-processor to accelerate a variety of data parallel applications. For the online processing (i.e: Software triggers and online event selections) GPUs are an attractive solution, online applications include high level processing which require floating point operations. However, the widely used FPGA (Field Programmable Gate Array) does not have such capabilities. The users have to program in the low-level hardware description language (HDL). GPUs, on the contrary, are programmable with high-level languages and meanwhile provide support even for double precision. An algorithm based upon conformal mapping and Hough transform was implemented on GPUs. The algorithm is tested with the PANDA central tracker simulated data. The results of the same algorithm are compared with CPU and FPGA implementations.

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