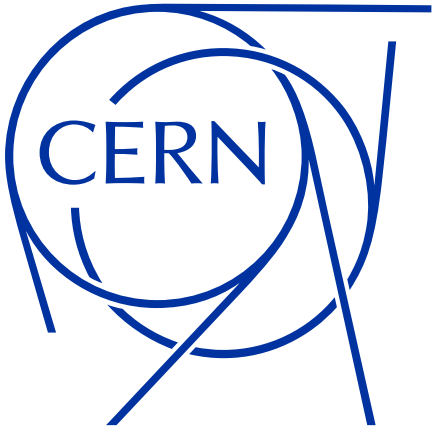


A switchboard for valuable signals, the UQDS and PDSU patch panels ...

TE-MPE-EP

Vito Vizziello

21/01/2025

What is the UQDS and PDSU patch panel

For the upgrade of the LHC to HL-LHC, the **patch panel** represents an element of the **Q**uench **D**etection **S**ystem that accomplishes the complex aim of mapping multiple signal sources to multiple destinations.

Importance of Patch Panel during Hi-Lumi

ELQA measurements can be done, at any moment, directly from the Patch Panel if radiation level around IFS boxes placed on the magnet cold mass are high.

ELQA measurements can be provided without the need to disconnect the quench detection system.

Patch Panel

Conveying all the needed signals from several IFS boxes directly to each specific UQDS.

Possibility to use a standard hardware configuration for UQDS with fewer risks to make mistakes with the cabling.

Optimizing the time and make it easy during the local interventions.

General architecture of the Patch Panel

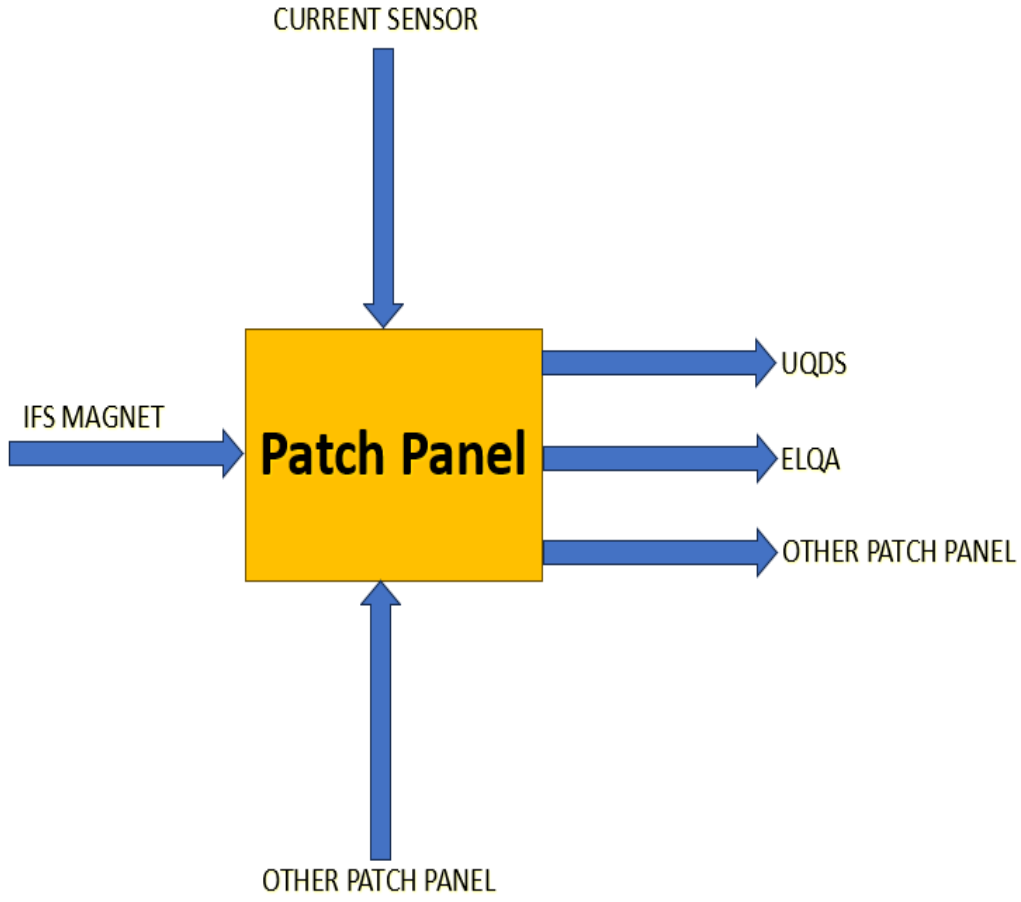
The Patch Panel collects INPUT signals from:

- IFS boxes of the magnets
- The current sensor boxes
- Another patch panel from a different rack.

Internally the patch panel is routed for driving each single INPUT signal to a specific OUTPUT.

The Patch Panel dispatches OUTPUT signals to:

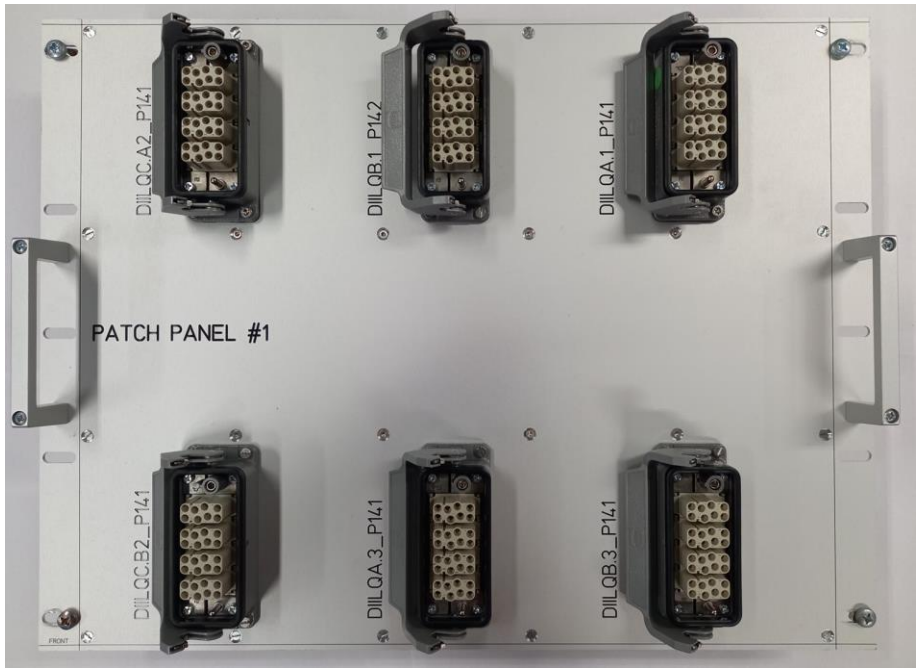
- UQDS → according to the configuration needed for each protection unit.
- ELQA → reproducing on a dedicated area the same pin-out/connector configuration as for the IFS boxes for each magnet.
- Another patch panel from a different rack.



View of the Patch Panel

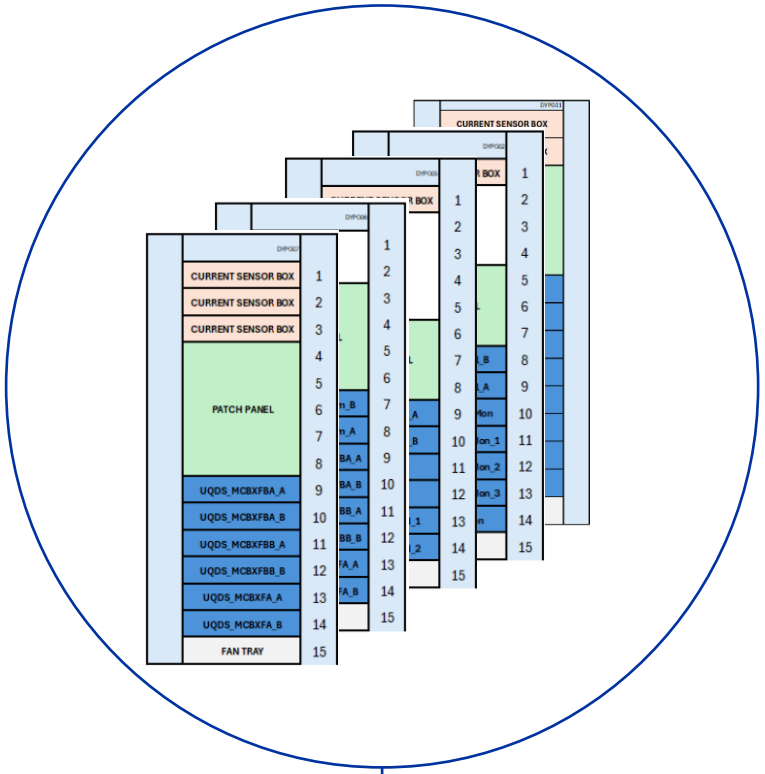
All the Patch Panels are different between each other; every rack has its own patch panel.

Front side: ELQA measurements

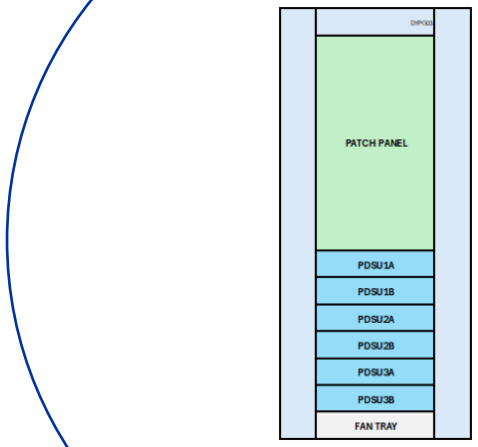


Back side: Input / Output
current sensors / other racks

IT-STRING Patch Panel



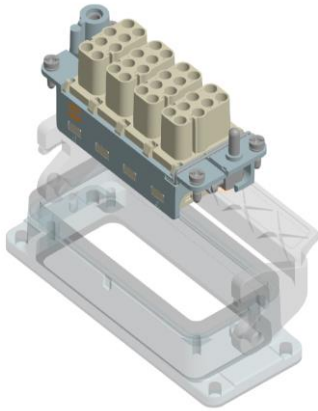
Universal **Q**uench **D**etection **S**ystem

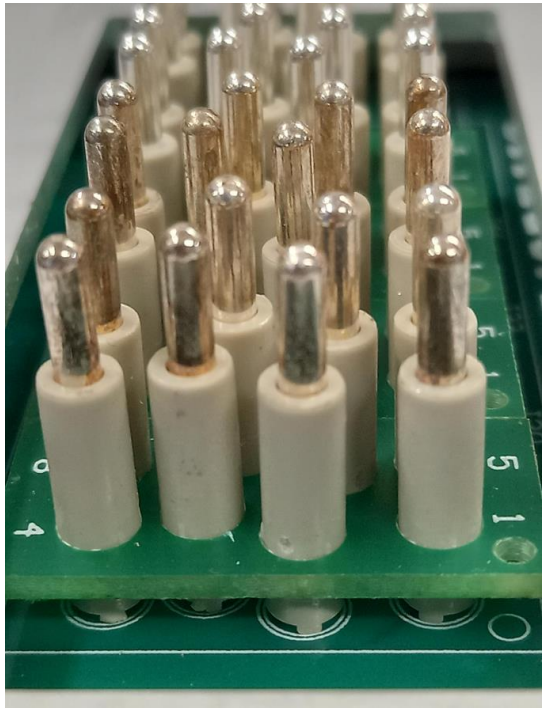


Protection **D**evice **S**upervision **U**nit

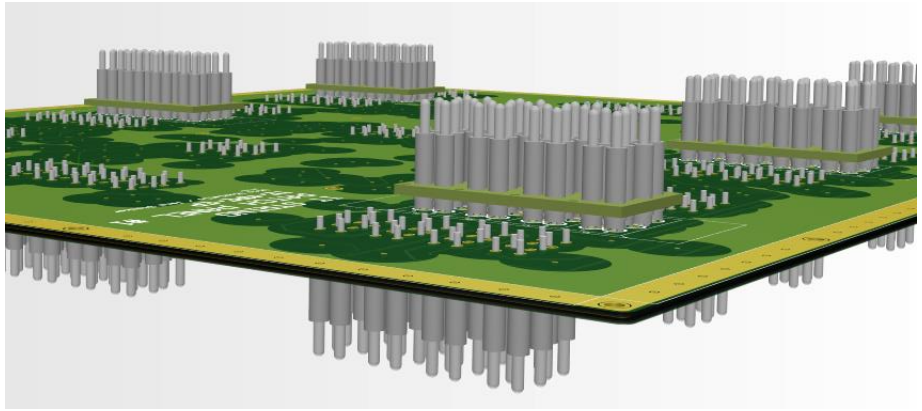
A switchboard for valuable signals, the UQDS and PDSU patch panels ...

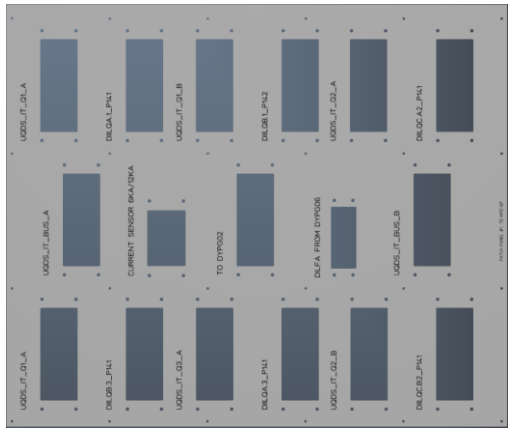
Development of the Patch Panel

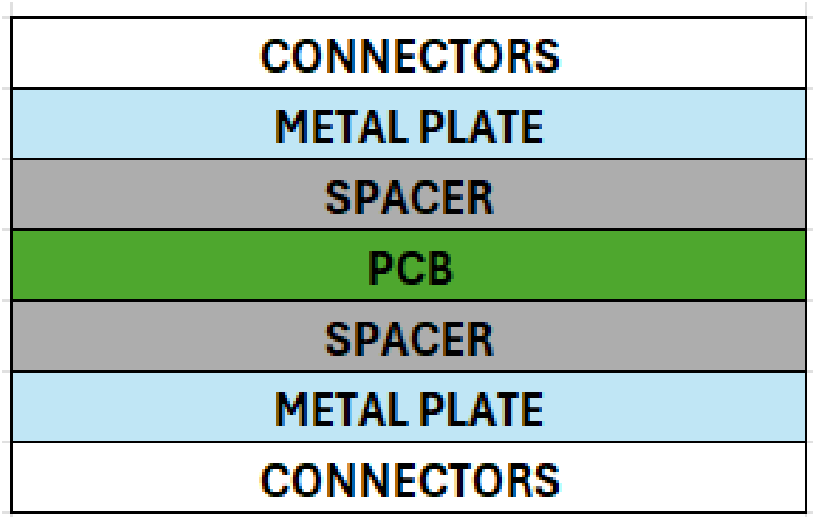




- All PCB based (no wires).
- PCB is housed in a sandwich: Metal plate, spacer, PCB, spacer, Metal plate.
- Connector housings are mounted on the metal plate, both sides, and are connected directly to the PCB via the pin-matrix.

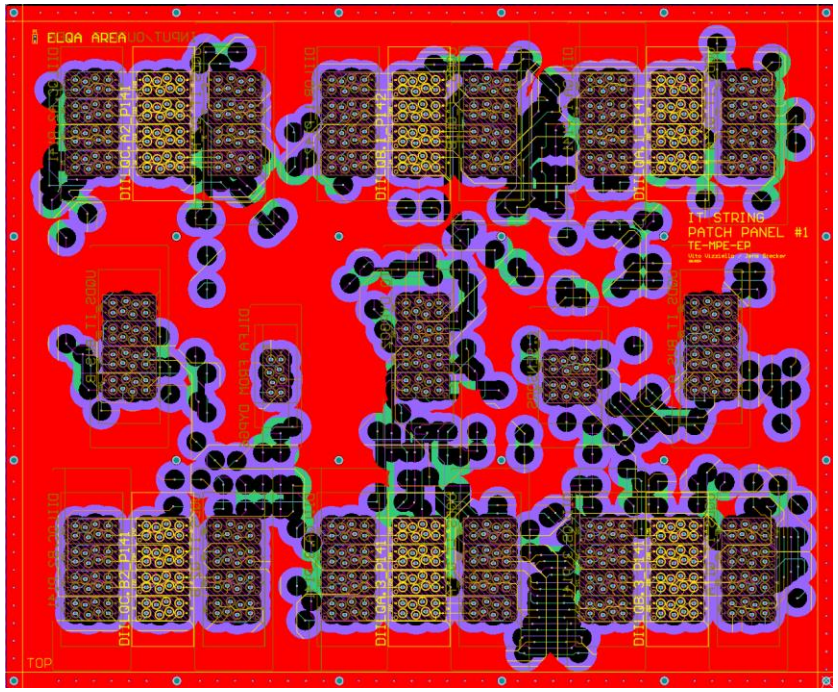


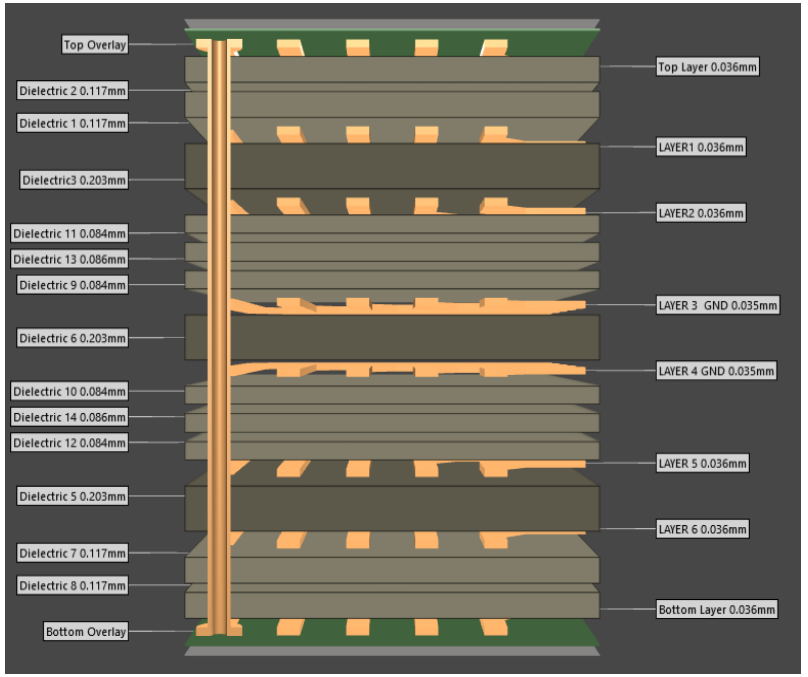




Development of the PCB

- PCB size: 3U, 6U, 9U
- Number of layers of the PCB: 8
- Number of dielectric layers: 13



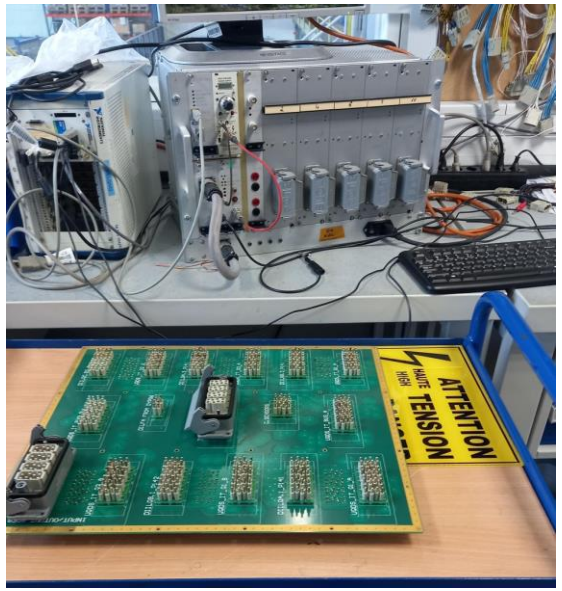


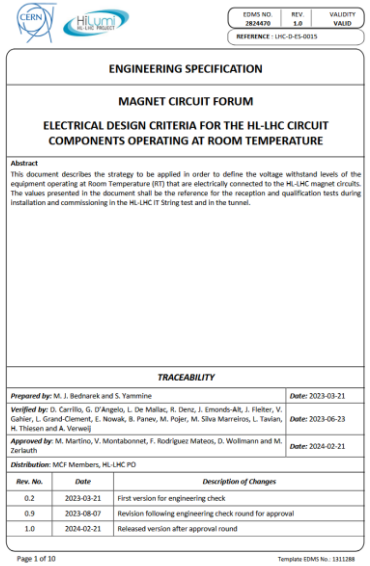
HV test validation

HV test validation by TE-MPE-PE

- The QDS Input Patch Panel must withstand a minimum of 2.5 kV for 60 s with no breakdown and a maximum leakage current of 10 µA.

- Each connector at 1 kV must have a leakage current of less than 0.1 µA after 60 s.





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REFERENCE : LHC-D-ES-0015

ENGINEERING SPECIFICATION

MAGNET CIRCUIT FORUM

ELECTRICAL DESIGN CRITERIA FOR THE HL-LHC CIRCUIT COMPONENTS OPERATING AT ROOM TEMPERATURE

Abstract

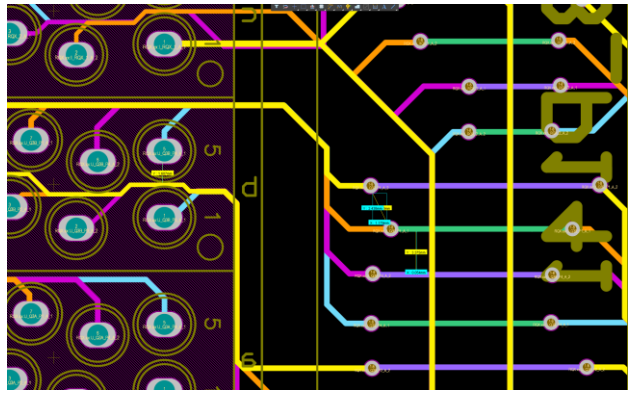
This document describes the strategy to be applied in order to define the voltage withstand levels of the equipment operating at Room Temperature (RT) that are electrically connected to the HL-LHC magnet circuits. The values presented in the document shall be the reference for the reception and qualification tests during installation and commissioning in the HL-LHC IT String test and in the tunnel.

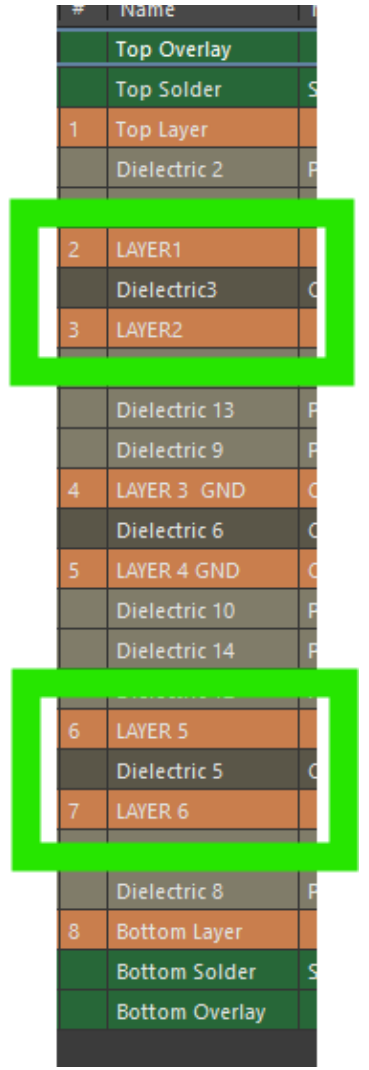
TRACEABILITY

Prepared by: M. J. Bednarek and S. Yammine	Date: 2023-03-21
Verified by: D. Carrillo, G. D'Angelo, L. De Mallac, R. Denz, J. Emonds-Alt, J. Fleiter, V. Gahier, L. Grand-Clement, E. Nowak, B. Panev, M. Pojer, M. Silva Marreiros, L. Tavian, H. Thiesen and A. Verweij	Date: 2023-06-23
Approved by: M. Martino, V. Montabonnet, F. Rodriguez Mateos, D. Wollmann and M. Zerlauth	Date: 2024-02-21
Distribution: MCF Members, HL-LHC PO	

Rev. No.	Date	Description of Changes
0.2	2023-03-21	First version for engineering check
0.9	2023-08-07	Revision following engineering check round for approval
1.0	2024-02-21	Released version after approval round

Page 1 of 10 Template EDMS No.: 1311288





Thank you

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