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ALICE ITS3 MOnolithic Stitched sensor with Timing (MOST): design overview and measurements highlights

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The MOST (Monolithic Stitched Sensor with Timing) is a 25.9\,cm-long wafer-scale pixel sensor prototype that bridges generic R\&D for future High Energy Physics (HEP) detectors with the developments aimed for the ALICE Inner Tracking System (ITS3).
Its main purpose is to investigate the yield of high-density pixel architectures, assess the timing capabilities of asynchronous readout, investigate an alternative sensor biasing scheme, evaluate yield enhancing power segmentation and verify a robust bias distribution method resilient to fluctuations of supply voltages.

This contribution presents both the design overview of the MOST chip and key measurements that validate its functionality and performance.

Summary (500 words)

The Monolithic Stitched Sensor with Timing (MOST) is a wafer-scale detector prototype developed to explore a stitching technique in the context of future High Energy Physics (HEP) applications, in particular for the ALICE Inner Tracking System upgrade (ITS3).
The MOST chip, measures 25.9\,cm\,×\,2.5\,mm and incorporates 40 pixel matrices with 18\,×\,18\,μm^2 pixels, which are distributed along the full length of the chip and are read out via shared global transmission lines.

MOST addresses several key R\&D objectives in the development of large-area monolithic sensors. It implements a global power delivery scheme, where analog and digital power domains span the entire chip, while small matrix sections (∼300 pixels) can be selectively connected or disconnected from the global network using integrated power switches. This design therefore allows regions with production defects to be isolated, enabling high-density designs without compromising the chip yield. This powering scheme has been silicon proven by MOST and adopted for the full-scale, full-functionality ITS3 detector prototype (MOSAIX).
Moreover, measurements show high pixel yield of above 99.99\% (achieved despite the high integration density over the pixel matrix) paving the way for more compact future designs.

Another feature of MOST is its asynchronous, data-driven readout. When a hit occurs, a pixel group sends a data packet containing its address serially to the CML outputs in the endcap via 1\,Gb/s CMOS transmission line spanning over the full length of the chip (25.9\,cm).
Thanks to the fixed time delay between hit and the data packet transmission the time-of-arrival (ToA) and time-over-threshold (ToT) can be measured, which allows the study to what extent the timing information can be preserved on-chip over a wafer-scale distance.
Experimental results indicate the full-length readout path jitter of 200\,ps, while the jitter for calibration pulse (that also span over the entire chip) is measured to be 12\,ps. The origin of the difference between these two values is under investigation.

MOST also explores an alternative sensor reverse-biasing method, achieved by shifting up the input branch of the front-end circuitry rather than by applying negative voltage to the substrate. This allows the substrate to remain at ground potential, simplifying chip design and integration. Measurements show that by applying shift voltage (VS) of 1\,V one can half the input node capacitance and the pixel noise, while further VS increase gives only minor improvement. Additionally, MOST also features a novel bias distribution scheme that is resilient to power supply variations allowing the generation of reference voltages in the endcap and their

distribution across 25.9\,cm distance, where local regeneration circuits replicate the intended currents and voltages.

This work presents a comprehensive overview of the MOST chip architecture and its experimental validation. Measurements confirm the chip's functionality, with a pixel yield above 99.99\%. Experimental results validate key architectural concepts such as power gating, sensor reverse biasing via the front-end shift and 1 Gb/s data transmission over 26 cm. This provides an important input for the next generations of large-scale monolithic sensors for HEP.

Author: BUGIEL, Szymon (CERN)

Presenter: BUGIEL, Szymon (CERN)

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