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On-Chip Data Transmission for Wafer-Scale MAPS

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Wafer-scale monolithic active pixel sensors (MAPS) for particle detectors face significant challenges in on-chip data transmission due to high resistance and capacitance in CMOS interconnects, leading to signal distortion, attenuation, dispersion, and inter-symbol interference (ISI). This contribution outlines these issues in the ALICE ITS3 MOSAIX chip and presents current solutions by implementing differential low swing transmission across stitched tiles, achieving 160 Mb/s over ~12 mm and better performance compared earlier stitched wafer prototypes (MOSS and MOST). As a future direction to push the performance further, this work also highlights the Backbone Transmission Line Encoding (BTLE) Driver system. This advanced solution, designed in same the technology as MOSAIX, uses a low-power transmitter with digital pulse shaping, line coding, and polyphase FIR filtering to mitigate ISI, enabling repeaterless 160 Mb/s links over 10 cm with a FoM of 37.3 fJ/bit/mm.

Summary (500 words)

Large-area, stitched Monolithic Active Pixel Sensors (MAPS) are crucial for next-generation particle detectors, such as those for the Electron-Ion Collider and the ALICE ITS3. A primary challenge in designing these wafer-scale sensors, is transmitting high-speed data from numerous pixel matrices to readout processors without compromising power, signal integrity, or the active pixel area. The data links implemented in MOSAIX rely on a differential transmission architecture with a low-voltage swing. The main advantages are power efficiency, immunity to supply noise, and reduction of noise injection into sensing nodes, allowing for the physical implementation of the data lines on top of the pixel region without affecting analog performance. Current solutions, as implemented in ALICE ITS3 prototypes, address these challenges through innovative on-chip transmission schemes. In MOSS, a stitched backbone (SBB) used single-ended CMOS buffers repeated every 3.2 mm, supporting up to 40 Mb/s but suffering from high power dissipation (due to charging parasitic capacitance to VDD/VSS) and noise coupling into front-ends. MOSAIX advances this with differential, low-voltage swing architecture, enabling 160 Mb/s over ~12 mm at ~1 pJ/bit/cm—improving speed and distance by ~4× and power by >3× compared to MOSS. The buffer comprises a receiver (RX) with a dynamic comparator and SR flip-flop for sampling, and a transmitter (TX) with a programmable capacitive driver that reduces swing to ~100 mVpp-diff, minimizing dynamic power ($\propto C_{\text{line}} \cdot VDD^2$). A 1-bit current-steering DAC sets DC levels, eliminating the need for DC-balanced streams. Lines routed over pixel regions maintain analog performance due to noise immunity. Extensive post-layout simulations validate static/dynamic timing and SET resilience, ensuring reliable data capture amid metastability risks along the 2×26 cm paths. Pushing the boundaries for future wafer-scale detectors requires a more advanced, repeaterless solution capable of spanning even greater distances. The BTLE Driver system is presented as the future direction for this technology. Raw waves are spectrally inefficient; pulse shaping limits bandwidth, concentrates energy, and minimizes ISI at sampling points. The BTLE transmitter chain features duobinary encoding, upsampling, and a parallel-processed 33-tap FIR filter with raised-cosine shape and integrated pre-emphasis tailored to channel characteristics. Partitioned into four phases operating at 160 MHz (multiplexed to 640 MHz), it eases timing while driving a 6-bit current-steering DAC for differential analog output. Fixed-point coefficient quantization optimizes precision and hardware efficiency. Simulations confirm open eye diagrams with negligible ISI, achieving a FoM of 37.3 fJ/bit/mm—pivotal for EIC MAPS and beyond.

The differential low-swing scheme demonstrated in MOSAIX provides a proven, low-noise, pixel-compatible

backbone for per-tile and inter-tile hops at 1022Mb/s over centimeter-class distances, dramatically improving on the SBB repeater approach. BTLE complements this by digitally shaping the spectrum for reliable 10-cm-class wafer-trunk links without repeaters, preserving active area and minimizing power. Together, these techniques define a scalable wafer-level architecture: local aggregation across tiles via low-swing differential links, followed by digitally pre-emphasized BTLE trunks to the LEC for high-integrity, low-power delivery to off-chip serializers. This integrated roadmap addresses present constraints while charting an upgrade path for future wafer-scale MAPS readout.

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