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28 nm MOS Transistor SPICE BSIM Model for Simulating Electrical Effects of 1-Grad Total Ionizing Dose based on Gate Oxide Capacitance

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There are no existing SPICE models that account the effects of radiation doses exceeding 1 GRad in global transistor-level simulations for analog design in 28 nm CMOS technology within Electronic Design Automation environments. We present RAD-BSIM, the first SPICE model based on Berkeley Short-channel IGFET Model (BSIM) leveraging gate-oxide capacitance variations to enable robust circuit design up to 1 GRad. RAD-BSIM translates the effect of radiation-induced charge trapping at gate oxide, spacer, and shallow trench isolation layers into an equivalent variation in gate oxide capacitance. The model's accuracy is validated by comparing RAD-BSIM simulated electrical characteristics with corresponding experimental measurements.

Summary (500 words)

Developing advanced readout and processing ASICs is a key enabler for next-generation High-Energy Physics (HEP) experiments, where precise 4D tracking (position and timing), as targeted by the IGNITE[1] project, must be maintained even under extreme radiation conditions. These integrated circuits must operate reliably in environments with Total Ionizing Doses (TID) over a 1 GRad, as expected in future high-intensity collider experiments. To address this challenge, accurate circuit simulation models are essential. While charge- and physics-based models have been integrated into EKV models for Technology Computer-Aided Design (TCAD) environments, there is currently no SPICE-compatible Berkeley Short-channel IGFET Model (BSIM) that accounts for Total Ionizing Dose effects in 28 nm bulk CMOS technology for circuit simulations in Electronic Design Automation (EDA) environments. In this work, we present RAD-BSIM, the first SPICE model based on BSIM leveraging gate-oxide capacitance variations to enable robust circuit design up to 1 GRad. The effect of damage caused by Total Ionizing Dose in CMOS MOSFET technology involves primarily the oxide layers, which result the most sensible, including the gate oxide (High-k), spacer oxide, and shallow trench isolation (STI) layers (SiO_2). This damage is attributed to the radiation-induced charge traps located in this oxide layer, which cause an alteration of the charge concentration profile in the channel and depends on multiple radiation-related parameters and device-specific characteristics including channel doping profile, impurity concentration, geometry (e.g., W/L ratio), and applied bias conditions. Our modeling approach encapsulates the cumulative impact of charge trapping across different oxide layers into a single equivalent effect, represented by a variation in the effective gate oxide capacitance per unit area (C'_{OX}). This abstraction facilitates the integration of TID-induced degradation effects into compact models suitable for circuit-level simulations. By an accurate choice of the value of C'_{OX} using the electrical response of irradiated devices, our models enable precise tracking of current electrical characteristics as well as the key MOST parameters (e.g., threshold voltage and source-drain resistance) after exposure to up to 1 GRad. The variation observed in the key parameters from the nominal BSIM to the RAD-BSIM model closely matches the variation measured experimentally between pre-radiation and post-radiation conditions at 1 GRad.

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Author: GELMI, Luca (INFN section Milano-Bicocca and University of Cagliari)

Co-authors: Prof. BARBARO, Massimo (University of Cagliari); Prof. DE MATTEIS, Marcello (University of Milano Bicocca)

Presenter: GELMI, Luca (INFN section Milano-Bicocca and University of Cagliari)

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