



Contribution ID: 91

Type: Poster

Development of a triggerless readout energy measuring and timestamp ASIC for silicon microstrips sensors

Tuesday 7 October 2025 15:00 (20 minutes)

The new version of ToAST as a radiation tolerant readout for silicon microstrips sensors, has been produced and it is now under characterization. It is implemented in a 110 nm commercial CMOS technology, and it is synchronous to a 160 MHz clock. A common time stamp is used to provide both particle time of arrival and energy particle information with ToT technique. Triple logic is applied to all configuration registers of 64 channels and in the global logic circuit for protection against single event upsets. Enclosed gate layout has been used for the analog switches to protect against TID leakage.

Summary (500 words)

A second version of ToAST (Torino ASIC for Strip detectors) has been designed and produced to increase TID (Total Ionizing Dose) resistance achieved with the first prototype (limited to 0.5MGy) and improve its Single Event Upset (SEU) tolerance.

The development of this triggerless readout energy measuring and timestamp ASIC for silicon microstrips sensors is in the framework of a future experiment dedicated to antiproton physics at FAIR and designed within the project REST (REadout STRip) at INFN.

This version is a full-size 64 channel integrated circuit, designed in the 110 UMC CMOS technology, with a die size of $4.4 \times 3.2 \text{ mm}^2$.

The microstrips sensor is connected to the chip on one side leaving on the opposite side the connection to all the electrical lines (supply, control and data transmission), thus allowing multiple dies being placed very close to each other.

Its analog front-end features the following parts: a charge sensitive preamplifier which can be programmed to accept signals of both polarities, a programmable shaper and a current buffer, a Time-over-Threshold (ToT) stage with linear discharge and two comparators with independent thresholds.

The lower threshold provides the time information, the higher one validates the event, thus reducing both the jitter for small signals and the noise-induced events.

The arrival time of the two edges of the comparator is measured by storing the corresponding value of a global time stamp reference signal, which is distributed to all channels. The rising edge time stamp provides the time of arrival and the difference between the two timestamps provides the ToT information.

The channels are grouped in regions made of 8 channels each, which provide local buffering. The event information is formatted in a 32bit word and transmitted over two serial links at 160Mb/s by a global controller. 144 registers can be tuned to optimize the performance of the chip.

The digital logic has been triplicated for SEU protection, both into the two configuration registers of each channel and in the global logic circuit. To improve the TID tolerance, enclosed gate layout has been adopted for the n-transistors in all the analog switches, which appear to be the most critical parts.

In the first results in laboratory, a non-linearity of the ToT gain is less than 1% (r.m.s.) in the range 1.5-16fC has been achieved.

The ToT gain spread among channels is large but can be reduced by the channel calibration DACs to less than 2% for gain around 55ns/fC (n-type) and around 42ns/fC (p-type).

The time jitter is below one clock cycle (6.25ns) for the leading edge and around 3 clock cycles for the trailing

edge. The noise shows an amplitude of few hundreds of electrons without sensor.

An irradiation test with ions to assess the effectiveness of the protection against SEUs has been performed and from first analysis of the channel registers, the cross section of SEU, evaluated in a hadronic environment, is less than $1 \times 10^{-16} \text{cm}^2/\text{bit}$.

Further characterization is foreseen in the next months, including a TID test with X-ray source.

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Session Classification: Poster 1

Track Classification: ASIC