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Results from tests of the Ignite32/64 ASICs in CMOS 28-nm technology

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The INFN IGNITE project plans to implement a large-area ASIC (order 1-2 cm2) aimed at fast 4D-tracking. System pixels are required to have pitch below 50 µm and time resolution better than 30 ps. In the present paper we present measurement results concerning the performance of the two prototype ASICs, the Ignite32 and the Ignite64, designed to readout respectively 32x32 and 64x64 pixel matrices having 55 µm pitch, developed within the AIDAInnova initiative. The internal architecture of the ASICs, their modular concept and tested performance on time resolution are illustrated in this work.

Summary (500 words)

The INFN IGNITE project is developing technical solutions for the next generation of trackers at colliders (4D-trackers), which may require high time resolution measurements at the pixel level (< 30 picoseconds on the electronic side), while keeping the pixel size (≤ 50 µm) and system power consumption substantially unaltered with respect to the present generation of inner tracking systems (1-2 W/cmˆ2).

IGNITE project plans to implement a Large-Area (LA) ASIC (order 1-2 cm2) and finally an integrated demonstrator comprising sensor, electronics, and fast readout. As an intermediate step, two ASICs, the Ignite32 and the Ignite64, have been designed and fabricated to readout respectively 32x32 and 64x64 pixel matrices having 55 µm pitch. A modular architectural concept allowed to produce the Ignite64 as a 4-time replica of the Ignite32.

The Ignite32/64 development has the following main purposes:
1. Characterization of Front-end performance (Analog F/E and TDC).
2. Test of biasing strategy for power integrity on the analog part.
3. Test of clock distribution strategy.
4. Hybridization and timing sensor characterization onto AIDA-Innova sensors (FBK 3D-Trench and TI-LGAD, CNM 3D-DS columns, CNM I-LGAD), all having 55 µm pixel pitch.
Item 1 is decisive both about the validation of circuit solutions in view of the LA-ASIC, now being designed, and the fruitful test of high-resolution timing sensors (item 4), for which now no alternative read-out solutions exist, neither is foreseen in the short term. Items 2 and 3 are crucial for the LA design and decisive concerning the final timing performance of the ASICs (therefore also for items 1 and 4). The ASIC architecture and global line distribution strategy are organized following a rigorous modular (or better fractal) structure, which is meant to be extended onto the LA device. Therefore, it is considered important to study their effectiveness not only by simulation, but on the testbench as well.

The ASICs have been characterized on a dedicated testbench in the laboratory both in stand-alone mode and after hybridization with 3D-trench sensors from the 2024 AIDAInnova batches. The talk will pivot on the following points:
• The internal architecture of the ASICs, their modular concept and its tested effectiveness.
• The tested performance of AFE and TDC on time resolution, compared with the project final requirements.
• Ongoing work on a mini-tracker demonstrator, which is in preparation for a test-beam at SPS.

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