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Advancements in a Test Stand for Inner System Electrical Links of the ATLAS Inner Tracker (ITk) Upgrade Silicon Detector

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Over the past year, significant progress has been made in the development of a dedicated test stand designed to evaluate the signal transmission integrity of approximately ˜9k electrical links used in the Inner System (IS) of the ATLAS Inner Tracker Pixel upgrade. The Quality Control (QC) method of choice is a pre-existing multi-channel FPGA data acquisition architecture that has the capability of producing Bit Error Rate (BER) tests and virtual eye diagrams at a data rate of 1.28Gb/s. This presentation includes the developments in the calibration of the QC infrastructure and results from multiple IS pre-production bundles.

Summary (500 words)

Of the ˜26k electrical links –comprising of data and command channels operating at 1.28Gb/s –used by the Outer Barrel (OB), Outer Endcap (OE), and Inner System (IS) subsystems of the ATLAS ITk upgrade, ˜9k links will be used for the IS readout. Specially developed Twinax cables that meet the radiation requirements, material budget, and signal loss of ≤13 dB at 640MHz will serve as the electrical links between the front end of the detector and optical readout. These E-links are grouped into various types of bundles, depending on subsystem configuration with challenging custom fabrication. Some IS bundles contain as many as 100 E-links densely packed together in very restricted space for solder termination on fine pitched pads. A rigorous and versatile QC process is therefore essential for qualifying these bundles.

The use of high-speed oscilloscopes to test individual links proves to be too slow to qualify the large number of links used in the ITk upgrade. A pre-existing FPGA architecture developed by SLAC with the capability of scanning up to 32 links at a time is the baseline system that speeds up the process of qualifying links with little user intervention through the use of a large number of MGTs. This system uses the Xilinx iBERT utility to match ITk's pixel data rate of 1.28Gb/s and simultaneously produces BER tests and virtual eye diagrams displayed in the Vivado interface. Offline software is used to analyze Vivado's output of the scanned links. The QC scheme is fast and effective at identifying broken infrastructure channels and faulty electrical links. A scan of 30 links used in the calibration of the test stand takes ˜3 minutes to complete demonstrating the speed at which subsystem bundles can be QC'd.

Non-uniformity of channels in the infrastructure prove to be a challenge in the total calibration of the QC test stand. A series of mini-DisplayPort (mDP) cables of various lengths are employed as references of difference loss levels to better understand the available channel configurations the infrastructure offers.

Between SLAC, CERN, and Edinburgh three functional test stands exist and have undergone extensive calibration tests over the past year. Advancements in the channel performance across the three systems through calibration and bundle tests have provided insights into usable and unusable channels, giving the team a smoother path to a functioning QC test stand. This presentation highlights the most recent results in the calibration as well as results from pre-production IS bundles. Combined, these results demonstrate the current performance of the test stand as a QC tool for the full production of IS ITk Pixel Twinax assemblies.

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