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# ”Unexpected talk” - GRAPH readout ASIC for large aperture, high resolution single photon imaging detectors designated for space applications

*Thursday 9 October 2025 09:00 (16 minutes)*

Large aperture, high resolution, single photon imaging detectors are in high demand for future space explorations by missions
such as HABEX or LUVOIR. Yet making a TRL 10 operational detector prooved to be a very challenging endavour that takes more than
a decade. This talk will review the state of the art technology, and present more in depth an ASIC designed to cope
with the requierd operatioanl parameter space. To complement, some fresh results obtained operating the ASIC on the detector will be presented.

## Summary (500 words)

This paper presents a methodology using Cadence Xcelium to accelerate gate-level Fault Injection (FI) simulations for digital integrated circuits. We evaluate three designs of varying complexity, including open-source AES and SHA256 cores from Secworks, extended with an AXI4-Lite interface and validated with NIST-standard test vectors. As a more complex case study, we include the Ribex ASIC, a radiation-tolerant RISC-V SoC developed at KU Leuven. Fabricated in TSMC 65nm technology, Ribex features a dual-lockstep Ibex RISC-V core, error correction, and checkpointing for state rollback. Our approach enables efficient Single Event Effect (SEE) analysis, integrates with existing verification flows, and improves scalability and accuracy. Table 1 summarizes the designs and their testbench cycle counts and performance at gate-level.

The framework is based on the Checkpoint-Restore Boot (CRB) principle, which enables re-execution from saved simulation states, and is enhanced with Hashing-based Checkpoint Differentials (CDIF). It supports multiple abstraction levels, including RTL, generic RTL (Verilog cell primitives), and gate-level representations. In addition to Single Event Effect (SEE) injection, it offers statistical tools to sample injection population size based on design specifications, allowing users to quantify error rates and confidence levels for FI verification. A built-in performance profiler helps optimize settings based on the size and complexity of the Device Under Test (DUT), ensuring efficient simulation runtimes. The framework also includes a two-stage result analyzer to improve detection of false positives and silent faults. Accuracy is enhanced by progressively refining validation, starting with hash-based comparisons and escalating to bit-level precision. The first stage checks whether faults vanish at the checkpoint mark; retained faults are then re-simulated with bit-level accuracy, as illustrated in Figure 2.

The main performance metric in this study is simulation cost, expressed in Cycles per Second (CPS) and total execution time. Measurements are obtained using Cadence Xcelium’s built-in profiling tool. All simulations are performed on an 8-core AMD EPYC 7313 system with 64 GB of RAM.

Various CRB interval sizes were evaluated for their impact on simulation cost, as shown in Figures 3 and 4. Each CRB interval supports an arbitrary number of injections and is simulated by a single CPU, enabling multi-threaded execution across intervals. Table 1 presents the average CPS and execution time for the Ribex, SHA256, and AES testbenches without fault injection (FI). For a single 100-cycle CRB interval without FI, CPS remains comparable to standard gate-level simulation. However, since only a short time slice is simulated,

execution time drops to tens of milliseconds for smaller designs (AES/SHA256) and hundreds of milliseconds for larger ones (e.g., Ribex). With FI enabled, the same snapshot yields CPS values of 6,398.47 (Ribex), 67,530.97 (SHA256), and 66,154 (AES), with corresponding runtimes of 0.278 s, 0.018 s, and 0.019 s, as shown in Figure 1. Although golden reference generation and SEE injection introduce per-checkpoint overhead, multi-threaded CRB execution maintains simulation throughput comparable to single-threaded gate-level testbench runs without FI—even on resource-constrained systems.

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