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Development of Low-Mass Flex PCB and Nanowire Interconnect Technologies for HEP Module Integration

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The development of lightweight flex PCBs and nanowire-based thermal interfaces for low-mass, high-performance detector modules are presented. A novel manufacturing approach enables flex circuits with double-sided pad access, assembled using ACF and gold studs. Signal integrity was simulated and validation trials conducted on test structures. For thermal management, sintered and glued nanowire interfaces were evaluated against silver paste and adhesives. These results provide quantitative design guidance for minimal-mass, scalable packaging in HEP detectors.

Summary (500 words)

Efforts to reduce the material budget in high-energy physics (HEP) detectors—without compro-mising signal integrity or thermal management—are central to next-generation module design. We present two ongoing activities addressing these challenges: (1) the fabrication of ultra-thin flex PCBs with double-sided pad access for low-mass interconnects, and (2) the evaluation of nan-owires as a novel thermal and electrical interface for sensor modules.

Flex PCB Prototyping and Assembly:

Thin film flex PCBs are often subject to tight design constraints, such as single-side pads, high cost, and long turnaround times. This makes them impractical for modular high-density assemblies and for prototyping. To address this, we have been developing a novel process to produce flex PCBs with both top and bottom pads. This involves using a sacrificial separation layer between the copper-clad polyimide stack and the rigid carrier during fabrication. The layer allows clean removal after processing while preserving precise layer alignment and structural stability.

Initial prototypes have a total thickness below 50 µm and routing geometries suitable for frequen-cies up to 1 GHz. Assembly into test module chains was achieved using anisotropic conductive film (ACF) bonding and gold stud bumping, enabling scalable interconnects compatible with au-tomated production.

Signal integrity simulations are underway using Ansys HFSS and ADS Keysight to characterize impedance, transmission, and crosstalk. Corresponding test structures have been fabricated and are under evaluation to validate these results experimentally. The objective is to establish a quantitative design guide that can inform the layout, bonding, and stack-up of low-mass flex solutions in detec-tor modules.

Nanowire Thermal Interconnect Studies:

We are also investigating nanowire-based interfaces as alternatives to conventional thermal pastes and conductive adhesives. Metallic nanowires, applied through sintering or adhesive bonding, promise low thermal resistance and adequate mechanical compliance for sensor attachment.

Nanowire samples are being characterized for thermal conductivity using test structures and infra-red imaging. They are also being benchmarked against silver paste, thermal grease, and adhesives. Preliminary data suggest potential for thermal conductivities in the range of 50 $W/cm^2 \cdot K$.

In addition to heat transfer, nanowire layers offer intrinsic electrical conductivity, which could pro-vide uniform backside bias distribution—an important consideration in large-area or high-voltage sensor designs. Early tests are exploring electrical performance and contact stability under thermal cycling.

Challenges and Outlook:

Key challenges include preserving flex integrity during release from the substrate and achieving reliable ACF bonding over curved or uneven geometries. For nanowires, optimizing the sintering or adhesive bonding process to avoid voids and ensure repeatability is a major focus.

These developments represent promising initial steps toward practical solutions for high-density, low-mass detector packaging. Both the flex PCB and nanowire interconnect technologies aim to meet the integration needs of future HEP experiments.

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