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Advancements and future expansions of the Caribou DAQ system

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Caribou is a versatile data acquisition system developed for use in several collaborative frameworks (CERN EP R&D, DRD3, AIDAinnova, Tangerine) to support laboratory and test-beam characterization of novel silicon pixel detectors. It combines a custom Control and Readout (CaR) board with a Xilinx Zynq System-on-Chip (SoC) running project-wide shared firmware and software stacks. Ongoing migration to Zynq UltraScale+ platforms aims to integrate SoC functionality directly into the CaR board, enhancing system performance and compactness. This contribution introduces the Caribou system and outlines recent progress across its hardware, firmware, and software components.

Summary (500 words)

Caribou is a modular data acquisition (DAQ) system designed for fast prototyping and qualification of silicon pixel detectors in laboratory and test-beam environments. As a generalized platform, it is used by various detector development projects across over 14 institutes and under multiple collaborative frameworks. Its architecture prioritizes reusability, flexibility, and ease of integration, enabling so far more than 15 silicon detector prototypes to be tested. The system is built around a custom Control and Readout (CaR) board and a Xilinx Zynq System-on-Chip (SoC) platform. The CaR board provides essential interfaces such as programmable power supplies (up to 8 channels with < 10 mV resolution), voltage/current references, fast ADCs (up to 65 MS/s), injection pulsers, and various types of I/O lines for readout and control. It connects to the SoC via FMC and to a user-designed chip board through a SEARAY connector, enabling detector-specific adaptation while retaining a common, maintainable DAQ backbone. The SoC runs an embedded Linux distribution built with Yocto and integrates two central components: Peary, a C++ software framework that provides hardware abstraction, configuration, logging, and multi-device control via CLI and Python interfaces; and Boreal, a firmware infrastructure offering reusable IP cores and automation scripts for synthesis and simulation. Firmware is implemented using Vivado Block Design, allowing detector-specific user logic to co-exist with shared control infrastructure. Supporting heterogeneous detector designs while maintaining a unified environment posed a major challenge. This was addressed by enforcing a strict separation between user and common logic in firmware and adopting a modular structure in the software framework. For instance, new detector protocols can be implemented as Peary device classes, while firmware blocks can be added or modified with minimal integration effort.

`Recent hardware developments include the CaR v1.5 board, which addresses signal integrity issues by replac`

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