Contribution ID: **147** Type: **Poster**

An Highly Integrated Detector Readout Module for Fast Prototyping Using RFSoC

Thursday 9 October 2025 18:40 (20 minutes)

We present a flexible detector readout prototyping module based on the AMD RFSoC platform, integrating fast ADCs, DACs, programmable logic, multicore CPU and several 28 Gbps-class transceivers. Sampling at GHz rates enables full digital signal processing, simplifying analog front-ends and improving timing and compactness. Two use cases are demonstrated: a digital emulation for the NA62 Liquid Krypton Calorimeter trigger and readout chain, and early prototyping of readout electronics for the EPIC MPGD Endcap Tracker. This approach accelerates development and co-design of detectors and front-end electronics, paving the way for scalable and customizable DAQ systems in high energy physics.

Summary (500 words)

Radio Frequency System-on-Chip (RFSoC) technology, originally developed for wireless communication and software-defined radio, is now attracting growing interest in scientific instrumentation, including high energy physics (HEP). Its main advantage lies in the tight integration of high-speed ADCs, DACs, programmable logic with a large number of DSP slices, and processing cores (ARM CPUs) within a single device. In addition to these elements, RFSoC platforms also integrate several 28 Gbps-class transceivers, enabling the implementation of high-throughput networking protocols. Platforms such as the AMD Xilinx ZCU216 board, featuring 16 14-bit ADCs at 2.5 GSPS and 16 14-bit DACs at up to 9.85 GSPS, enable unprecedented flexibility and compactness in developing front-end electronics and prototyping data acquisition systems.

Although HEP applications typically operate at much lower sampling rates (on the order of 100 MHz), adopting RFSoC solutions opens new opportunities. GHz-range sampling enables a dramatic simplification of analog front-end electronics by reducing or eliminating the need for analog shaping circuits. Instead, signal processing can be performed entirely in the digital domain, allowing for highly customizable and precise transfer functions. This shift can lead to reduced power consumption, smaller footprint, improved synchronization, and simplified data transport across multiple channels.

In this work, we present the development of a highly integrated and reconfigurable detector readout prototyping module based on the ZCU216 RFSoC platform, with applications demonstrated in two distinct use cases.

The first use case targets the Liquid Krypton Calorimeter trigger and readout system of the NA62 experiment at CERN. The current front-end uses a 9-pole Bessel analog filter to produce pseudo-Gaussian pulses. We developed a testbench that emulates the calorimeter signals using the RFSoC DACs, which are then looped back into the ADCs sampling at 2.5 GSPS. The digital implementation of the shaping function enables direct comparison with the existing system, with the aim of evaluating, for example, the efficiency of pile-up mitigation strategies or improving energy resolution and energy peak reconstruction. We report the results of a full 16-channel testbench implementing the complete trigger and readout chain, including performance figures such as timing, resolution, and resource usage.

The second use case involves the Micro-Pattern Gaseous Detectors (MPGDs) for the Endcap Tracker in the EPIC experiment at the future Electron-Ion Collider (EIC). Here, the RFSoC platform serves as a fast prototyping environment to emulate the functionality of the custom front-end ASIC currently under development. A simple electrical interface couples μ-RWELL detector strips to the platform's ADCs, allowing real-time acquisition of detector signals. This approach enables early testing and validation of front-end concepts before ASIC availability, streamlining the co-design of detector and electronics.

These results highlight the potential of RFSoC platforms in accelerating development cycles, enabling precise digital signal processing, and simplifying analog front-ends in particle physics experiments.

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Session Classification: Poster 2

Track Classification: Module, PCB and Component Design