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The challenges of integrating a SoC platform into the CERN accelerator control system for the HL-LHC Beam Position Monitor system

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The data acquisition electronics for the new HL-LHC Beam Position Monitor system will be based on a RFSoc, a System-on-Chip with integrated high-speed Analog-to-Digital Converters and Digital-to-Analog Converters.

While modular systems based on industrial computers and FPGA modules are well known and supported across CERN's accelerators, SoC based systems are still novel, bringing new possible architectures and different integration challenges.

This paper describes the requirements for the integration of the HL-LHC BPM system and it describes a new integration model made possible by the SoC technology, analysing advantages and shortcomings with respect to a traditional modular architecture.

Summary (500 words)

The new HL-LHC Beam Position Monitor system will be installed for HL-LHC upgrade close to the interaction region and will be sensitive to both counter-rotating beams.

The data acquisition electronics will acquire 8 channels in parallel at multi-giga-sample rate and perform inter-channel data processing to compute bunch-by-bunch position and perform beam-to-beam correction at 40 MHz. For this reason, the system will be based on a RFSoc, a System-on-Chip with integrated high-speed Analog-to-Digital Converters (ADC) and Digital-to-Analog Converters (DAC).

In the scope of this paper, a System-on-Chip (SoC) is an integrated circuit containing a CPU or processing system, memories, input/output interfaces and programmable logic. An RFSoc integrates RF components as well, as ADCs and DACs.

While modular systems based on industrial computers and FPGA hardware modules are well known and centrally supported for their integration in CERN's accelerator control system, SoC-based systems are still novel, bringing new possible architectures and different integration challenges.

In fact, integrating a system in CERN's accelerator control infrastructure implies several requirements. Some examples that apply to HL-LHC BPM and that are presented in this paper: the system needs to be accessible through CERN's technical network using standard protocols and standard software frameworks; it shall be able to receive the accelerator's timing signals; it shall be possible to remotely reset it and power cycling it; if it hosts an OS and is in the technical network it shall be possible to update such OS with security patches, read its system logs and have a remote console for maintenance.

The paper proceeds to identify two main ways the HL-LHC BPM SoC-based system can be integrated into the accelerator controls. The first as an FPGA hardware module, needing a standard front-end computer (FEC) as host; in this case the integration is implemented in the FEC, and the system needs the identification of standard protocols and drivers for interfacing the SoC and the FEC. The second as a standalone system, for which the currently supported FEC software stack is ported to the SoC processing system, and the border that traditionally sits between a FEC and an FPGA hardware module is physically and logically transferred within the silicon of the SoC. The advantages and disadvantages of both solutions are analysed, together with an identikit of the kind of applications that are better served by one or the other architecture.

Finally, the paper presents the reasons why the standalone architecture is chosen for the HL-LHC BPM system,

it describes how the system functionalities are consequently distributed among the SoC resources and which design choices are implemented to minimise the risks on the long-term maintenance of such an integrated architecture.

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