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The iFTDC Front-End Card for the COMPASS and AMBER Experiments

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The iFTDC is a low cost, simple and flexible front-end card designed to measure signal timing for different types of detectors with a precision of 150 ps. It's based on ARTIX-7 FPGA, has 64 LVDS inputs and few user IO pins for configuration of attached ASICs. The FPGA's built-in high-speed serial link connects the board to the DAQ using the Unified Communication Framework protocol. The iFTDC can be connected directly to Ethernet for laboratory measurements. The iFTDC firmware has built-in scalers and can be operated in streaming mode.

The performance and applications of the iFTDC cards are discussed.

Summary (500 words)

The iFTDC Front-End Cards for the COMPASS and AMBER Experiments

INTRODUCTION

The iFTDC was originally developed for the COMPASS experiment to provide a new modern front-end electronics for large area gas detectors such as MWPC, Straws, and drift chambers. The main component of the FE board is the ARTIX-7 FPGA, deliberately chosen for its low cost. The iFTDC has 64 channels with LVDS inputs. The TDC IP block is implemented in two versions with low and high resolution of 800 and 400 ps bin size respectively. The effective time resolutions are 250 ps and 150 ps. To integrate the iFTDC into the DAQ, we have included the UCF[1] IP core, designed for high-speed serial links. UCF supports multiple virtual channels. One channel provides deterministic latency for trigger information. The second channel is used for the IPBus interface. The third channel is used to read the data. The interface bandwidth is 3.04 Gb/s. For laboratory setups or small experiments, the iFTDC card can also be accessed directly via 1Gb Ethernet. In this case, the IPBus software remains the same, although the data is transmitted via a UDP link. The iFTDC card is equipped with two LEMO connectors, one for trigger input and one for trigger output. These signals allow several iFTDC cards to be synchronized with each other.

TDC IP Core Design

The TDC core uses a high speed shift register and programmable delay line available in each IO block. The maximum frequency of the shift register is 1.2 GHz. It defines a minimum bin size or time resolution. To achieve better resolution, we use two shift registers from adjacent IO blocks for one channel and program the delay lines to achieve a half clock period shift between two registers. The delays can be programmed with a step of 78 ps. The delay step defines a theoretical limit for differential non-linearity and in our case it would be 5%. However, measurements show that the DNL is in the order of 20% and is determined by other irregularities in the FPGA structure.

Scalers

Each TDC channel has a 32-bit scaler that is read out via the IP bus. The scalers are reset at the start of the SPS spill and provide an integral rate of each channel. The scalers run independently of the data acquisition and have multiple applications. In the AMBER experiment, CEDAR detectors are equipped with the iFTDCs. The scalers allow the CEDAR position to be aligned with the beam and the detector parameters to be optimized for the desired particle. The other application is related to streaming DAQ. One of the challenges of streaming DAQ is controlling the data rate to avoid saturation of the DAQ bandwidth. The scalers are used to determine the data rates before the start of a run, to optimize thresholds and to keep noisy channels under control.

1. D. Gaisbauer et al., "Unified communication framework," 2016 IEEE-NPSS Real Time Conference (RT), Padua, Italy, 2016, pp. 1-2, doi: 10.1109/RTC.2016.7543158.

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