TWEPP 2025 Topical Workshop on Electronics for Particle Physics



Contribution ID: 81 Type: Poster

A radiation tolerant digital quench detector for the LHC's superconducting main dipole magnets

Tuesday 7 October 2025 15:00 (20 minutes)

During LHC Long Shutdown #3, the base layer quench detectors for the LHC main dipoles will be upgraded to a new type. The new FPGA-based quench detectors are equipped with two galvanically isolated, high-resolution input stages that digitise the two dipole aperture coil voltages. This new digital design allows the quench detection settings to be changed remotely. As the detectors are installed below the dipole magnets, they have to withstand the radiation present during LHC operation, which can exceed 100 Gy/y at certain locations. This paper discusses the design, testing, component selection and implementation of the new detector boards.

Summary (500 words)

The quench detectors that monitor the superconducting main dipoles of the Large Hadron Collider (LHC) at CERN in Geneva were designed and built about 20 years ago. Although they have been in stable operation since the LHC was commissioned in 2008, an upgrade of these electronic boards is planned during the LHC Long Shutdown #3 (LS3) starting in 2026. The new quench detectors are designed to protect the magnets using the same algorithm as the existing quench detectors. However, while the existing detectors use an analogue Wheatstone bridge for inductive voltage compensation, the new digital detectors perform this step in the digital domain. In addition, the new detector will provide remote control of the quench detection settings and a higher resolution of the digitised signals for analysis purposes. As the quench detector will be installed in the LHC tunnel below the dipole magnets, it must be able to withstand the radiation received during operation, which can exceed 100 Gy/y at certain locations. With approximately 2500 quench detectors to be installed, reliability and availability are critical to accelerator operation.

This paper starts from the operating experience of the existing quench detectors and leads to the revised specification of the new type. With a maximum test voltage of 2500 V to ground (20 min) and a maximum short term differential input voltage of 1 kV, the analogue input stages require a robust design. Following the revised specification, the new design is shown in detail, focusing on the robust, high accuracy, galvanically isolated digitising analogue input stage. Coupled with a flash-based FPGA, these stages form the core of the quench detector. Component selection with respect to radiation tolerance is another aspect of the paper. Measurement results from working prototypes are presented. The results of a first radiation test (July 2025) at CERN's CHARM facility are also be included.

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Presenter: STECKERT, Jens (CERN) **Session Classification:** Poster 1

Track Classification: Radiation-Tolerant Components and Systems