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Readout Electronics System for the CEPC Reference Detector

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Abstract

The framework of the readout electronics system for the CEPC reference detector has been designed based on background simulations and the baseline design of sub-detectors. To maximize the possibility of new physics exploration, an architecture of front-end triggerless readout with a full back-end trigger has been chosen as the baseline. The detector front-end electronics will be mostly implemented with ASICs to the radiation tolerance requirements. Inspired from CERN common projects such as lpGBT, Versatile Link and bPol, a common data interface, realized by a chip-set FEDI (Front-End Data Interface ASIC), and a common power module PAL (Power At Load), will be used for all the sub-detector electronics. The back-end electronics can thus also benefit from this architecture, which features a unique interface protocol, and can be commonly designed for all sub-detectors. In this talk, we will introduce the overall design of CEPC sub-detectors electronics with their general requirements, the latest R&Ds, especially the ASICs and the common interface system. In the end, our research team will be introduced and the effort related to the DRD7 will be discussed.

Biography

Wei Wei is a professor at the Institute of High Energy Physics (IHEP), Chinese Academy of Sciences, and the leader of the electronics group there. He graduated from the University of Science and Technology of China (USTC) with a bachelor's degree in Physics in 2005 and received his PhD from IHEP in 2010. Since then, he has been involved in ASIC design, especially in the areas of pixel detectors and waveform sampling. He has led the design teams for the Photon Counting pixel detector of HEPS (High Energy Photon Source), the Charge Integration pixel detector for SHINE (Shanghai High Repetition Rate XFEL and Extreme Light Facility), and the CMOS Pixel Sensor chip Taichupix for the CEPC Vertex detector. He is leading the development of the CEPC Electronics System, and the author/editor of the electronics chapter in the Technical Design Report for the CEPC Reference Detector.

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