Contribution ID: **19** Type: **WG2 - Hybrid silicon sensors**

Novel silicon 3D-trench pixel detector fabricated on the 8-inch wafer utilizing CMOS processing technologies

Wednesday 4 June 2025 08:50 (15 minutes)

A novel 3D-Trench silicon pixel sensor featuring an enclosed deep trench surrounding the central columnar cathode will be developed in this project, the pixel size ranges from 25×25 μm2 to 150×150 μm2. The fabrication will be performed on the 8-inch CMOS pilot line at the Institute of Microelectronics of the Chinese Academy of Sciences (IMECAS). To reduce the dead area in the 3D sensor, the Bosch Deep Reactive Ion Etching (DRIE) technology is being developed to achieve an aspect ratio of more than 100:1. At least two batches of sensors will fabricated in this project, the first batch is expected to be delivered in 2026 and mainly used to validate the fabrication technology, the later batch will be delivered by 2027 and focused on the performance investigations targeting a position resolution of less than 10 μm, a time resolution of less than 50 ps and a radiation hardness of more than 1×1017 neq/cm2. Variations of this technology will also be developed in this project, for example double-sided 3D trench electrode detectors (DS-3DTED), back-incidence 3D composite electrode silicon detectors (3DCESD), hypothetical sphere-electrode detectors, novel 3D electrode LGAD.

Type of presentation (in-person/online)

online presentation (zoom)

Type of presentation (I. scientific results or II. project proposal)

II. Presentation on project proposal

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Session Classification: WG2/WP2 - Hybrid Silicon Technologies