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Studies on ML processing and compression of signal shared AC-LGADs

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Resistive Silicon Devices (RSDs), particularly AC-coupled Low Gain Avalanche Diodes (AC-LGADs), open the path of pico second level space and time (4D) tracking in high-energy physics (HEP) experiments such as those at the Large Hadron Collider (LHC), Electron-Ion Collider (EIC), and future (lepton) colliders facilities. These sensors combine the fine spatial resolution of segmented detectors with the excellent timing performance of LGADs, achieving nearly 100% fill factor. Unlike conventional detectors, typically structured as linear strip arrays (1D) or pixel matrices (2D), RSDs offer a highly flexible geometry for readout pads, allowing for optimization based on experimental demands.

When ionizing radiation interacts with these sensors, the generated charge spreads beyond adjacent pixels. This broad charge sharing, while beneficial for interpolation-based resolution enhancement, is complicated by reduced signal amplitudes and Landau fluctuations on pixels farther from the true hit location. To address these challenges, we study pixelated AC-LGADs fabricated at Brookhaven National Laboratory with different pad geometries, including square and triangular configurations with a 500 µm × 500 µm pitch, and analyze their impact on spatial resolution.

In contrast to previous studies, we leverage full-waveform information from each readout channel and utilize Recurrent Neural Networks (RNNs) to infer the full waveforms of the readout pads, given the hit's position and AC-LGAD structure, thereby reconstructing the hit position. The higher precision achieved by the classical charge-imbalance and geometry-based matrix inversion methods is leveraged by the amount of information processed by the networks, such as identifying optimal trade-offs between spatial granularity and data volume. Initial studies on Transient Current Techniques are used as inputs to further refine the algorithms with particle beams, where Landau fluctuations challenge the readout.

To support real-time applications and reduce computational load, we evaluate waveform rasterization techniques for compressing temporal signal data while preserving critical spatial information. These techniques are essential for future implementation on Field Programmable Gate Arrays (FPGAs) and other low-latency hardware platforms. Additionally, we conduct comparative studies of alternative geometric pad arrangements, assessing how shape and connectivity influence charge collection and algorithmic performance. These combined studies demonstrate the feasibility and scalability of using RSDs with flexible geometries, optimized readout configurations, and machine learning-enhanced reconstruction to meet the stringent resolution and speed requirements of next-generation high-energy physics (HEP) detectors.

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I. Presentation on scientific results

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