3rd DRD3 week on Solid State Detectors R&D



Contribution ID: 30

Type: WG5 - Characterization techniques - facilities

Advancements and future expansions of the Caribou DAQ system

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Caribou is a versatile data acquisition system used in multiple collaborative frameworks (CERN EP R&D, DRD3, AIDAinnova, Tangerine) for laboratory and test-beam qualification of novel silicon pixel detector prototypes. The system is built around a common hardware, firmware and software stack shared across different projects, thereby drastically reducing the development effort and cost. It consists of a custom Control and Readout (CaR) board and a commercial AMD Zynq System-on-Chip (SoC) platform. The SoC runs a Yocto distribution integrating the custom software framework (Peary) and custom FPGA firmware built within a common firmware infrastructure (Boreal). The CaR board provides a hardware environment providing various resources such as power supplies, slow control interfaces, and high-speed data links for the target detector prototype. Boreal and Peary, in turn, offer firmware and software environments that enable seamless integration of control and readout for new detector prototypes. Additionally, a unified testing method, integrated into the above frameworks that supports the FPGA device families in use, is currently under development. While the first version of the system used a SoC platform based on the ZC706 evaluation board, migration to Zynq UltraScale+ platforms is progressing with the finalized support of the ZCU102 board and the ultimate objective of integrating the SoC functionality directly into the CaR board, eliminating the need for separate evaluation boards. This talk describes the Caribou system, focusing on the latest project developments and showcasing progress and future plans across its hardware, firmware, and software components.

Type of presentation (in-person/online)

in-person presentation

Type of presentation (I. scientific results or II. project proposal)

I. Presentation on scientific results

Author: KAMOISIS, Ilias (CERN and Aristotle University of Thessaloniki (GR))

Co-authors: DANNHEIM, Dominik (CERN); BUSCHMANN, Eric (Brookhaven National Laboratory (US)); CHEN, Hucheng (Brookhaven National Laboratory (US)); BENOIT, Mathieu (Oak Ridge National Laboratory (ORNL)); ST--JEAN, Ryan (Carleton University (CA)); TANG, Shaochun (Brookhaven National Laboratory (US)); SPANNAGEL, Simon (Deutsches Elektronen-Synchrotron (DE)); KOFFAS, Thomas (Carleton University (CA)); VANAT, Tomas (Deutsches Elektronen-Synchrotron (DE)); OTARID, Younes (CERN)

Presenter: KAMOISIS, Ilias (CERN and Aristotle University of Thessaloniki (GR))

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