Contribution ID: **58** Type: **WG1 - Monolithic Sensors**

Design and characterization of CASSIA monolithic pixel sensors with gain

Tuesday 3 June 2025 10:00 (20 minutes)

The CASSIA (CMOS Active SenSor with Internal Amplification) project is focused on developing monolithic active pixel sensors (MAPS) with internal signal gain in a commercial CMOS technology. The advantages of this approach include a higher input signal enabling simplification of in-pixel electronics, an improved signal-to-noise ratio for radiation hardness, and superior timing resolution for future 4D tracking applications. Initial prototype sensors (CASSIA1) were fabricated to demonstrate the feasibility of implementing a gain layer in the Tower Semiconductor 180 nm CIS process. Current developments are focused on the design of a new sensor prototype (CASSIA2), which implements the sensor structures with gain alongside in-pixel electronics to operate the sensors either in low-gain (LGAD) or high-gain (SPAD) mode.

The presentation will give an overview of the latest measurement results on CASSIA1, including measurements of sensor response to DC and pulsed laser sources, as well as in-pixel gain scans of various sensor implementations. The talk will also describe the designs featured on the CASSIA2 prototype, including the in-pixel front-end amplifier used for LGAD-mode operation, several types of quenching circuits used for SPAD-mode operation, as well as a simple digital readout architecture used to obtain pixel address information from small-scale matrices.

Type of presentation (in-person/online)

in-person presentation

Type of presentation (I. scientific results or II. project proposal)

I. Presentation on scientific results

Authors: KOTSOKECHAGIA, Anastasia (CERN); Mr POŽAR, Borna; SOLANS SANCHEZ, Carlos (CERN); PERNEGGER, Heinz (CERN); BERDALOVIC, Ivan; LUNDE, Jenny (University of Oslo (NO)); Mr JUGOVIC, Matija (University of Zagreb - FER); BARTULOVIĆ, Paula; HABERL, Sebastian (University of Innsbruck (AT)); SULIGOJ, Tomislav (University of Zagreb - FER)

Presenters: BERDALOVIC, Ivan; SULIGOJ, Tomislav (University of Zagreb - FER)

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