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Conceptual Basis for Canadian Participation in the MALTA Project: toward a Design and Verification Strategy

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A consortium of Canadian researchers from Carleton and Waterloo Universities has joined the CERN-led MALTA project, a CMOS MAPS project fabricated in the 180nm TowerJazz technology node. We expect that Canadian expertise in analog mixed-signal design, Radiation Hardening by Design (RHBD) and algorithmic error correction for hardware implementation will be particularly valuable in advancing the previous MALTA design in 65 nm CMOS technology. We aim to use design concepts enhancing timing resolution, speed, radiation resilience and power consumption. There are two focus areas:

1. Focus area 1: Optimization of the analog front-end (AFE) for improved timing resolution, noise performance, power efficiency and enhanced radiation resilience.
2. Focus area 2: Optimization of the digital periphery for higher bandwidth and scalability to larger pixel arrays with radiation hardened by design (RBHD) registers and memories.

For the AFE optimization we propose to introduce amplifier topologies such as the folded cascode front-end taking full advantage of feature sizes and lower nominal voltage supply of 65 nm CMOS. We propose to improve the AFE performance by implementing pixel threshold equalization. The 65nm process enables calibration circuitry to be embedded within each pixel without violating area constraints. A complementary step is the development of on-chip architectures for detecting and flagging bad or noisy pixels during operation.

In the digital periphery, the aim is to simplify the integration of the MALTA chip into larger detector systems by introducing the concept of chip-to-chip serial transfer as has already been envisioned by earlier MALTA designers. In parallel, we aim to ensure reliable, high-speed operation of essential digital components (SRAM, FIFO buffers, Flip-Flops) within the MALTA sensor under significant radiation exposure. This can be achieved by implementing RHBD memory and logic cells, e.g. interlocked cell designs (DICE –Dual Interlocked Cell) optimized for power efficiency. Furthermore, by implementing Error Correcting Codes (ECC) particularly for on-chip memories (SRAM, FIFOs) one can also detect and correct radiation-induced changes of state (bit-flips) in digital memory elements.

We will present in some detail the above ideas while justifying the move to the 65nm technology mode. Where possible, experience gained from previous applications will be provided. To ensure robust performance, we will present a preliminary integration and verification strategy encompassing block-level and system-level aspects of the proposed design, while acknowledging potential challenges.

Type of presentation (in-person/online)

online presentation (zoom)

Type of presentation (I. scientific results or II. project proposal)

III. other (please specify)

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