SiC PIN Update

Jiaqi Zhou[2], Sen Zhao[1],Xiyuan Zhang[1],Xin Shi[1]

1. Institute of High Energy Physics, CAS
2. Jilin University

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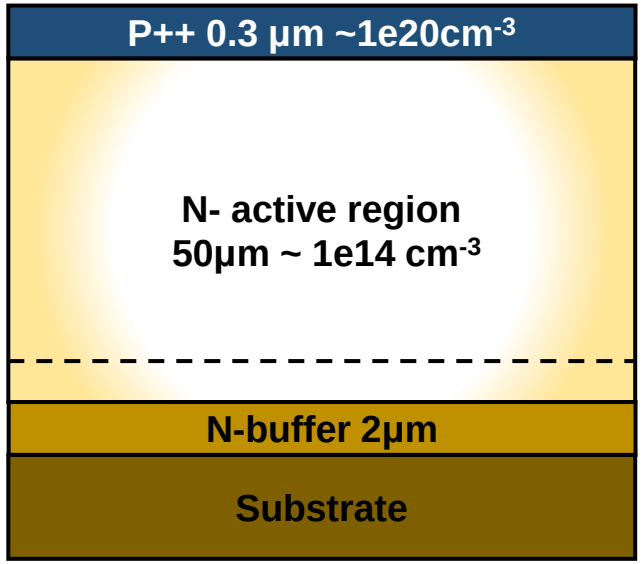
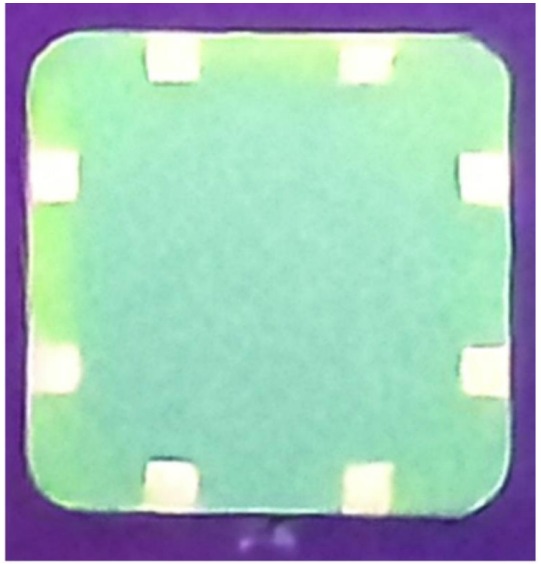
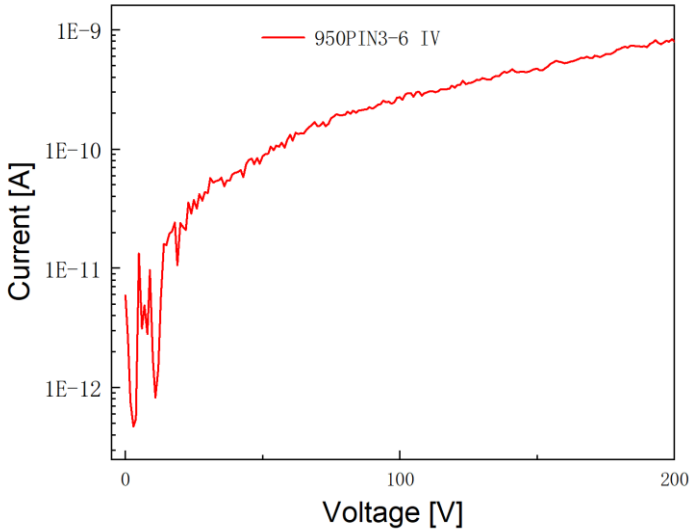
IHEP 4H-SiC-PIN devices status

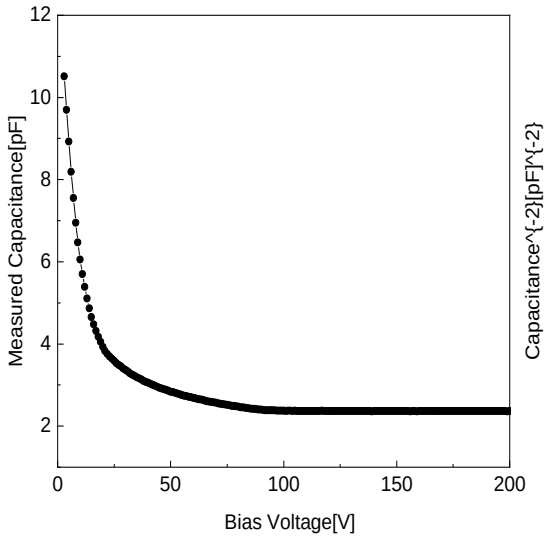
- 4H-SiC PIN Diodes
- Full depletion voltage ~ 96V
- The doping concentration ~ 1.44e14 cm^{-3}
- The full depletion depth reaches ~ 27μm
  - The actual active region is only eighty percent of the theoretical value, which is 40 μm

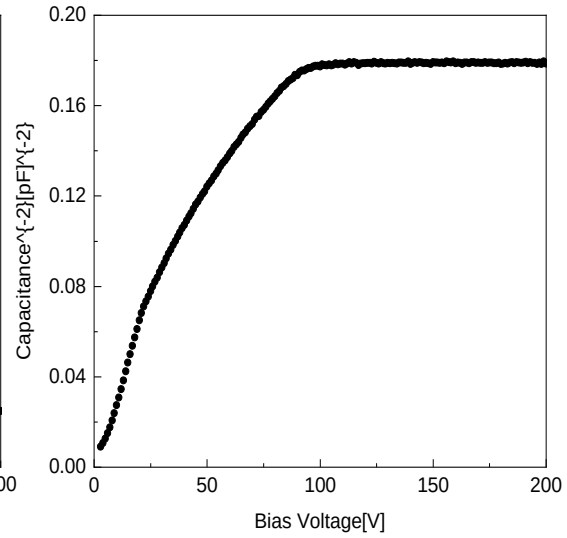
PIN epitaxial structure





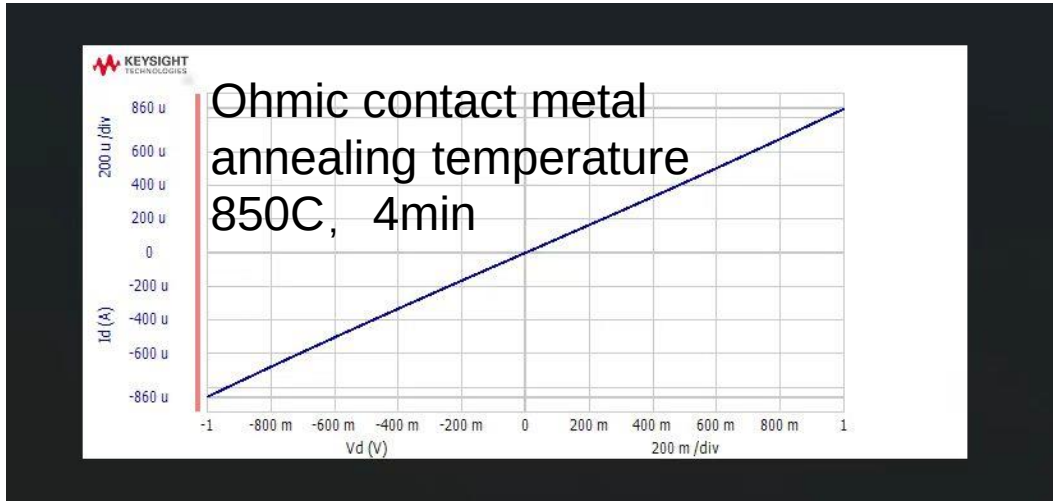


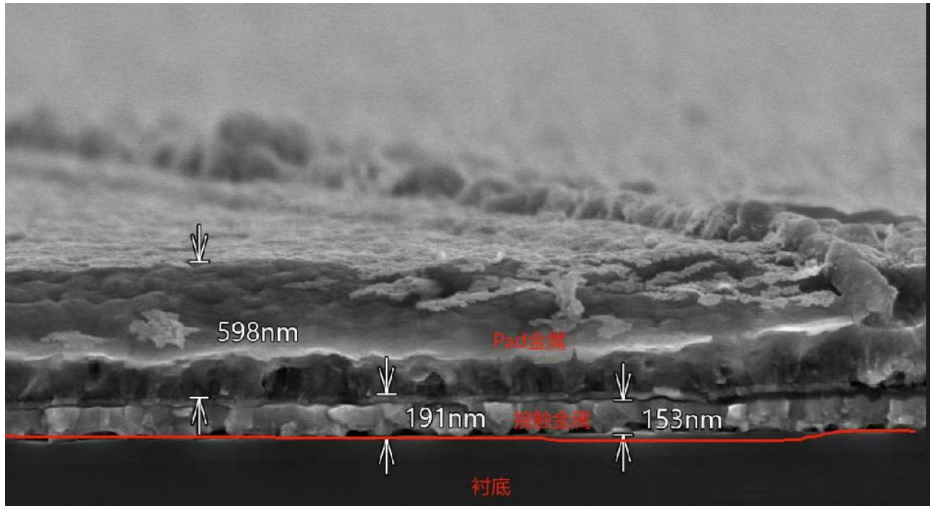




IHEP 4H-SiC-PIN devices status

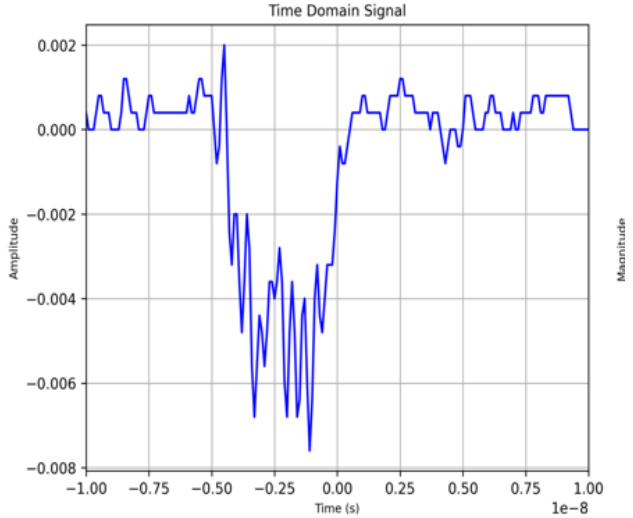
- P-type Ohmic contact not very well
  - Poor contact between the SiC and metal
- Should optimize the Ohmic process



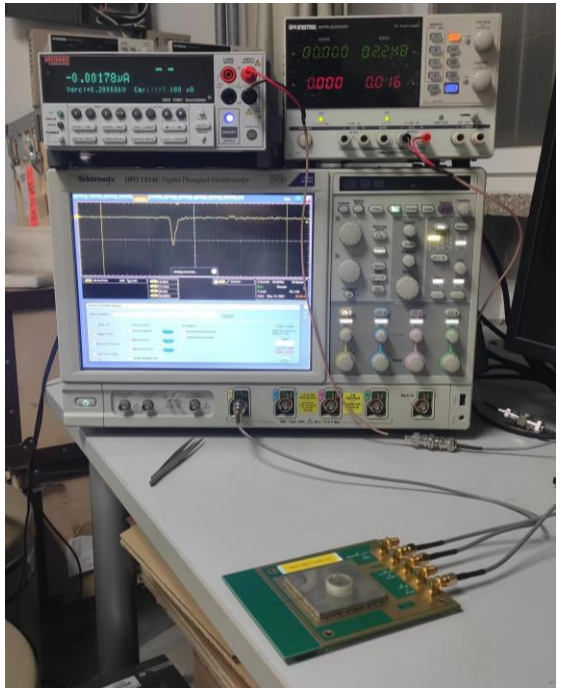


IHEP 4H-SiC-PIN devices status

- **Charge collection （alpha）**
- **Single test board —— UCSC**

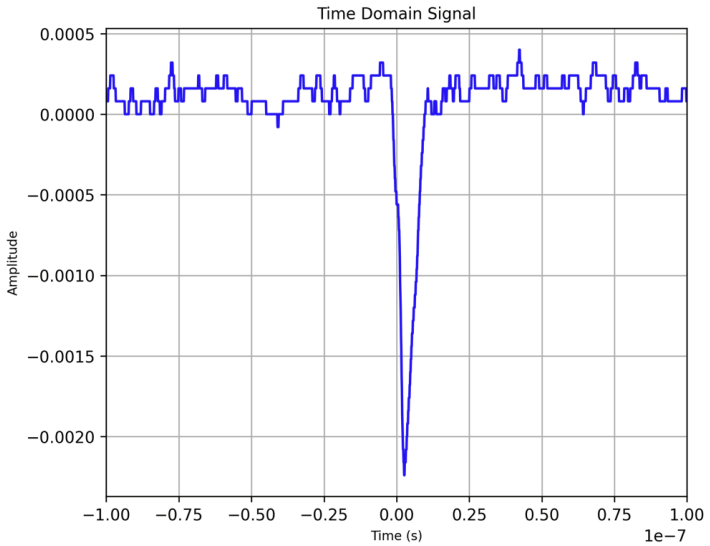


300V



sampling rate is 100 ps/pt
bandwidth is 2 GHZ

When the bandwidth is large, the oscillation is severe, making accurate sampling impossible



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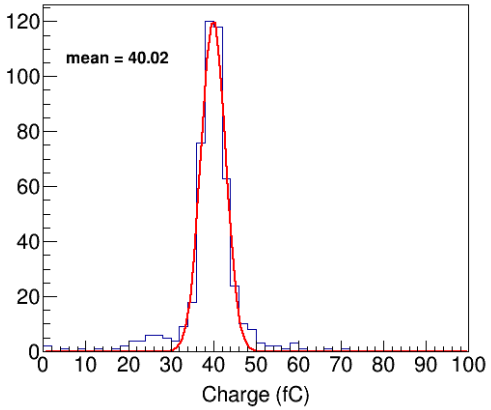
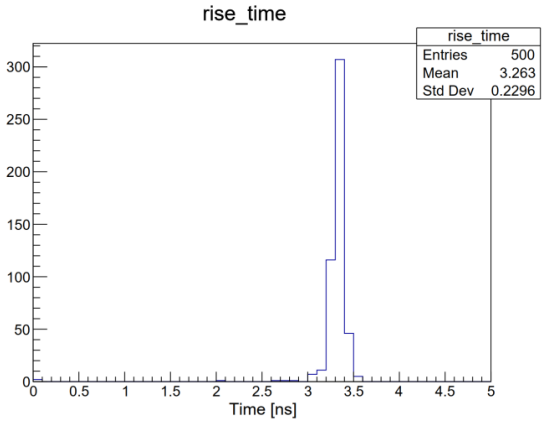


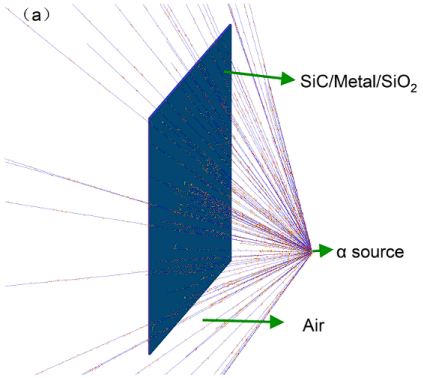


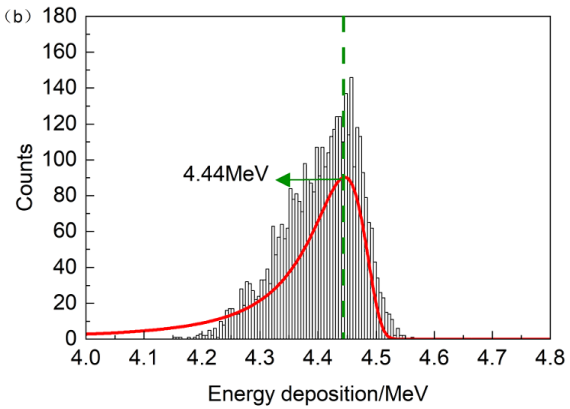
When the bandwith is 2 MHZ

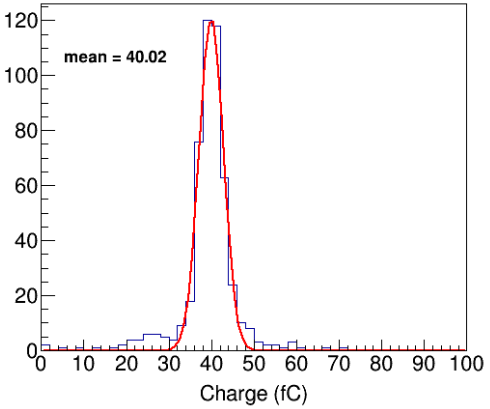
- The charge collection is around 40 fC.
- The rising time is around 3.2 ns.

IHEP 4H-SiC-PIN devices status

- **Charge collection （alpha)**







- The 5.4MeV alpha particle injection process was simulated by Geant4. Tolal energy deposition is 4.4 MeV.
- It is reported that the SiC needs around 9 eV to generate one electron-hole pair.

→ The charge collection should be

$$\frac{4.4\text{Mev}\times 1.6\times 10^{-19}}{9\text{ev}} = 80\text{fc}$$

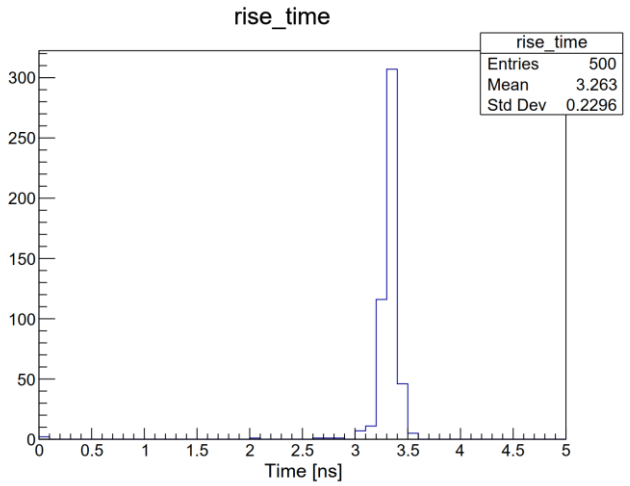
- We suppose that 40 fc is based on low bandwidth, which may have resulted in the loss of high-frequency signals,The signals obtained are all low-frequency signals.
- Other possible is that due to surface trapping and non-ionizing energy loss in the device, a portion of the charge will be lost. However, is 50% reasonable?

IHEP 4H-SiC-PIN devices status

The full depletion depth reaches ~ 27μm

- **Rising time （alpha)**

Characteristic	Si	4H-SiC
Eg (eV)	1.12	3.26
Thermal conductivity	1.5	4.9
$E_{breakdown}$ (V/cm)	0.5	3
Saturated electron velocity (cm/s)	1×10^7	2×10^7
ionization energy for e-h pair (eV)	3.64	7.8
displacement energy	13	21.8



- The rising time should be $\frac{27\text{um}}{2\times10^7\text{cm/s}} \approx 135\text{ps}$
- The rising time ~ **3.2 ns**.

The measured value of the rising time differs from the theoretical value by an order of magnitude.

Question

- We gauss that the filtering and amplification factors of the UCSC circuit board made in China have not reached the ideal values
- Is the bandwidth of the circuit board insufficient, and can optimizing the circuit board solve these two issues?

IHEP 4H-SiC-PIN devices status

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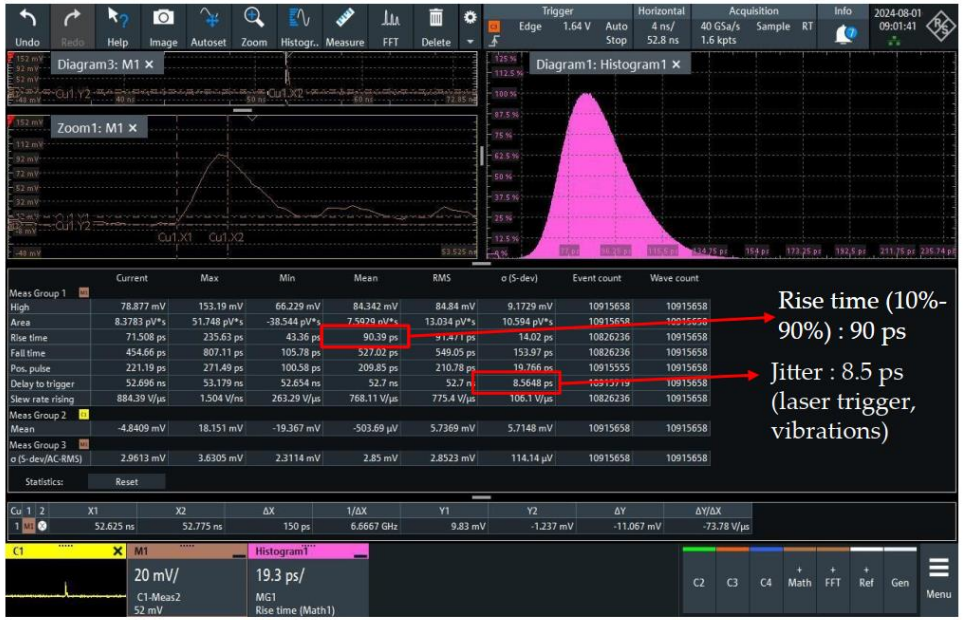
UCSC Board Tests

- UCSC board with feedback $R_{14} = 82\ \Omega$
- 4H-SiC detector with C_{det} = 0.5 pF, UV-TCT with ~3 ps jitter
- Achieved 90 ps risetime!
- Eqv. BW = 3.9 GHz
- However, oscillations in signal, esp. for $R_{14} < 82\ \Omega$
- Would need a more HF adequate design and HF resistors



1/(2 * pi * 0.5 pF * 82 Ohm) = 3.88 GHz

Andreas Gsponer WG6-SiC-LGAD Readout Discussion 14

In WG6-SiC-LGAD Readout Discussion,We observed that Andreas Gsponer in HEPHY increased the feedback resistor, which enhanced the gain, contrary to our previous simulation results. What could be the reason for this?

Plan and Request

Amplifier board request

Compared to Si, SiC faster saturated electron velocity and smaller signal

- **Single test board and Multichannel test** board for **DC/AC-coupled** SiC device (PIN/LGAD)
- <300 ps rising time
- 2 GHz, 22 dB
  - may improve?
- We need higher filtering requirements
- We need higher magnification requirements

- Plan to product a new batch PIN device…
- Could you send us a test board? If that's not possible, may we send our samples to you?