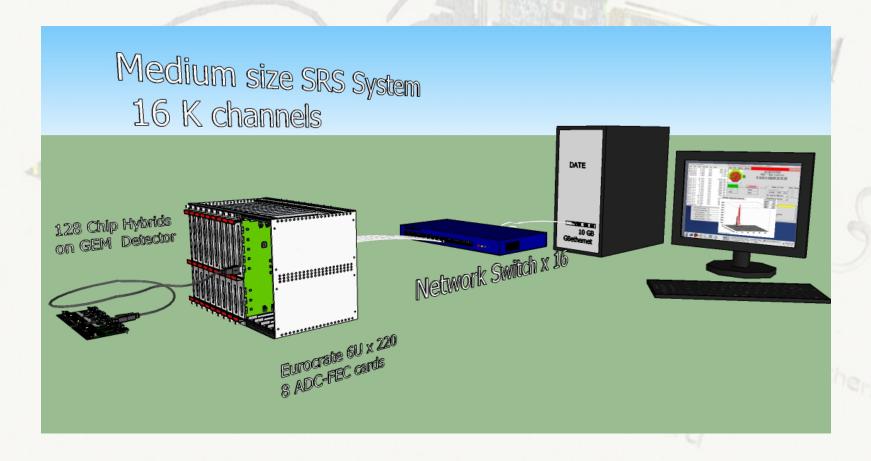
# SRS target by end 2010: 16 k channel system



### Frontend hybrids

so far all based on APV25 chip

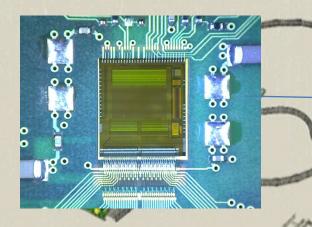
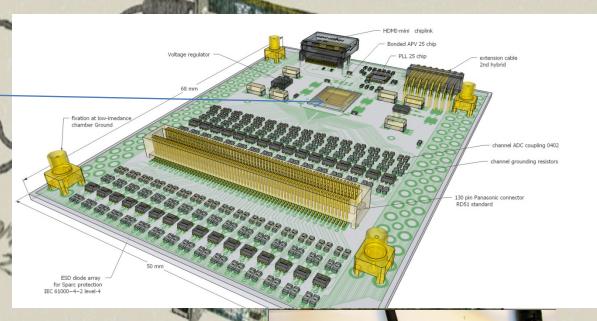


Photo of wire-bonded APV on RD51 hybrid Version 3



Version 1 proto: 5 working ones

Version 2 users: 11

Version 3 systems: 15 (CERN: Rui + bonding service)

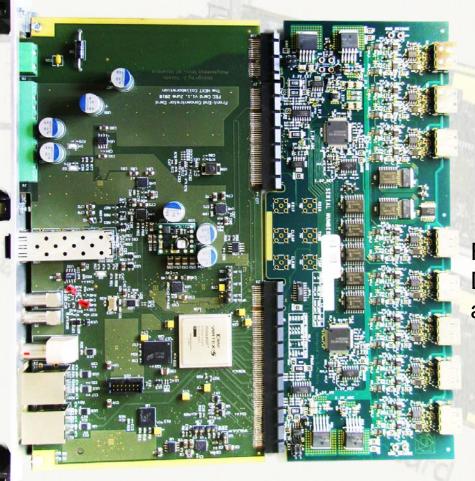
292 (ELTOS + Hybrid SA) under production this week



### FEC and ADC adapter assembly

FEC card designed @UPV-Valencia by J.Toledo

Firmware:
Gigabit ethernet
Alfonso Tarazona



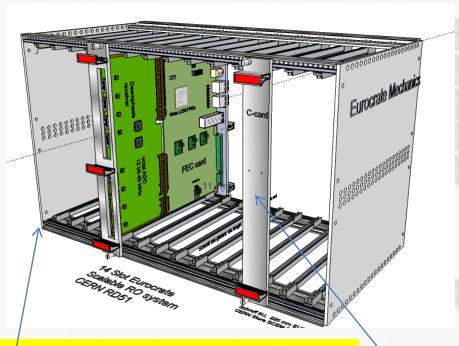
Octal ADC card designed@cern by S.Martoiu

Firmware:
Data processing
and buffering
S.Martoiu

1st GO: fit together and work

minor modifications for volume production

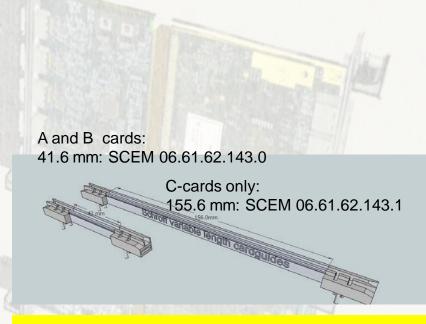
### Eurochassis 6U x 220



<u>Chassis:</u> 6U x 220 mm, CERN SCEM 06.61.61.045.7 Fabricant ATOS http://www.atos-racks.com

#### **C-cards and FEC cards:**

Front panel set 6U-6TE with fixations: CERN SCEM 06.61.63.156.3

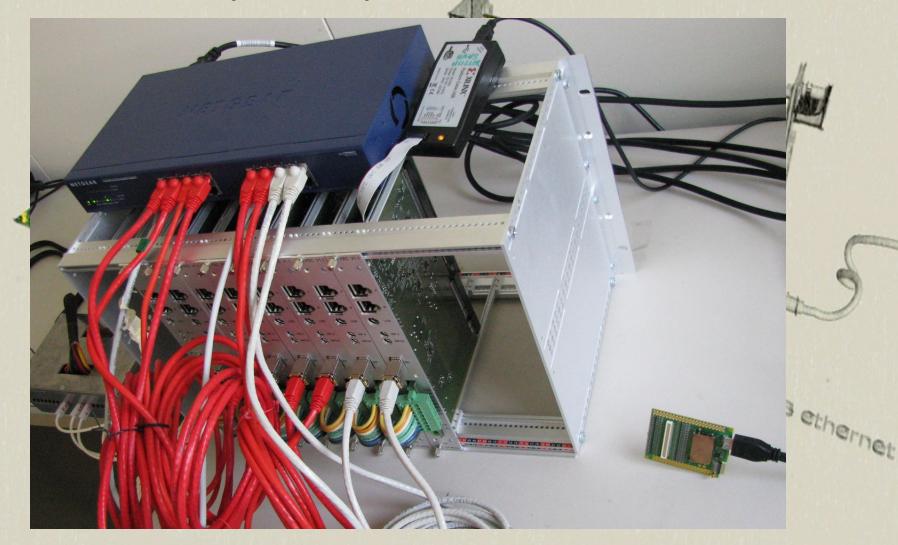


Card guides for SRS CERN store:

#### **A-cards and B-cards**

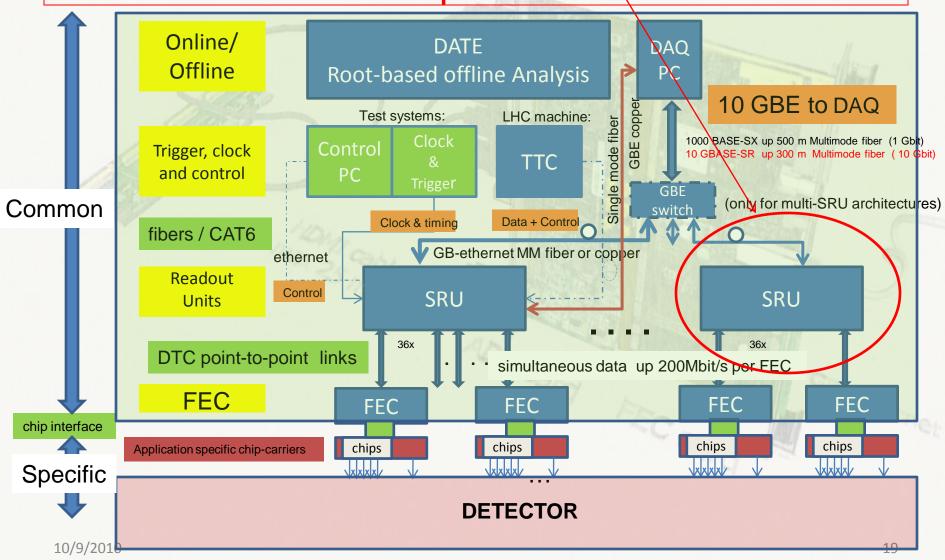
Front panel set 3U-6TE with fixations: CERN SCEM 06.61.63.056.6

# Online(DATE) via 8xGbE Switch



### Scalable architecture > 16 k channels

→ requires SRU



## About chip candidates for SRS

SRS was designed to allow choice of frontend chip

the optimal chip interface is serial (analogue or digital)

RD51 maintains a chip matrix under <a href="https://espace.cern.ch/rd51-wg5/chipmatrix/default.aspx">https://espace.cern.ch/rd51-wg5/chipmatrix/default.aspx</a> please tell us if you want to add a chip to the knowledgebase popular chip candidates: APV25, Beetle, VFAT, AFTER

The first SRS chip adapter implementation was made this year for the APV25 (+Beetle)

VFAT is on hold until it becomes available (
AFTER and NX-YTER would require some team to build the adapter
Adapter for BNL chip was started by ATLAS/Univ. O. Arizona
Adapters for emerging chips, MICROROC, Medipix are considered

More chips possible, their integration in SRS is user-driven

### SRU -2010

