Timepix readout

A readout system for the Timepix chip

M. Lupberger, J. Kaminski

University of Bonn

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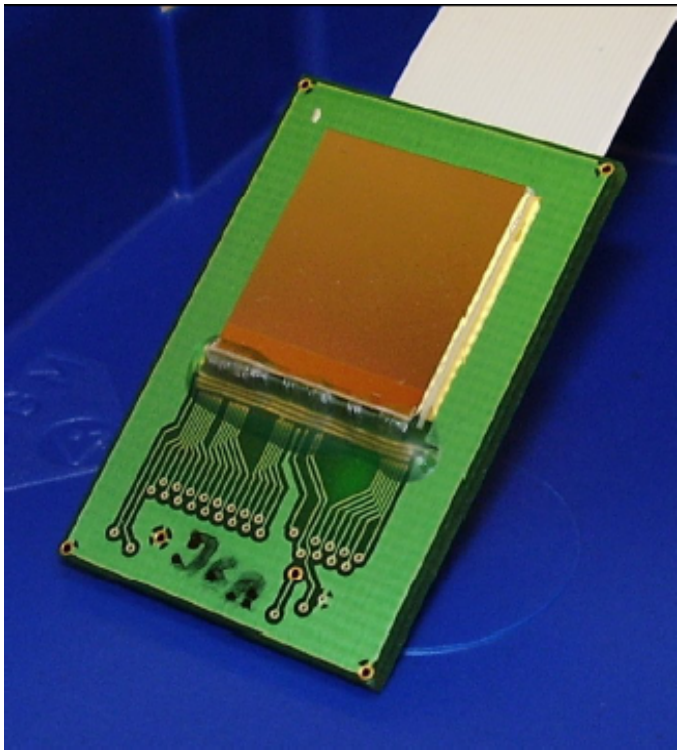
Timepix

Timepix chip derived from MediPix-2

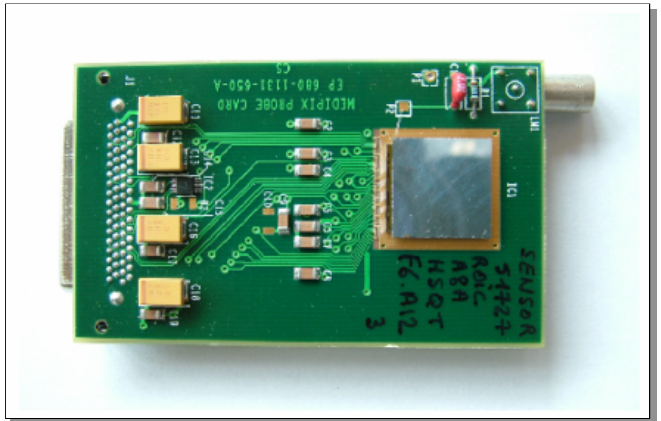


Size of matrix: 256 × 256 pixels
Pixel size: 55 × 55 μm²
Chip dimensions: 1.4 × 1.4 cm²

Each pixel can be set to one of these modes:

- TOT = time over threshold
  gives integrated charge
- Time between hit and shutter end

- CMOS 250 nm technology, IBM
- amplifier (t_{rise} ~150 ns)
- 14 bit counter
- clock every pixel up to 200 MHz



MUROS readout system

MUROS v2.1:

- successor of MUROS v1 (only Medipix1 chip)
- designed at NIKHEF for Medipix2 and Timepix chip readout (new FPGA code)

- serial readout for at most 8 Timepix chips
- VHDCI cable <3 m to Timepix carrier board
- VHDCI cable to NI card in PC
- Timepix readout: theo. < 50 frames/sec
  lowered by shutter length
- adjustable readout frequency [<240MHz

Unfortunately, out of production.

Alternatives:

USB -device

Relaxed

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New readout system

Goals:

- ultimately read out ~100 chips
  → large area detector (e.g. full TPC endplate module)
- modular system → use SRS (RD51)
- ethernet based
- use Virtex6 FPGA
- zero suppression
- triggerable, integrate with slow control & calibration
- keep Timepix-3 compatibility in sight

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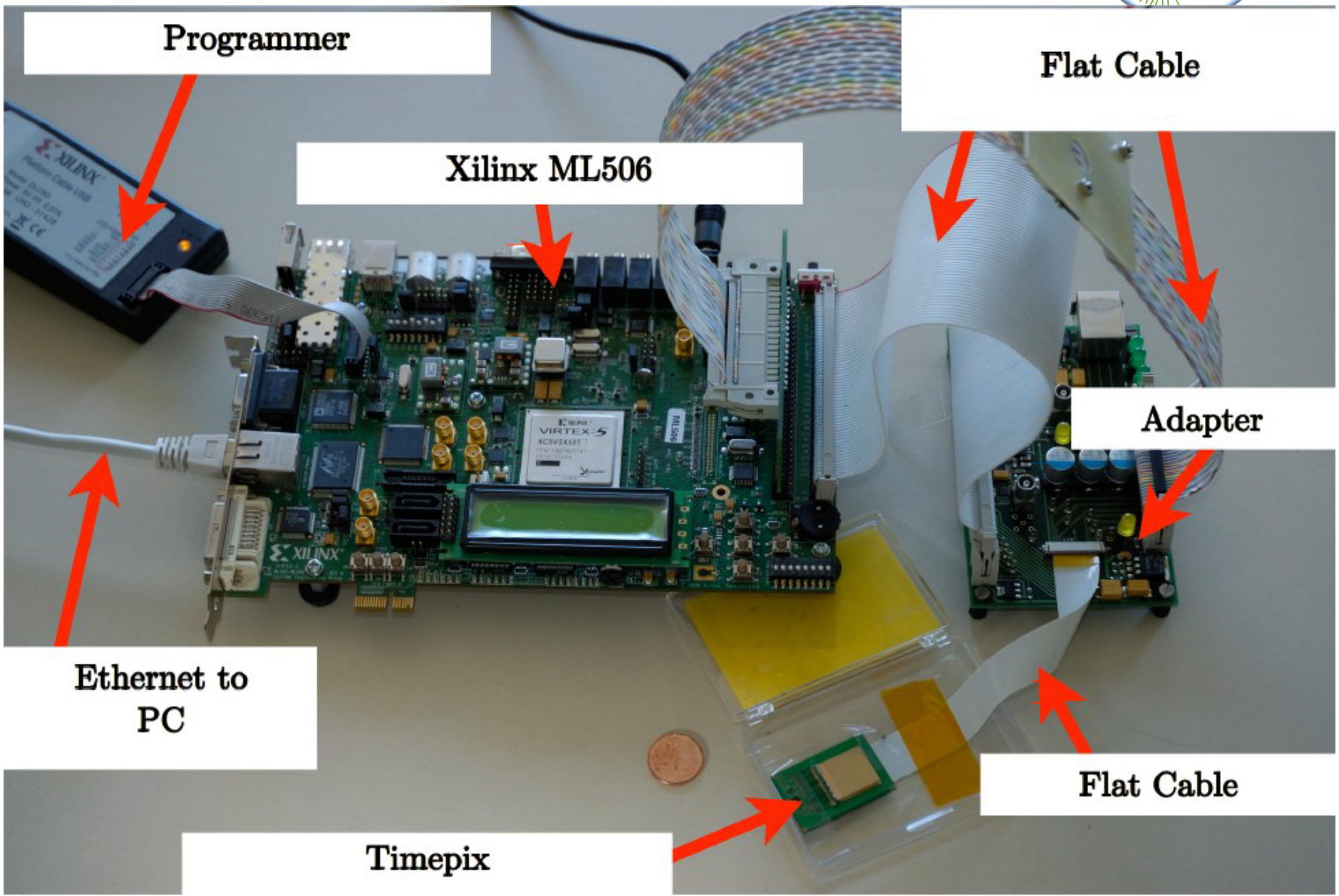
Mainz readout system



Software

FPGA

- On-chip Ethernet MAC
- On-board Gigabit Ethernet phy chip
  - 1000BASE-T
  - no embedded CPU
- Firmware (VHDL)
  - common clock for digitization and data transfer, crystal based
  - serial/deserial interface to the Timepix bit-serial port
  - Timepix matrix data not buffered in FPGA
    → kept on Timepix while awaiting packet transmission
  - shutter with programmable delay and width (external/software control)
  - non-volatile storage of hardware description on CF card

PC Software: in C++

- Functionality:
  - reset, setup (Timepix mode, matrix mask, DAC settings)
    shutter, readout, test pulse enable, choose trigger
  - start a run: set FSR, set matrix, readout matrix setup, DAQ

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Bonn activities so far:

- Setup of second Mainz system in Bonn
- Re-target to Virtex6
  - Xilinx ML605 board with Virtex6 FPGA
  - firmware modifications to Virtex5 VHDL
    - new ethernet MAC
    - adapt to different clock and pin setup
    - implement Timepix control modules
    - solve timing problems
  - hardware modifications
    - new adapter board for cabling
- Implement new features: at the moment: zero suppression

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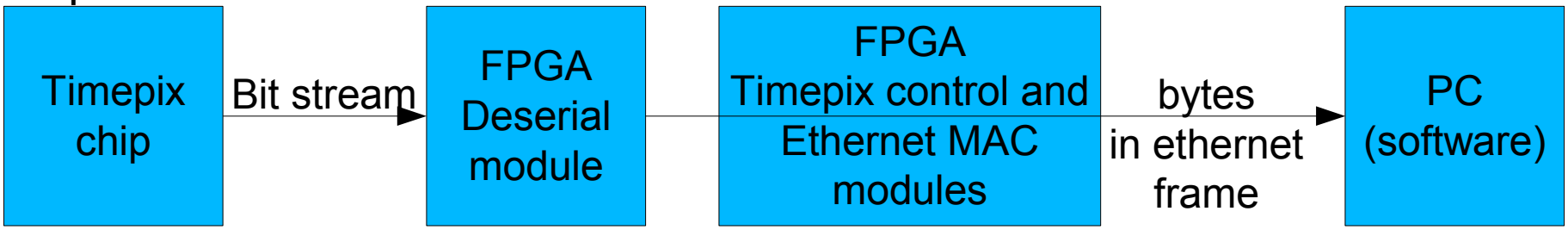
Current activities:

New readout procedure:

Aim: Zero suppression, lower data volume, higher readout rate

Old procedure:



Only pipeline data: Convert bit stream to bytes for ethernet

- PC software receives data from Chip (in byte packets)
- Sort data stream (x,y, bit position of counter of pixel(x,y))
- Get **pseudo random counter value** (x,y) and convert to **real counter value** using Lookup table
- Generate Matrix

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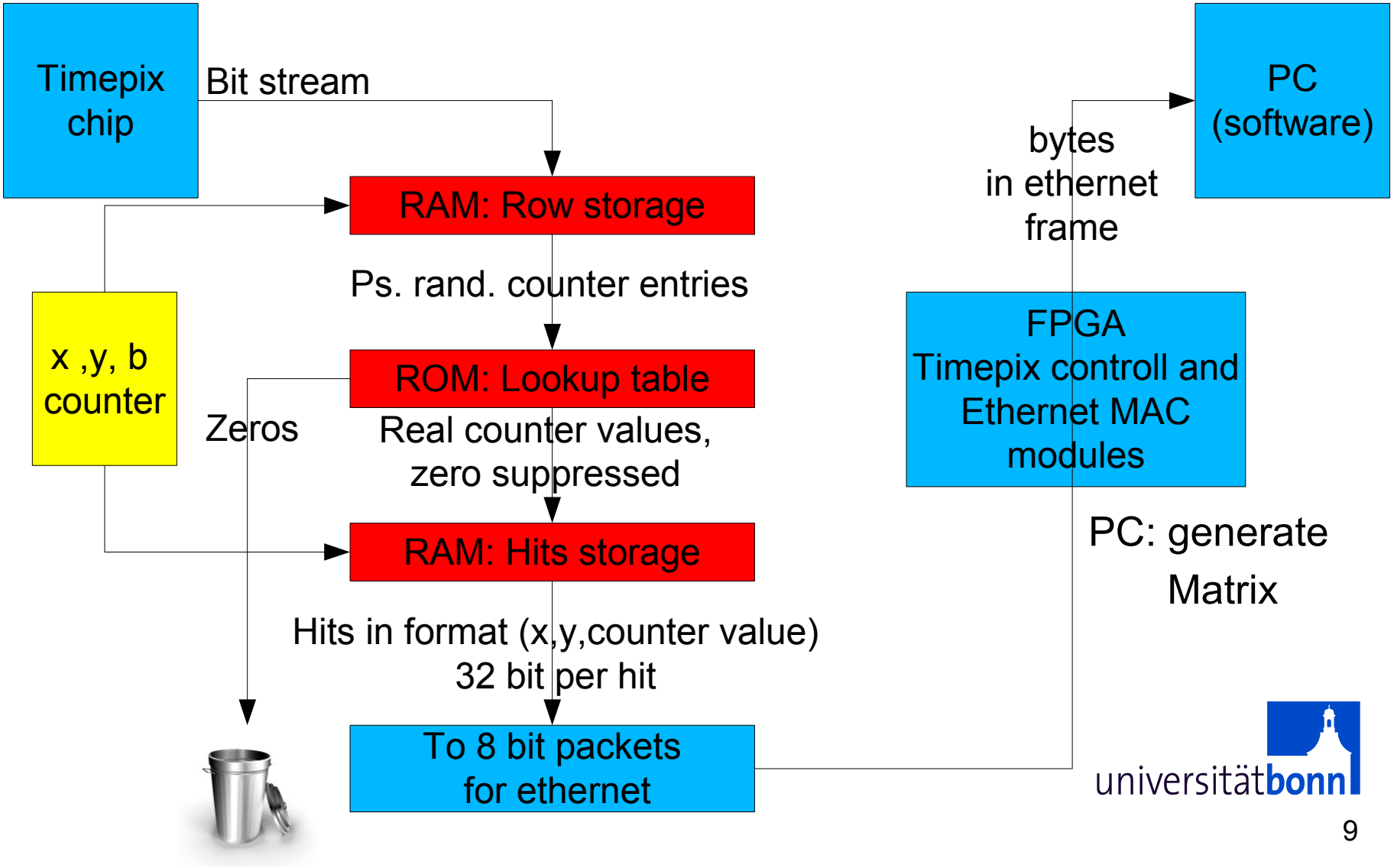
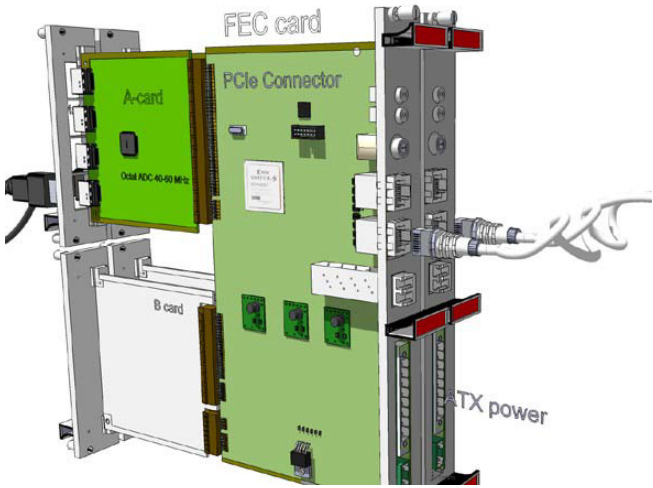
Current activities:

New procedure (additional):



Our way to go

- Advancement of PC software (Mainz)
- Multi chip (first step: 4 or 8) readout with Virtex6 (Bonn)
  or – more likely - build chip module for SRS
- Modular system: Scalable Readout System SRS:
  - small set of modular components
  - performance at low cost
  - designed for scalability
    (e.g. 1 FEC for 8 chips x
    14 FEC/crate = 112 chips)
  - plugin-choice of frontend ASICs
  - open developer platform for physics algorithms
  - supported software made for physics
  - Developed at CERN for RD51



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Summery

Timepix chip (single, quad, octo) is used as readout structure in gaseous detector (prototypes)

- Current readout systems can handle up to 8 chips
- Largest area covered: 2.8 x 5.6 cm²
- New readout system under development
  - single chip readout realized
  - hardware description for Virtex6 FPGA
  - FPGA zero suppression almost realized
  - a scalable readout system to handle ~100 chips is aimed for
  - Readout for large area gaseous detector

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