Front End IC for the ATLAS Muon Upgrade, A Status Report

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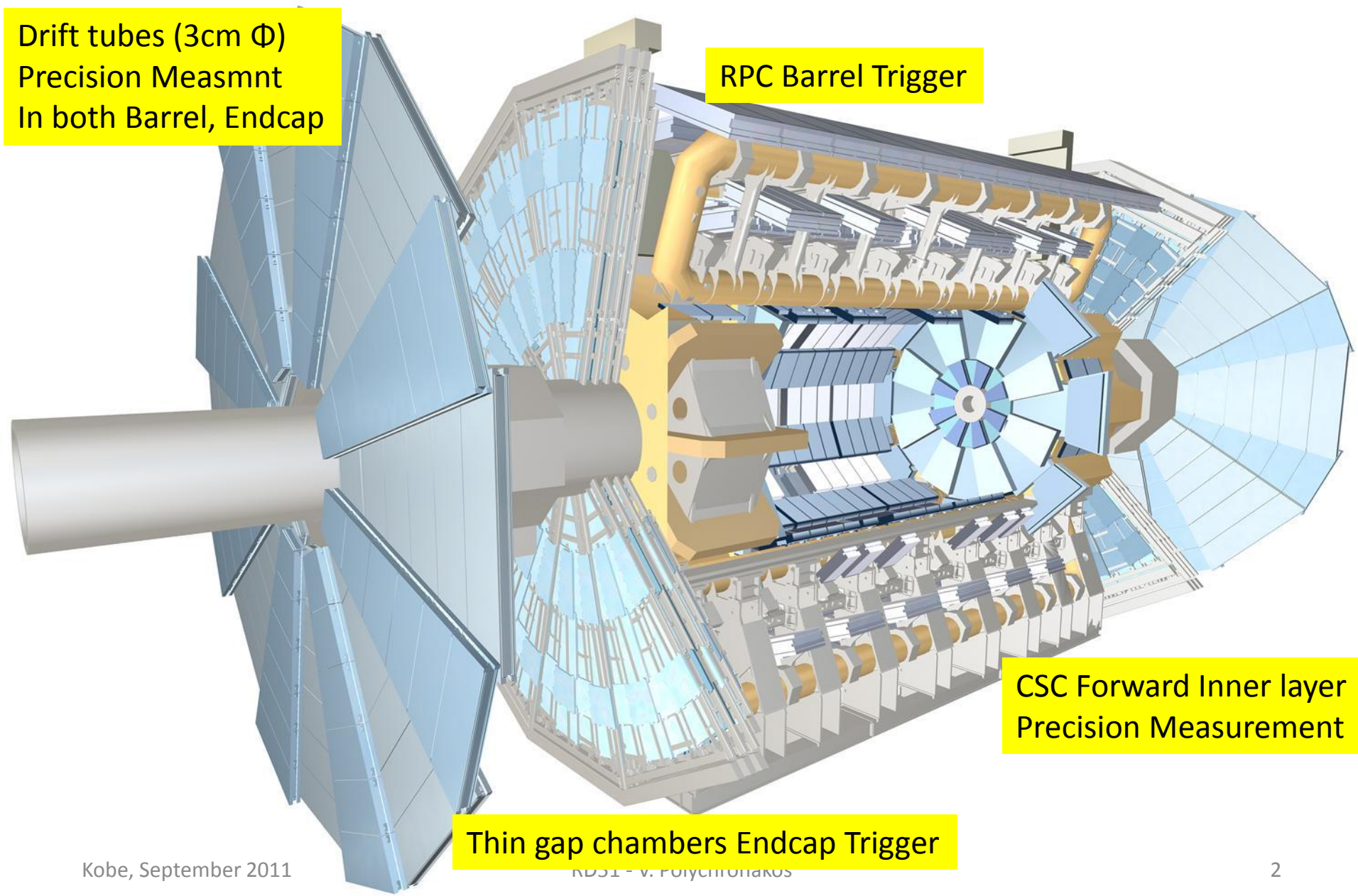
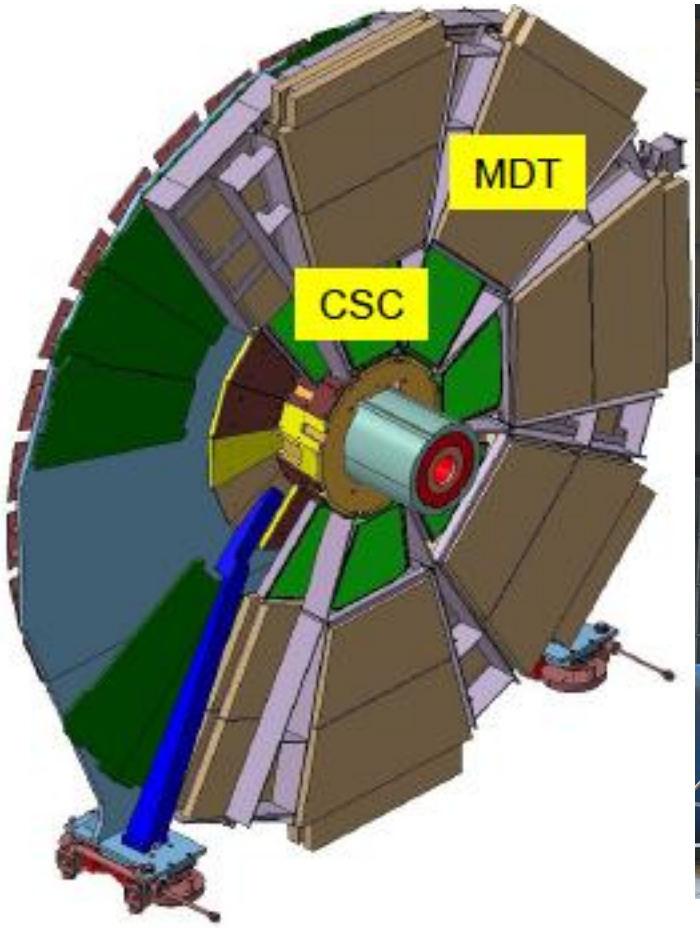
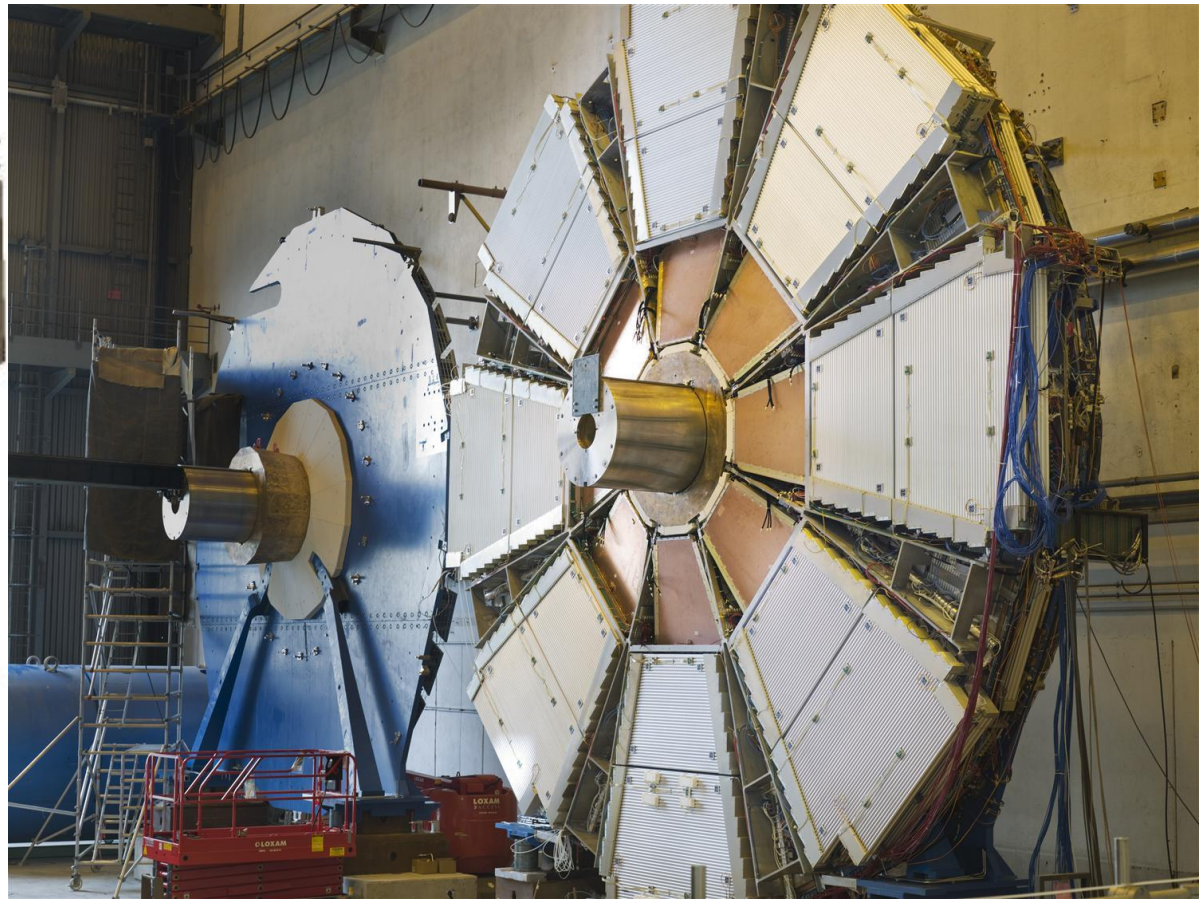
Kobe, September, 2011

The ATLAS Muon Spectrometer



The Present "Small Wheels" (9m Diameter)



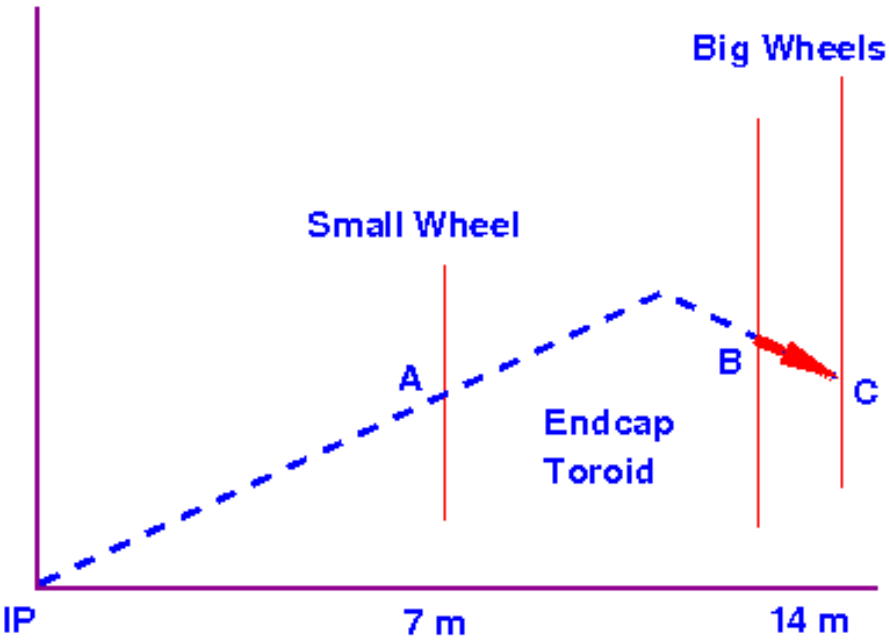


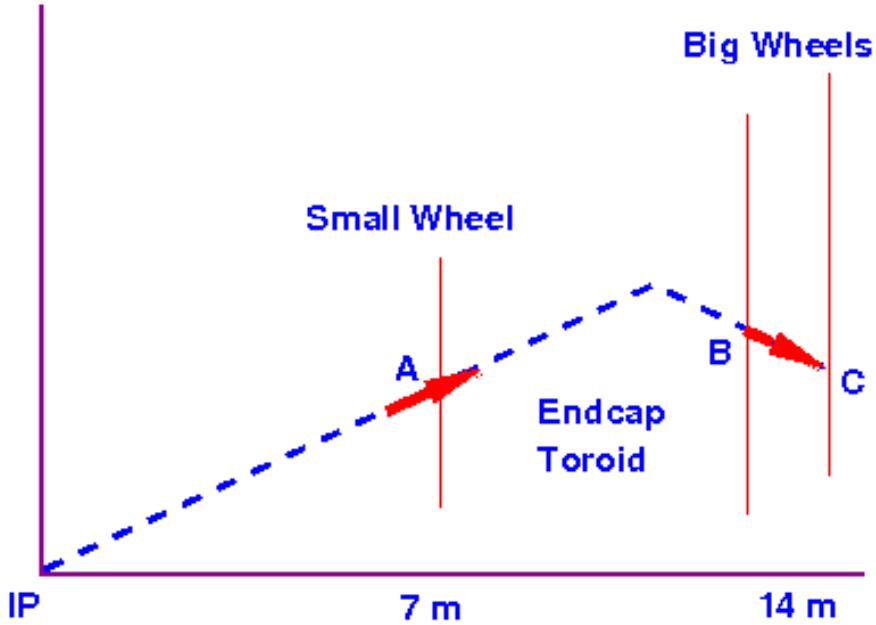
- Need New Detectors that participate in the Level1 Trigger by providing a vector with ~1 mrad resolution
- Need to handle considerably higher rates at L = 5x10e34

Three reasons for the New Small Wheels (in order of increasing importance)

- Complete Original Scope in CSC Area, add more layers. Alll detectors in SW expected to be at their Rate Limit
  - Very weak, doubt it could convince Reviewers
- Improve Pt resolution to sharpen thresholds
  - Requires 1 mrad pointing resolution for a ~20% gain which quickly disappears if resolution ~1.5-2 mrad
- Eliminate Fakes in Pt>20 GeV Triggers
  - Serious issue, Higher Luminosity Physics MUST use Pt thresholds 20-25 GeV. Currently over 90% of high Pt triggers are fake

The Problem with High pT Triggers



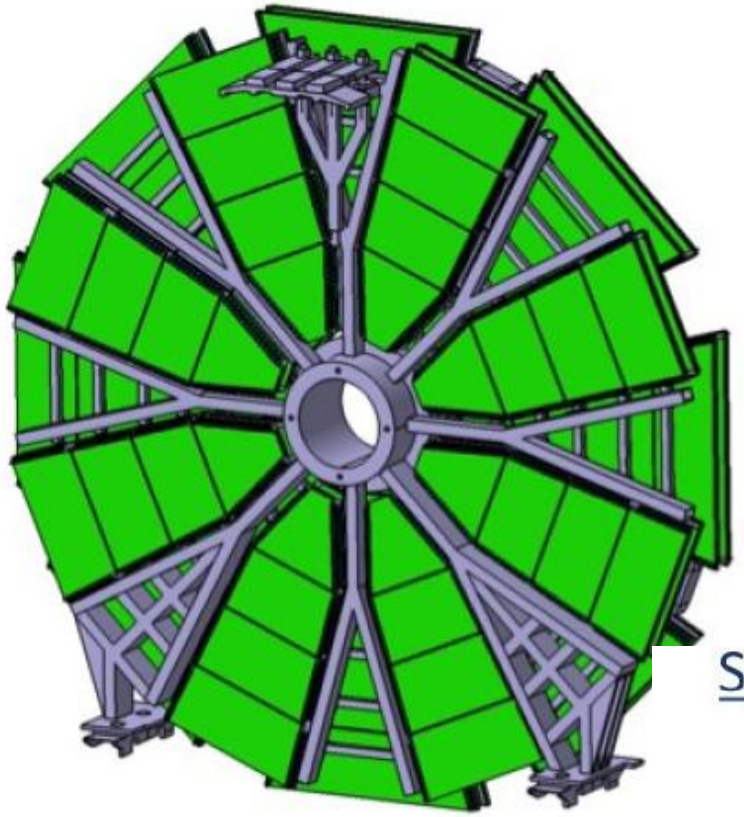


Current Endcap Trigger

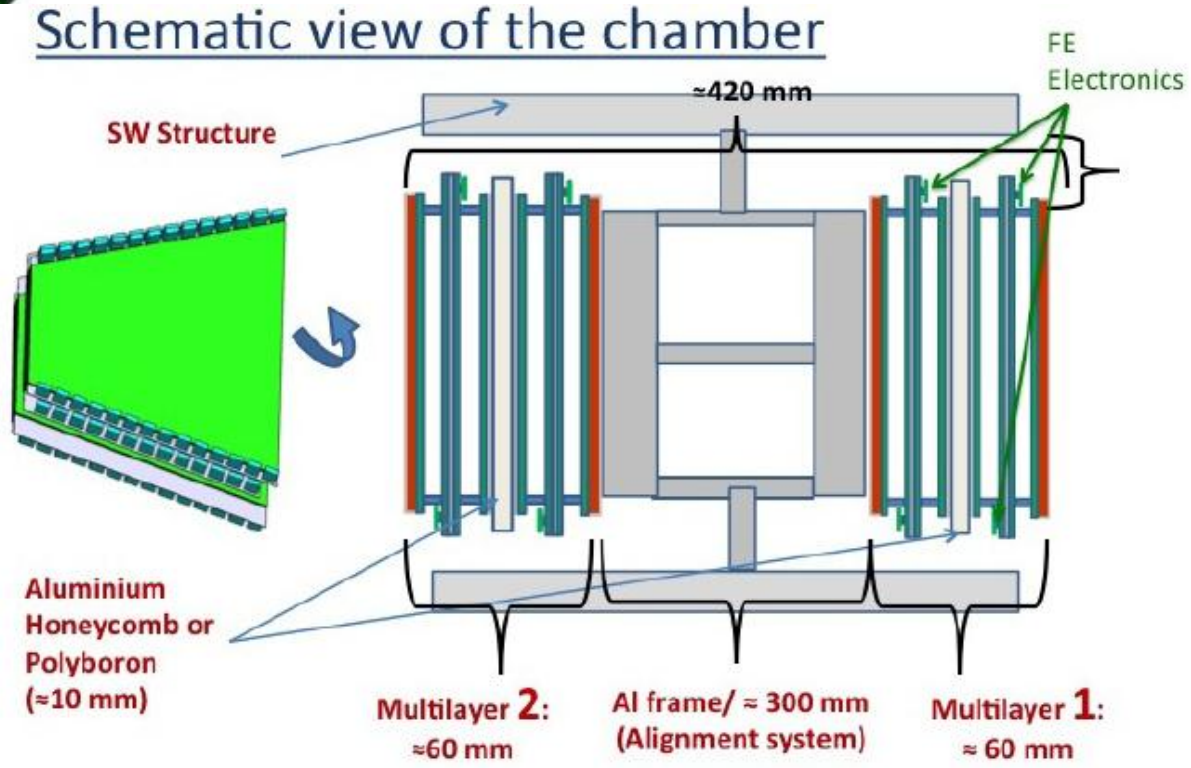
- Only a vector BC at the Big Wheels is measured
- Momentum defined by implicit assumption that track originated at IP
- Random background tracks can easily fake this

ProposedTrigger

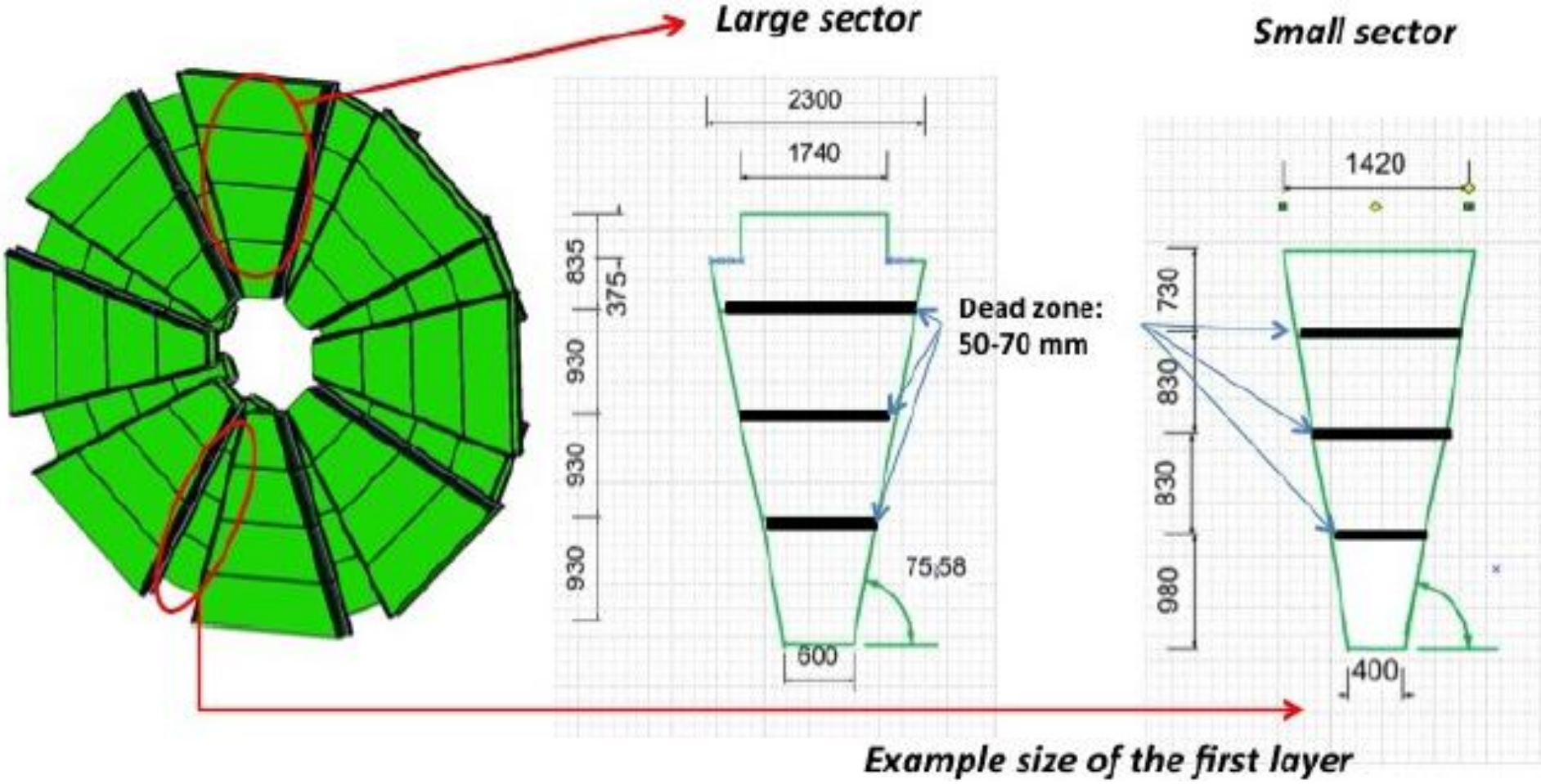
- Provide vector A at Small Wheel
- Powerful constraint for real tracks
- With pointing resolution of 1 mrad it will also improve pT resolution
- Currently 96% of High pT triggers have no track associated with them



A tentative Layout of the New Small Wheels and a sketch of an 8-layer Chamber built of 2 4-layer multilayers separated by an instrumented Al spacer for monitoring in-plane alignment



A possible segmentation of Large and Small Sectors

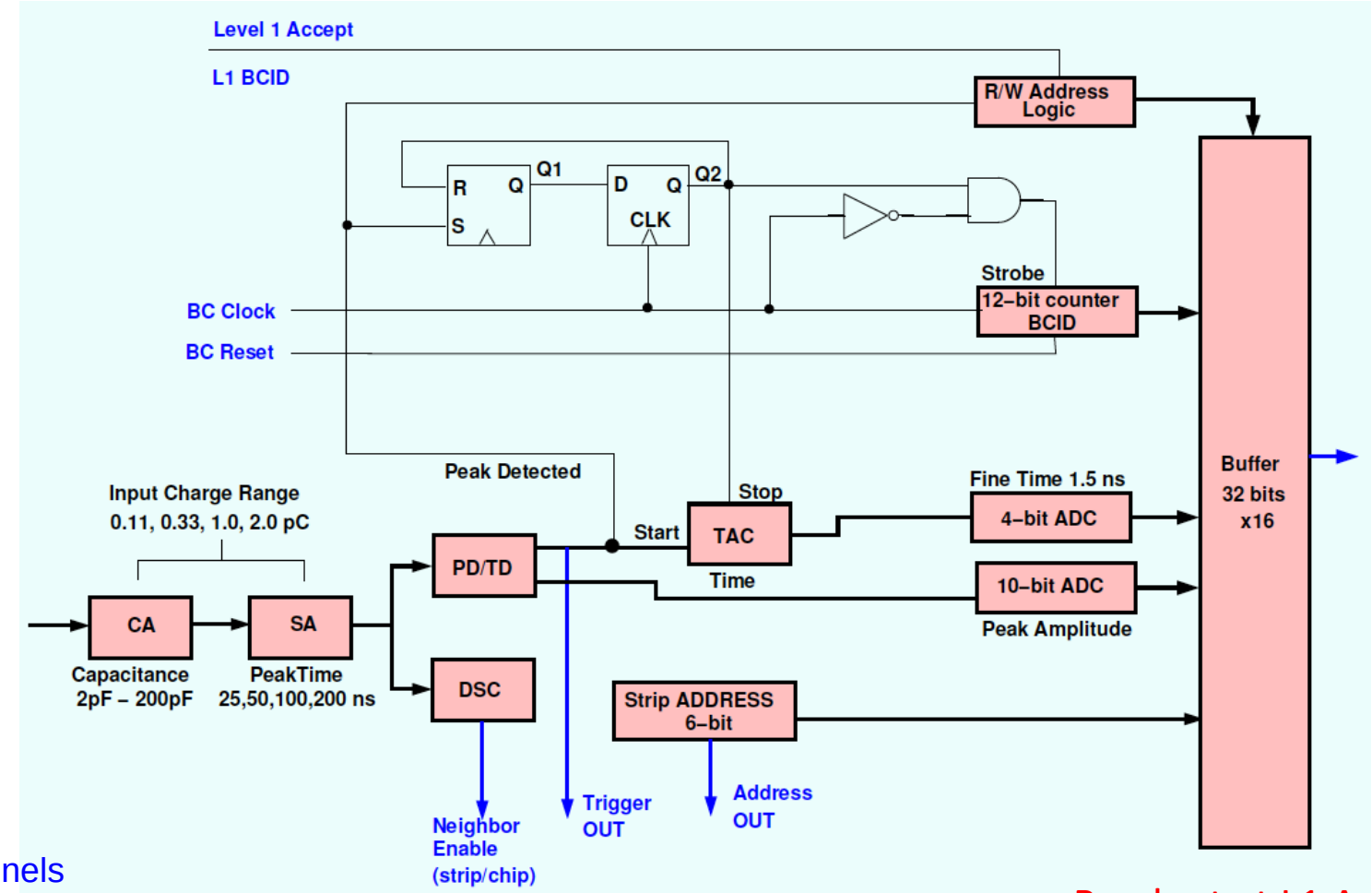


The Electronics Challenge

- The Small (~0.5 mm FWHM) charge footprint of the μMegas Detectors results in excellent position and double track resolution
- Results in a very large number of channels (order 10^6)
- Two Functions of the Readout:
  - Provide Precision measurement of charge and time at Trigger Level 1 accept
  - Provide in real time vector with ~1 mrad resolution to assist Trigger Level 1

- First task relatively easy to accomplish by highly multiplexed, data driven system
- Custom front end ASIC being under development

Block Diagram of the IC being designed



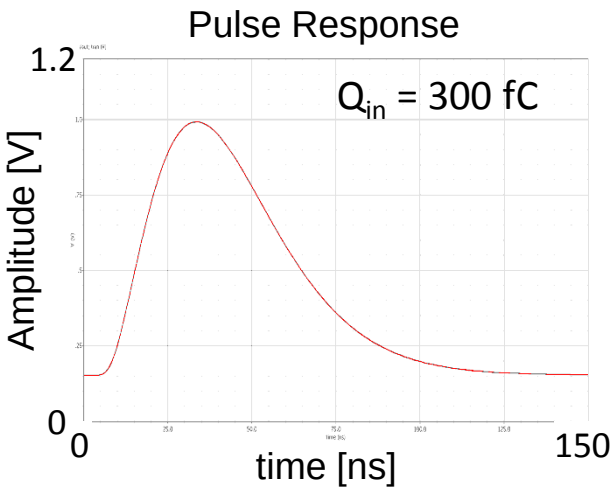
To SRS

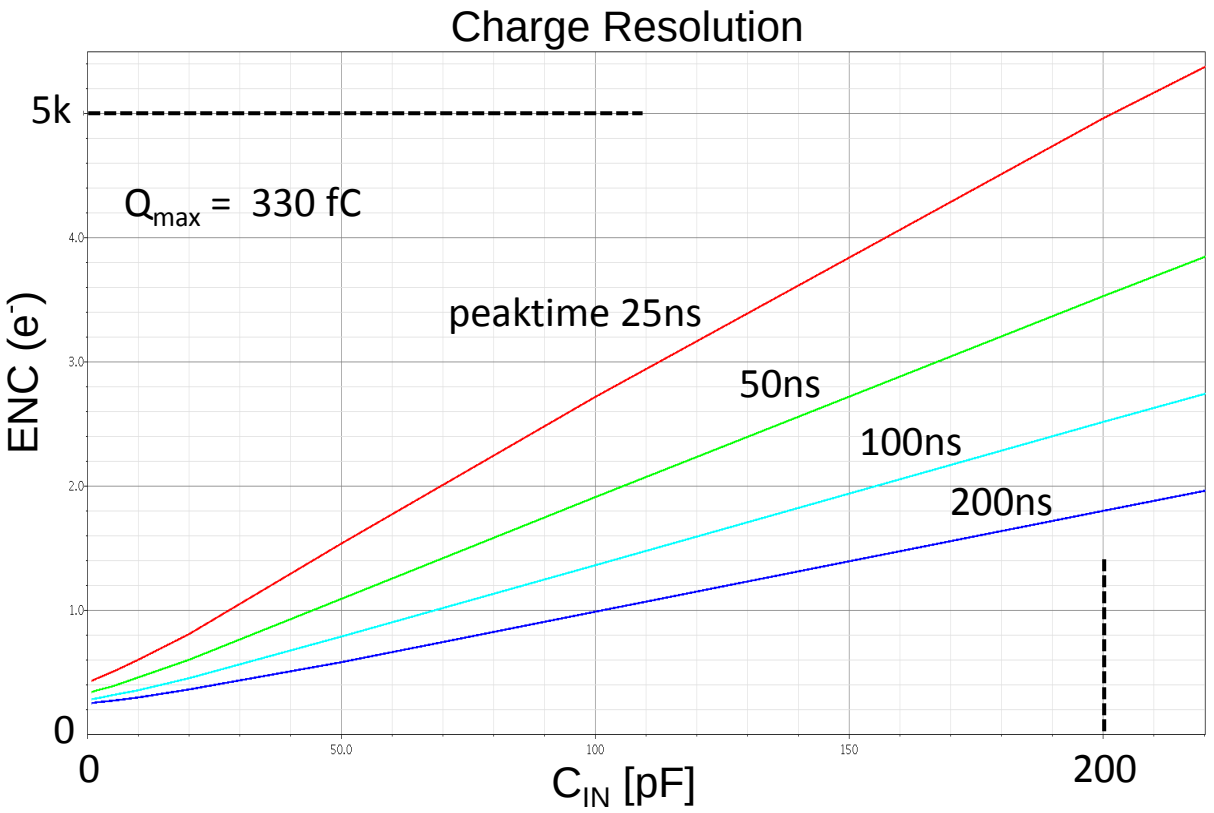
- 64 channels
- adj. polarity, adj. gain (0.11 to 2 pC), adj. peaking time (25-200 ns)
- derandomizing peak detection (10-bit) and time detection (1.5 ns)
- real-time event peak trigger and address
- integrated threshold with trimming, sub-threshold neighbor acquisition
- integrated pulse generator and calibration circuits
- analog monitor, channel mask, temperature sensor
- continuous measurement and readout, derandomizing FIFO
- few mW per channel, chip-to-chip (neighbor) communication, LVDS interface

Readout at L1 Accept
No Problem
Zero-suppressed, already digitized, much of DAQ already on Front End IC

VMM1 IC SPICE Simulation performance

Analog section:
transistor-level simulations
power ≈ 4 mW





BUT, How about Trigger?
Need to process in Parallel at 40 MHz

How can we take advantage of the 0.5 mm strip pitch?

Assume that we use ONLY one hit (the strip with the first arriving signal above a set threshold) from each 64-channel chip at each bunch crossing

This way:

- We have a trigger system with granularity of 3.2 cm (64 channels x 0.5 mm) BUT
- With spatial resolution ~ 0.5 mm
- We now have to deal with ~30,000 channels and not 2 million

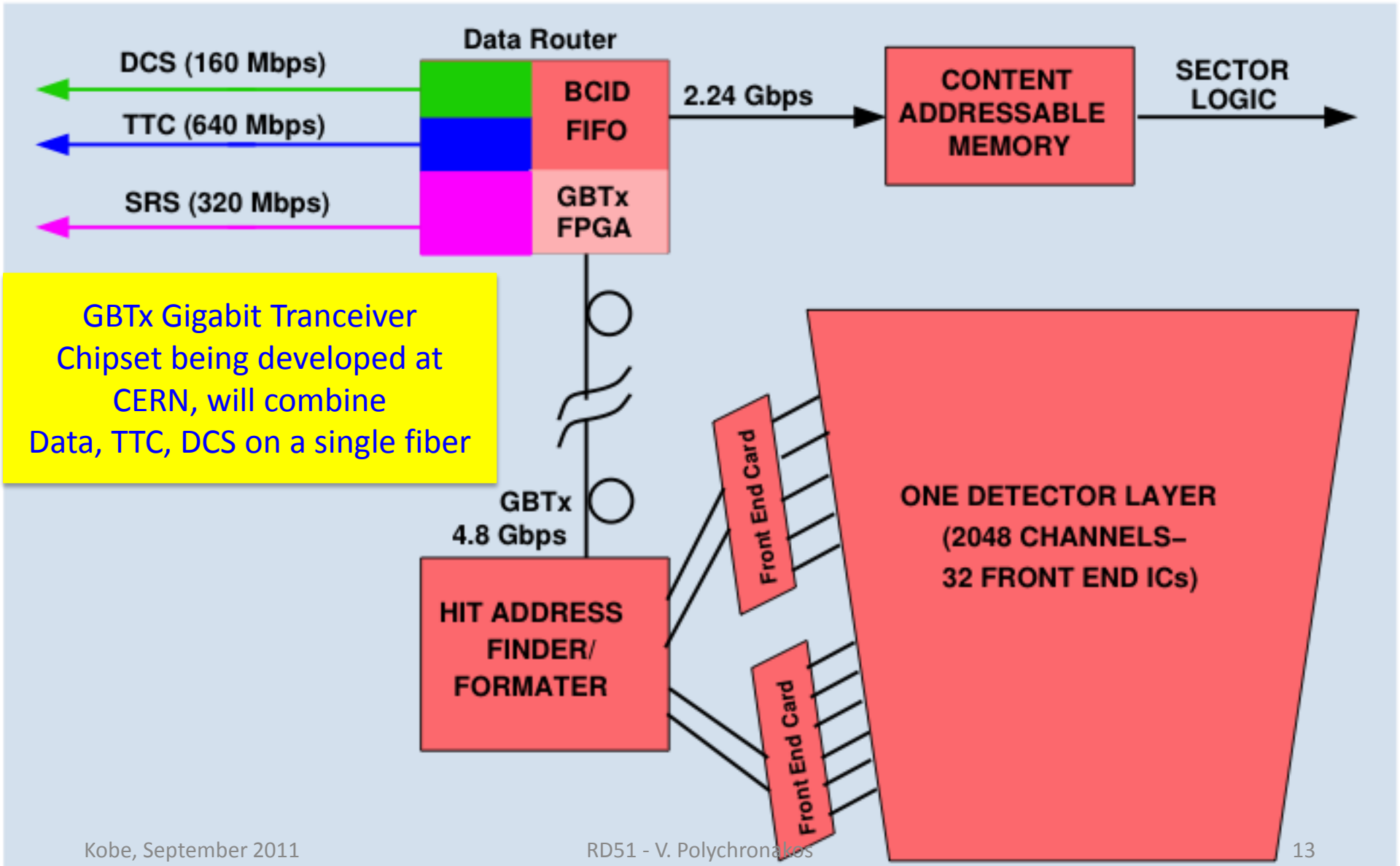
But are we paying a price for this? i.e. efficiency loss?

Consider worst case at η= 2.4:
Rate r = 10 kHz/cm^2, strip length l = 50 cm, strip width w = 0.5 mm

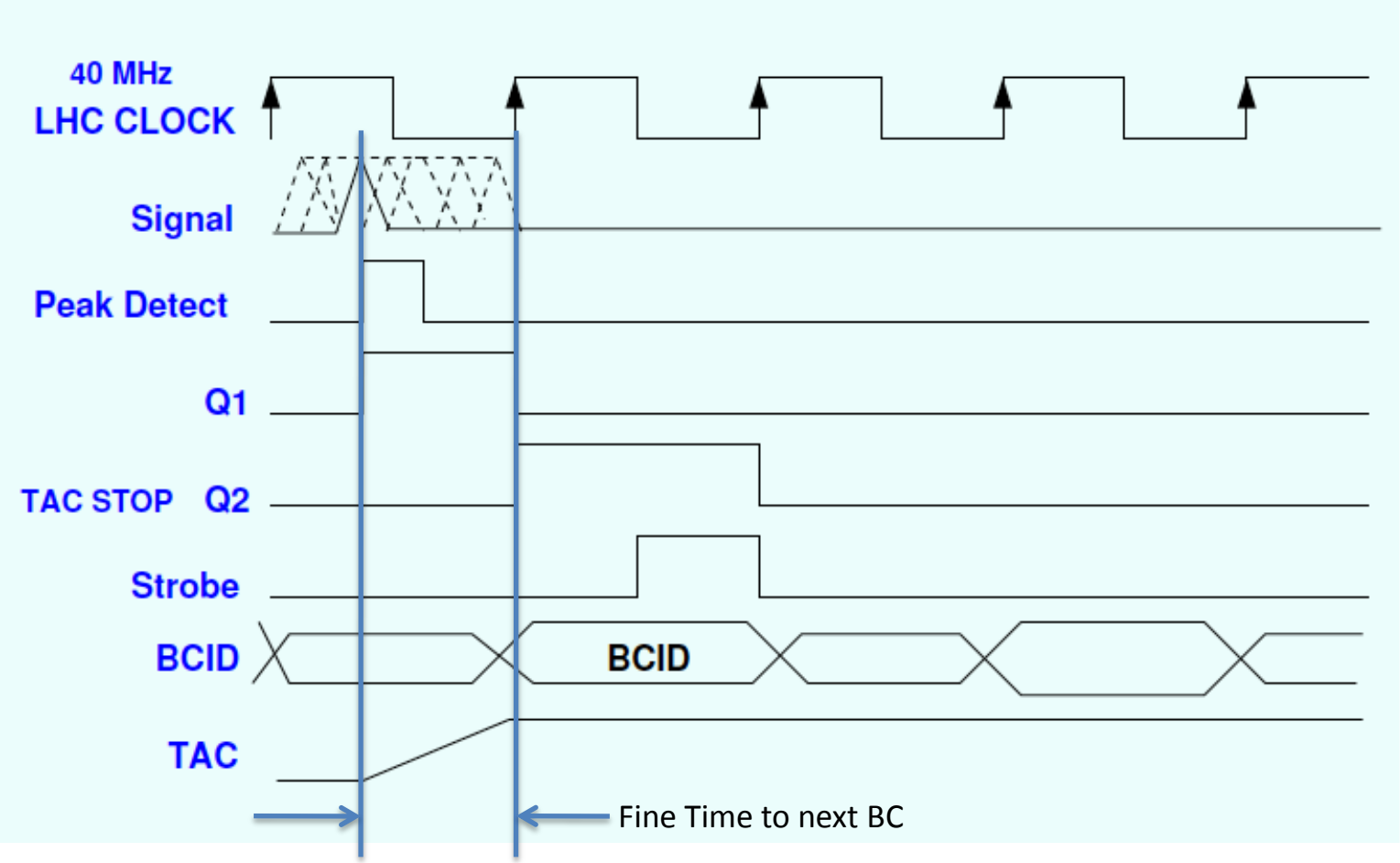
Occupancy/BC = rlwt = 6.25x10^{-4}

	Probability per Front End IC [%]		
# Hits	Probability per Chip per Bunch Crossing	Probability per Chip per 3 Bunch Crossings	Probability per Chip per 5 Bunch Crossings
0	96.1	88.7	81.9
1	3.8	10.6	16.5
>=2	0.1	0.6	1.6

Trigger/DAQ Block Diagram



Timing Diagram



40 MHz BC clock convenient for LHC but any clock can be used to related hit with trigger accept

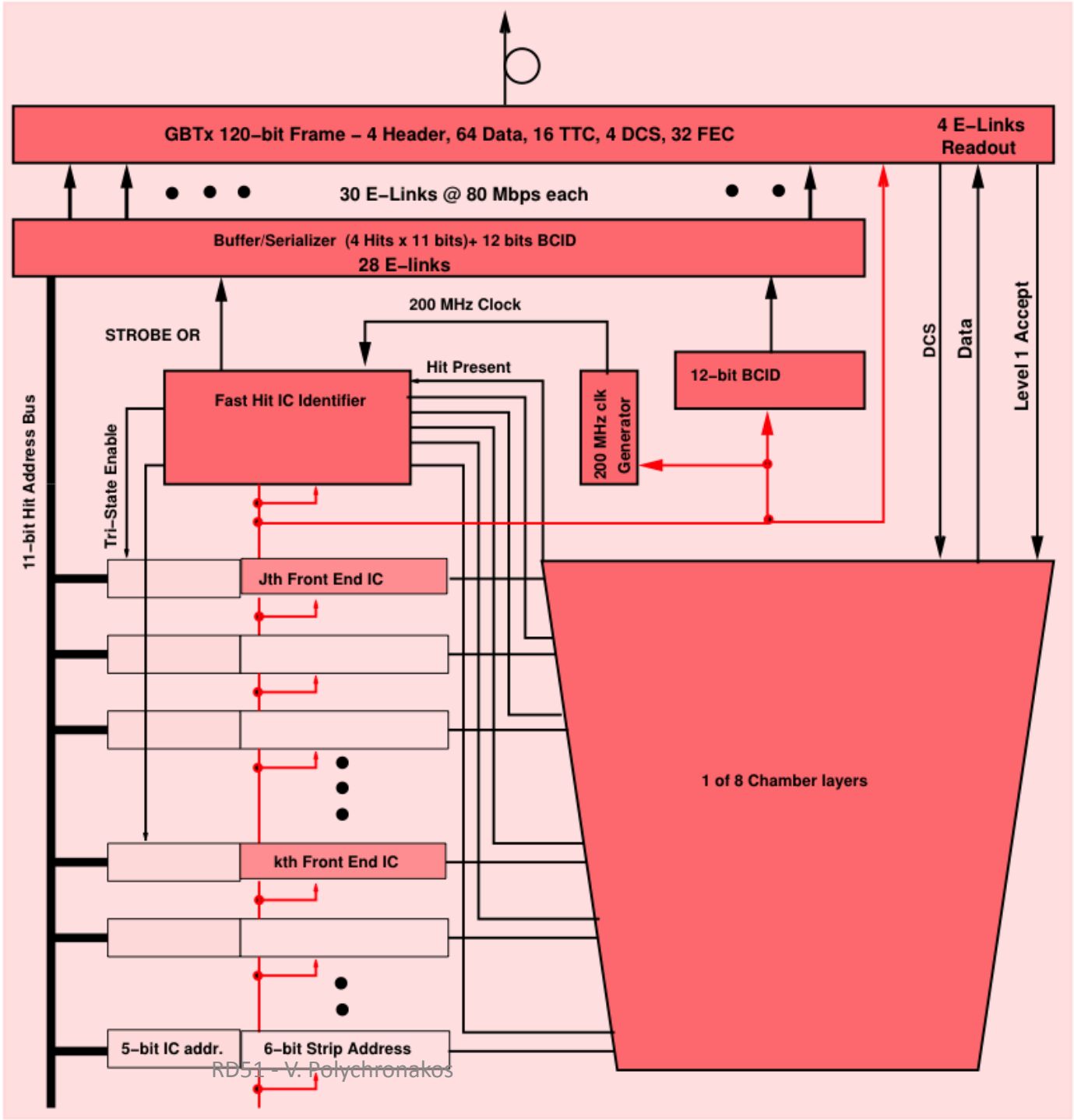
On-Detector Card

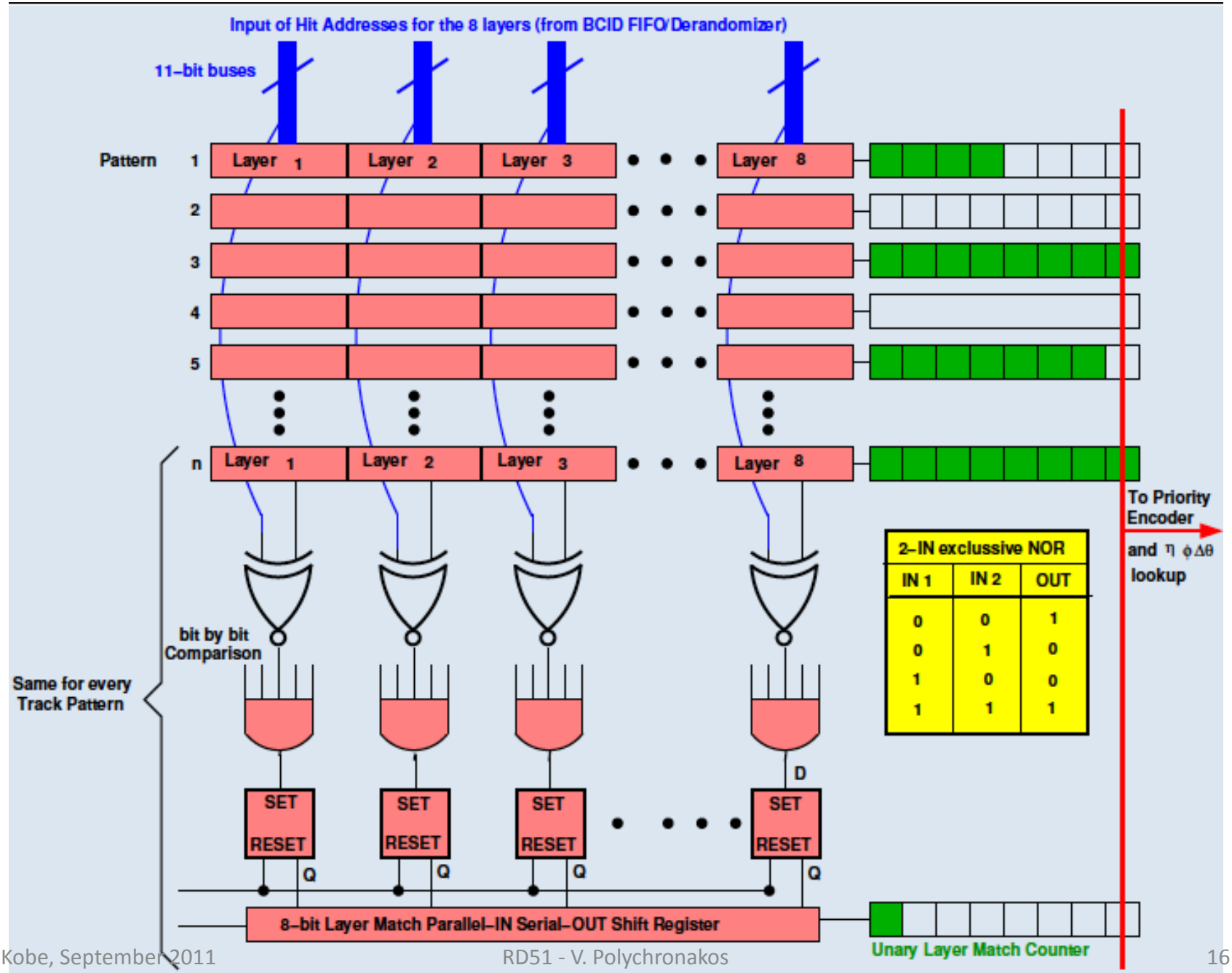
6 bit prompt strip address

5 bit IC address per plane

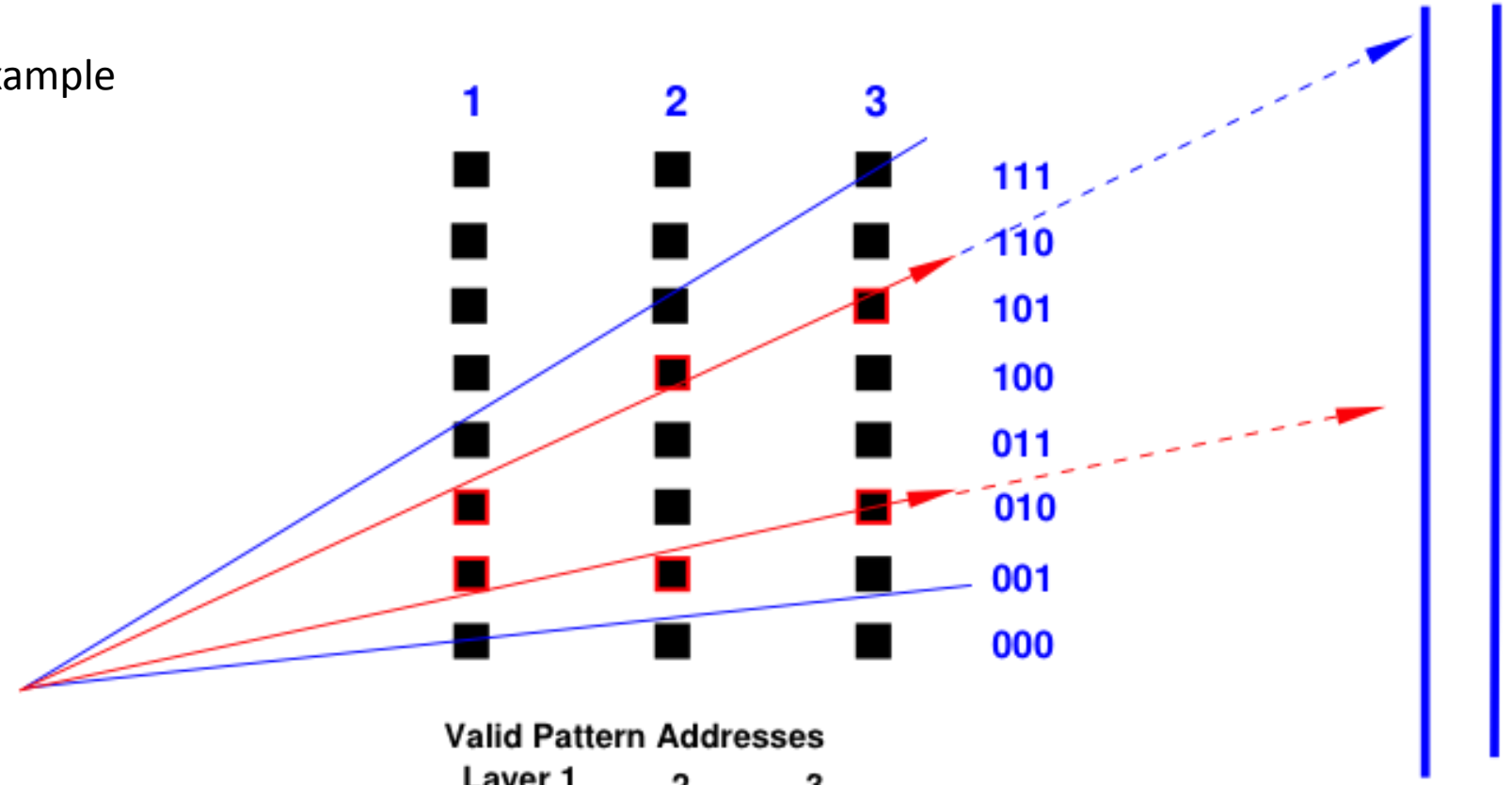
Up to 4 hits per plane transferred in 2 BC

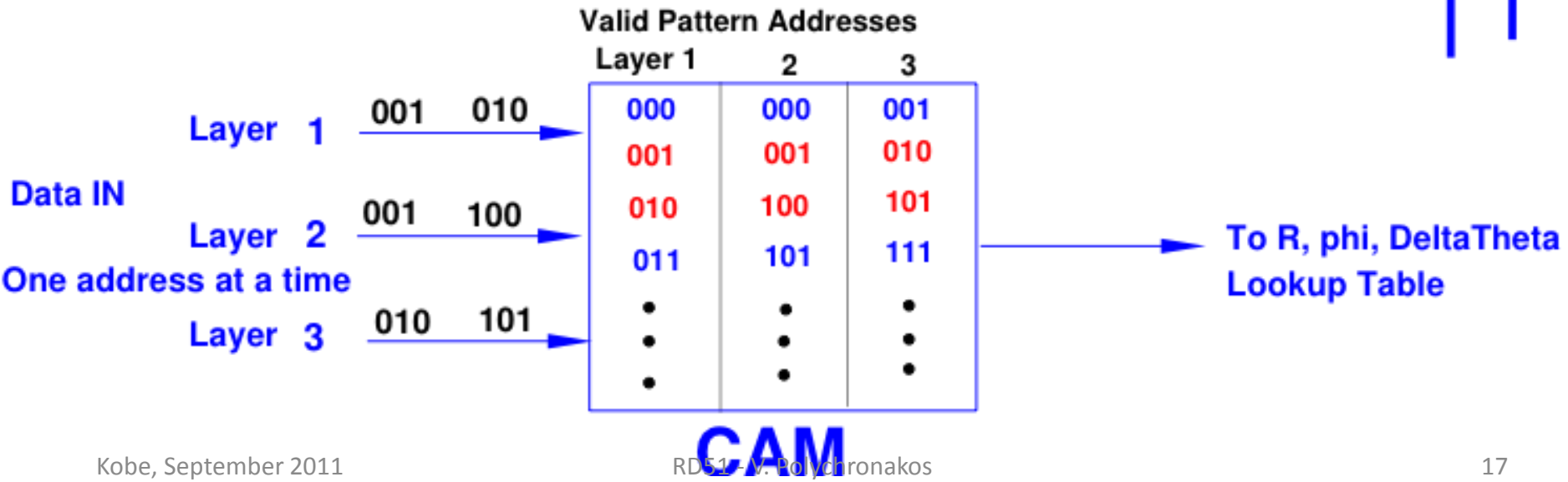
A Custom Digital IC the likely implementation




Input of Hit Addresses for the 8 layers (from BCID FIFO/Derandomizer)
11–bit buses
Pattern
1
2
3
4
5
n
Layer 1
Layer 2
Layer 3
Layer 8
To Priority Encoder
and η φ Δθ lookup
2–IN exclussive NOR
IN 1
IN 2
OUT
0 0 1
0 1 0
1 0 0
1 1 1
bit by bit Comparison
Same for every Track Pattern
D
SET
RESET
Q
8–bit Layer Match Parallel–IN Serial–OUT Shift Register
Unary Layer Match Counter
Matched Patterns

An Example

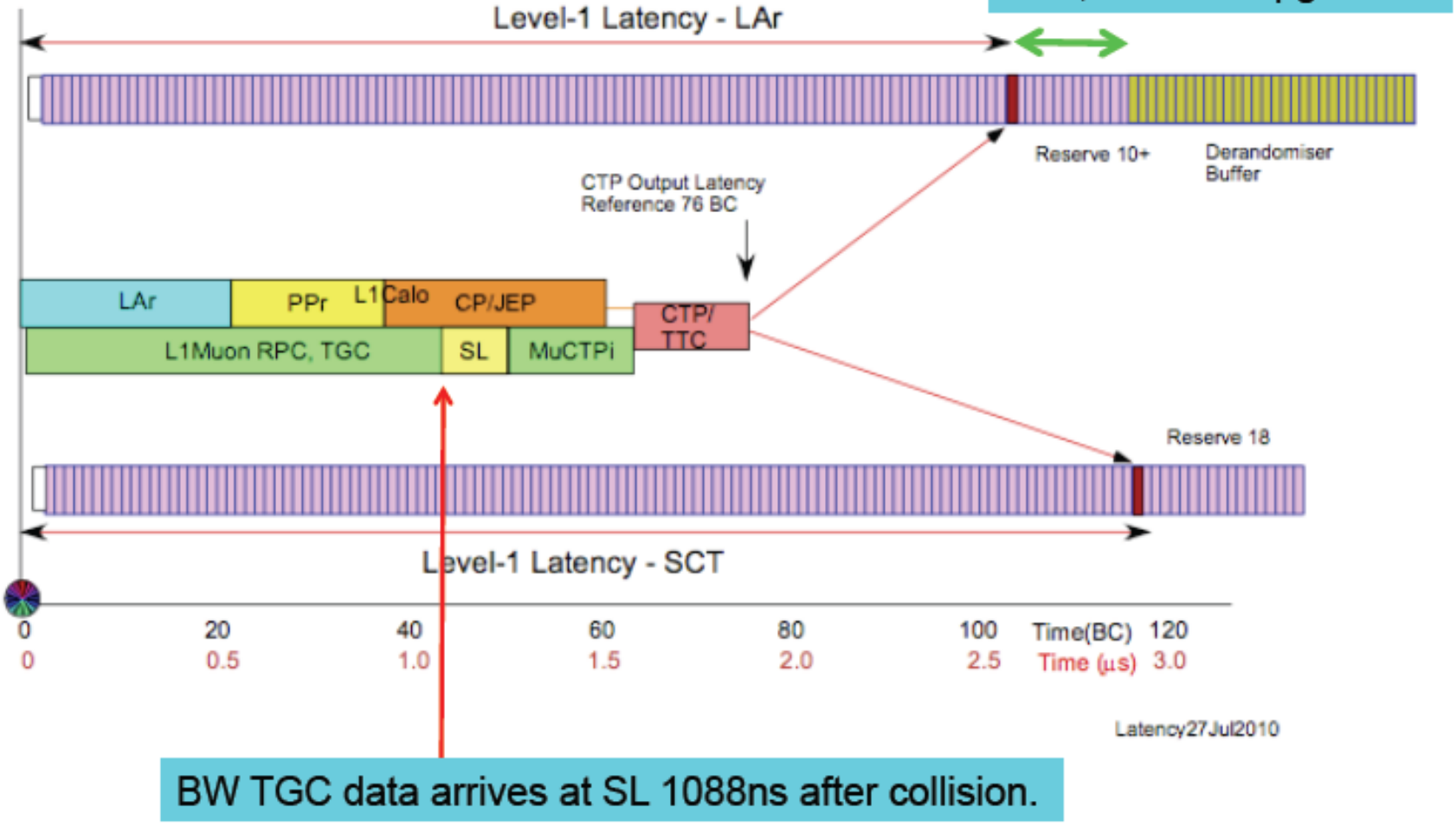

1
2
3
111
110
101
100
011
010
001
000


Valid Pattern Addresses
Layer 1
2
3
Layer 1
001 010
Layer 2
001 100
Layer 3
010 101
Data IN
One address at a time
000 000 001
001 001 010
010 100 101
011 101 111
To R, phi, DeltaTheta
Lookup Table
CAM

L1 latency

Current L1 Latency

This margin is shared by muon upgrade, topo trig, CTP, MuCTPi upgrades



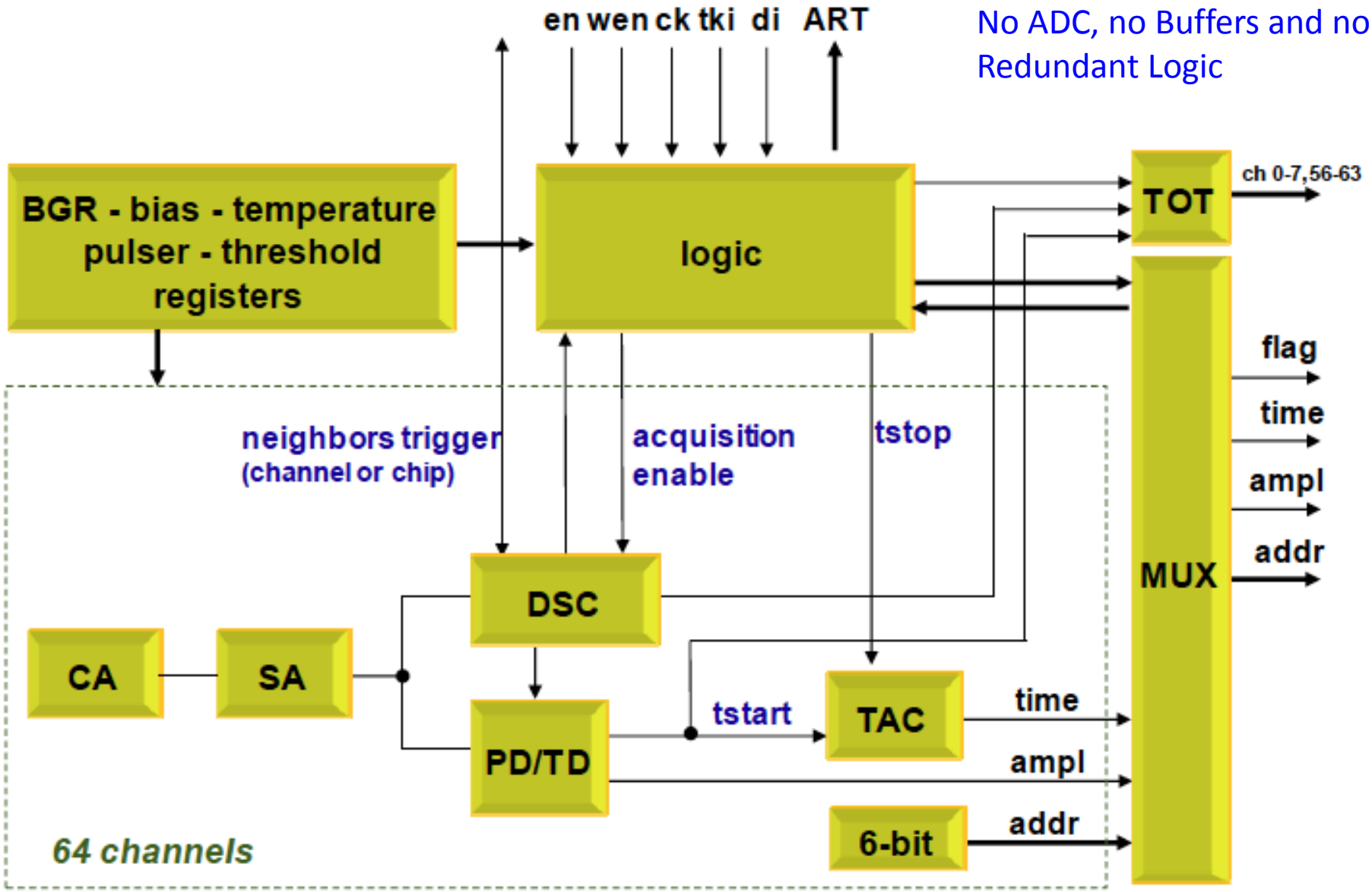
BW TGC data arrives at SL 1088ns after collision.

Time Required (BC)

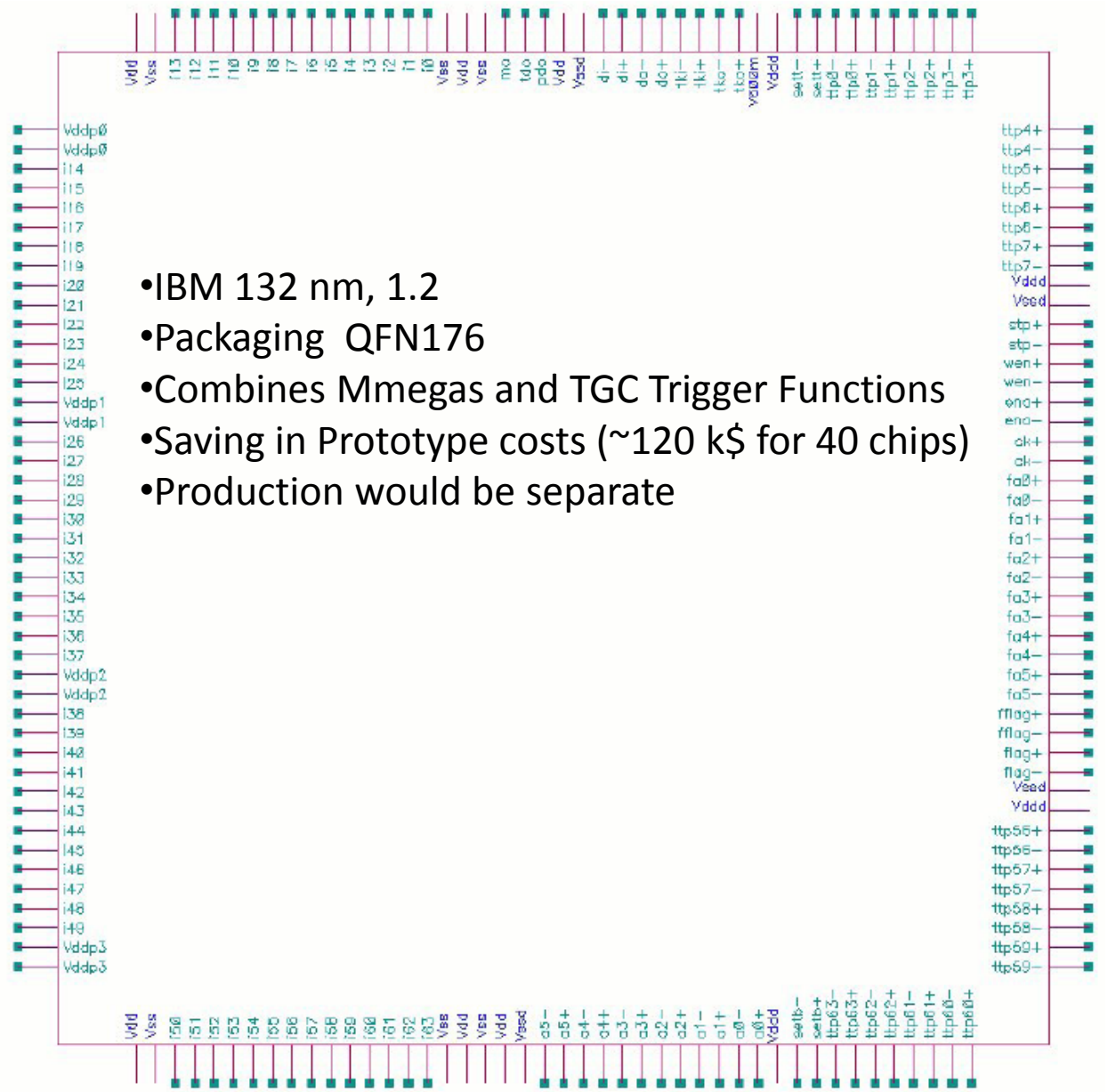
Muon TOF	1
Detector Response (drift time)	1
Front End Response (peaking time)	2 -- 3
Front End to GBTx	2
To USA15 (80 m fiber)	15
GBTx FPGA to CAM (up to 5 addresses per BCID)	1 – 2
CAM Read (160 MHz clock)	2 – 3
To Sector Logic	1 – 5*
Total	25 – 32

* Assumes that existing sector logic clocked @ 40 MHz

First Version of the front End IC



Layout of the Prototype ASIC

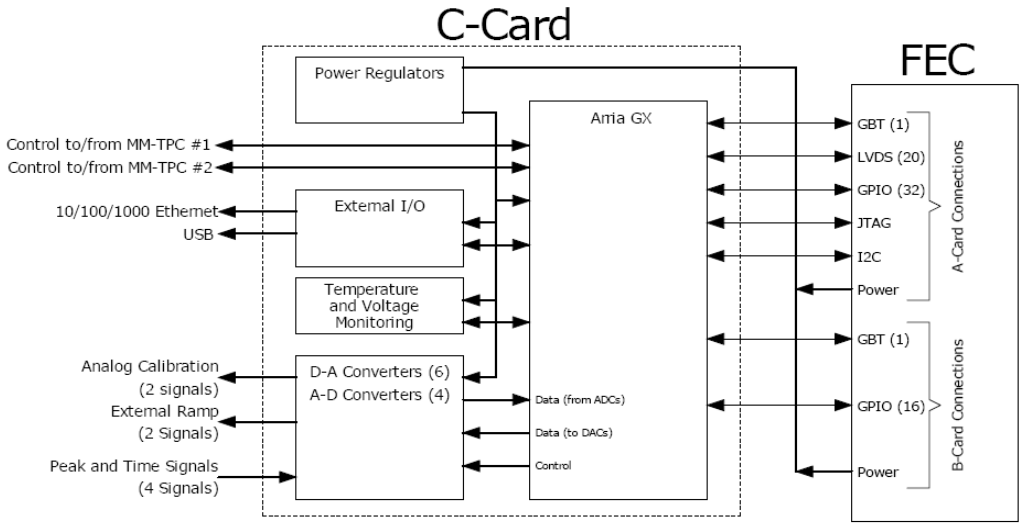


- IBM 132 nm, 1.2
- Packaging QFN176
- Combines Mmegas and TGC Trigger Functions
- Saving in Prototype costs (~120 k$ for 40 chips)
- Production would be separate

- **Main functionalities and settings**
  - global
    - temperature monitor
    - pulse generator (10-bit adjustable amplitude)
    - coarse threshold (10-bit adjustable)
    - self-reset option
    - analog monitor at *mo*
      - analog outputs, trimmed thresholds, (Band-Gap Reference) BGR, threshold, pulser amplitude , temperature sensor
    - high-drive analog buffers on *mo*, *pdo*, *tdo*
    - smart resets
  - analog section
    - charge amplification and high-order shaping
    - adjustable polarity (negative, positive)
    - gain: 0.5, 1, 3, 9 mV/fC (2, 1, 0.33, 0.11 pC)
    - peaktime: 25, 50, 100, 200 ns
    - test capacitor, channel mask
  - discriminator
    - trimmer (4-bit adjustable, 1mV)
    - sub-hysteresis processing
    - neighbor logic on channels and chips (ch0, ch63)

- peak detector
  - multi-phase
- time detector
  - TAC ramp (selectable 100ns or 200ns)
  - starts at peak-found
  - stop selectable (*ena*-low or *stp*-low)
- ART
  - address of the first event in real time
  - selectable at first threshold or at first peak
  - self-resets in 40ns
  - *fflag* indicates event
  - address available at *fa0-fa5*
- timing per channel
  - available for channels 0-7 and 56-63
  - selectable between time-over-threshold and time-to-peak
- readout
  - *flag* at first peak indicates events to readout
  - sparse with smart token passing (token skips empty channels)
  - amplitude available at *pdo*
  - timing available at *tdo*
  - address available at *a0-a5*
- interfaces
  - analog IOs ESD protected
  - digital IOs LVDS 600mV +/- 150mV
- analog monitors
  - analog outputs, trimmed thresholds, BGR, threshold, pulser, temperature sensor

Further Front End Card Development for prototype and future on-detector readout(U.Az)

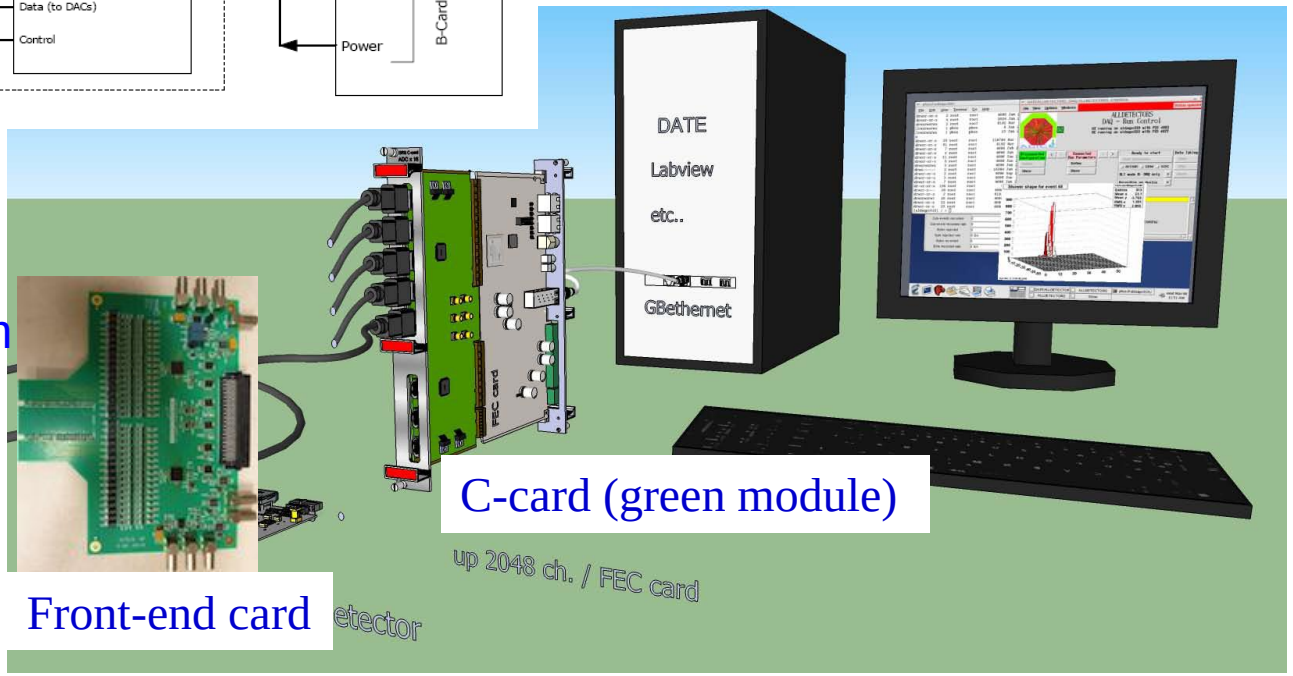


- Integration of BNL ASICs into
  - Development of so-called "C-card" for
    - BNL "LEGS TPC" ASIC
    - BNL new "MM TPC" ASIC
- Development of "small format" front-end card for CSC size Micromegas
- Development of complete front-end system for CSC size Micromegas

Scalable Readout System

SRS

Common Readout System developed for use by the RD51 collaboration for beam tests at CERN but not only



Summary

- Design of first prototype finished
- Has all Basic Functionality for both mMegas and TGC
- Layout to be done over the next month or two
- To be submitted for fabrication with MOSIS in November 2011
- Note: the first prototype won't implement the ADCs and the SEU circuitry.
- Work on front end boards started, to be tested early next year
- A second submission in about one year from now
- Preproduction and production to follow, estimate end of 2013 beginning 2014
- Schedule consistent with the overall Small Wheel schedule