Status of Chapter 4 – Detector Technical implementation

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THANKS!

- To all who have contributed to this chapter, who wrote sections, provided graphs, and helped shaping it!

Basic Structure of chapter 4

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Contents

1. Introduction

- Contains 2 parts:
  - Technical requirements
    - Outline the main technical aspects/changes/challenges (pixel size, readout rate, material budget, power consumption, L2 trigger, strip readout)
  - Environment and operating conditions
    - Radiation levels (e.g. effects on leakage current, ASICs technology node)
    - Operating temperature

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the thinner gate oxides. Recent measurements in 0.13 μm CMOS technologies suggest that ELT transistors may not longer be needed. Therefore the target technology nodes for the ALICE ITS upgrade are either 0.18 μm or 0.13 μm CMOS processes as will be described in subsection 4.2.1.

For hybrid pixel detectors the sensor is a separate silicon chip produced on high resistivity silicon. In the case of monolithic silicon detectors the detection volume is implemented in the readout chip itself, either as a layer of epitaxial silicon of defined thickness or as the bulk material on which the readout circuitry is produced. In general the radiation induced damage to the silicon lattice will lead to a macroscopic degradation of the sensor characteristics. This manifests itself as an increase in leakage current, a change in depletion voltage in case of a depleted operation and in trapping of the signal charge [?].

The leakage current will increase proportionally to the 1 MeV n equivalent fluence [?]. Given the values reported in table 4.2 the expected increase in leakage current is summarized for a set of configurations in following table.

Pixel layer	pixel size (rϕ × z) × thickness [μm^3]	I [A]
Pixel 0 (r=22 mm)	(20 × 20) × 50	16×10^{-12}
Pixel 0 (r=22 mm)	(30 × 30) × 100	72×10^{-12}
Strip layer	**strip width × length × thickness [μm^3]**	**I [A]**
Strip 0 (r= 235 mm)	50 × 20000 × 300	2.5×10^{-9}

Table 4.3: Leakage current increase due to radiation induced damage at room temperature. Damage constant α=4×10^{-17} A/cm.

Given the current radiation level estimations, it is possible to operate the ITS in a well-controlled temperature regime around room temperature (e.g. 20°C) with humidity control. A detailed description of the cooling system is discussed in chapter ??.

The choice of technology has to be compatible with several years operation in the ALICE experiment. Details on access scenarios and eventual interventions are discussed in chapter 5.

2. Technology Options for Pixels

- Contains 3 main parts:
  - 1.Technology node and architecture
    - Shortly presents 0.13 um and 0.18 um CMOS technology
  - 2. Overview of different technical implementations
    - Hybrid
    - Monolithic
  - 3. Module and interconnection

2. Overview of different technical implementations

- Starts with a review of the different concepts (hybrid, monolithic; readout schemes, process influence, new developments)
- Discusses the main technical challenges for the upgrade: spatial resolution, material budget, power management, radiation resistance
- The discussion is summarized in a schematic table.

in the sensor (Q) and the corresponding parasitic capacitance (C). For a 100 μm thick sensor the charge generated by a minimum ionizing particle (MIP) is approximately 8000 e-h pairs, while the parasitic capacitance is in the order of 30 fF. Thus the resulting Q/C is about 50 mV. In the case of monolithic detectors with a epitaxial layer thickness of 15 μm and a capacitance of 3-5 fF, the Q/C amounts to 40-60 mV. Monolithic pixels with a depletion layer of the order of 50 μm would yield a Q/C ratio in the 200-300 mV range. Therefore they could offer a very favorable analogue power figure. For this reason and for its potential radiation hardness due to the charge collection by drift, the approach pursued by LEPIX is considered of significant interest even though it is yet in a very early phase of development.

Table 4.4 summarizes the main features of the technologies considered for the ALICE ITS upgrade.

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	Hybrid Pixels	Mon. Pixels (MAPS)	Mon. Pixels (LePix)
Maturity	++	+	-
Pixel size	+	++	+
Material budget	-	++	++
SNR	++	+	++
L1 trigger	+	-	+
Timestamp	+	-	+
Cost/cm^2	-	++	+
Radiation hardness	++	+	+

Table 4.4: Key parameters for different pixel technologies under consideration for the ALICE ITS upgrade.

Hybrid Pixels

- Short review of target thicknesses and comparison with current detectors
- 3 parts
  - Sensor
    - effects on radiation; challenge of thin sensor production: epitaxial approach or carrier wafer approach; edgeless layout
    - results from epitaxial prototypes last year and outlook for run at VTT this year for 100 um edgeless sensors.
  - Frontend Chips
    - Reference to experience in the past, possible architecture
  - Bump bonding and TSV

4.2.2.1 Hybrid Pixel Detectors

A very lightweight design has to be achieved with minimum material budget in order not to degrade the resolution by multiple scattering. Hybrid pixel detectors consist of a front-end ASIC and a silicon pixel sensor. Therefore, to minimize the material budget both components have to be as thin as possible. The following table summarizes the current values used in LHC experiments and the target values for material budget contribution for a hybrid pixel detector in an upgraded ITS. In order to achieve the material budget limitations of 0.5% X_0 per layer the target thickness of the front-end ASIC and the sensor is set to 50 μm and 100 μm, respectively. A traversing MIP will thus produce about 8000 electron-hole pairs in the sensor.

	ASIC thickness [μm]	Silicon sensor thickness [μm]
ALICE pixel	150	200
ALICE ITS upgrade	50	100
ATLAS pixel	180	250
CMS pixel	180	285

Table 4.5: Summary of thicknesses used in current LHC hybrid pixel detectors and target values for a hybrid pixel detector for the ALICE ITS upgrade.

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4.2.2.1.1 Sensor Technologies The use of thin silicon sensors, with thicknesses in the range of 100 μm will require novel developments in terms of processing. The technical challenges to be met with this respect are on one side the procurement of thin blank detector grade wafers and on the other side the processing of such thin wafers in the standard production lines.

On the other hand, the radiation environment expected for the innermost layers in ALICE is still relatively modest, compared to the pixel layers of ATLAS and CMS. The

Assuming a duration of 200 ns for the calibration-comparison phase a bias current of 1 uA, a power supply of 1.5 V and a trigger rate of 10 kHz, the discriminator average power consumption would be only 2 nW. In this case, the average current per cm^2 would be 200 μA A capacitor of 1 μF per cm^2 reserved to the comparator power supply would be sufficient to guarantee a voltage drop of less than 20 mV during a single read-out cycle.

It is nevertheless clear that simultaneous enabling of all the discriminators will pose challenges to the design of the on-chip power supply network that should not be underestimated. Very careful analysis and prototyping would be needed before such an approach can be adopted as baseline.

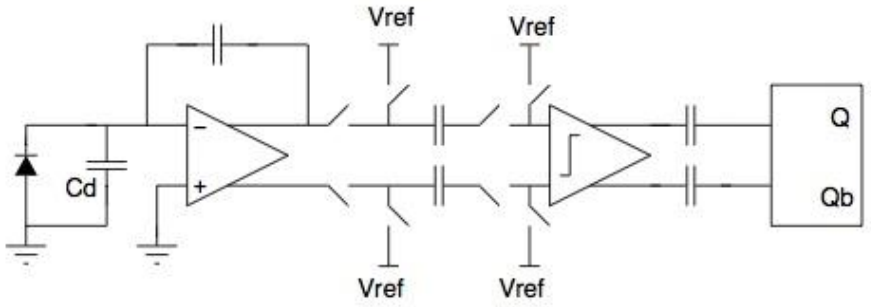

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Figure 4.4: Simplified schematic of a pixel cell with dynamic comparator

4.2.2.1.5 Development strategy There is a lot of expertise in the HEP community in the design of front-end for hybrid pixel detectors. Furthermore, several architectural concepts which are specific of the ALICE ITS could be already investigated in the R&D program for the monolithic sensors with sparsified read-out. Therefore, a dedicated prototyping phase for the front-end ASIC for hybrid pixel sensor will start only if this option will be selected. In this case, one would follow a two step approach. First, a reduced matrix is designed, incorporating all the building blocks and a smaller number of pixels. This chip could be produced at a reduced cost using MPW service and could be connected to a sensor for final validation. This approach has already been followed by the NA62 and PANDA collaborations. Techniques for the individual bump bonding of small dies to sensors have been successfully demonstrated. In the second step, a full size chip will be produced in a dedicated engineering run. While system level issues can only be studied with the final ASIC, the two-step approach will minimize the risk, since only silicon proven blocks will be employed in the full size chip.

4.2.2.1.6 Power supply requirement The maximum voltages allowed by the technologies is 1.5 V and 1.8 V for 0.13 μm and 0.18 μm CMOS processes, respectively. However, a new layout will have to be optimized and can try to minimize the actual

4.2.2.1.7 Through Silicon Vias Through Silicon Vias (TSV) offer the possibility to fan out the contacts for a chip to the back side of the ASIC instead of routing them to the wire bonding pads located on the edges of the die. Through Silicon Vias make therefore the connection between the front and back sides of the ASIC. A back side redistribution layer can be used to bring the electrical contacts to a matrix of contacts big enough to accommodate BGAs. In order to make TSV holes with a reasonable aspect ratio the readout wafers will be thinned to 2-3 times the diameter of the holes.

For a High Energy Physics vertex detectors the sensor will usually be of very thin Si material and the tile will be placed on a flexible low-mass substrate. Very basic screen printing of conductive glue can be used to connect the tiles to the low mass substrate. A potentially interesting aspect of this approach is that one could consider using a wide kapton foil supporting a 2D matrix of chips which could then be bent around a beam pipe with one 'pig-tail' for contact to each row of tiles.

First tests are being carried out together with the Medipix collaboration to evaluate a novel TSV approach. The test-wafers for this trial are Medipix 3 wafers and first prototypes are expected to be delivered in late 2011.

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4.2.2.1.8 Bump Bonding and ASIC Thinning Typical bump bonding diameters in current detectors are in the order of 25 μm. The most common material choices for the bump bond are eutectic Pb-Sn, Sn-Ag or Indium, depending on the vendor and the environmental requirements. In the present ALICE SPD bump bonds of eutectic Pb-Sn with a bump diameter of 25 μm have been used. The Pb-Sn bump is deposited on a Under Bump Metallisation (UBM) layer which provides the metallurgical connection to the Aluminum pad on the components and the wettable metal for the actual bump. The different metal layers are deposited in sputtering systems and electrolytic baths. Photolithographic steps are used to define the bump diameter. The minimum diameter of the bump defines also the possible pitch of the pixel. Current techniques are proven for pitches down to 50 μm and are believed to match still with pixel pitches of 30 μm. However, smaller pixel pitches will most likely require a change in bump technology. A first evaluation of the feasibility of making hybrid pixel detectors with a pitch of 30 μm is planned using dummy components.

To achieve the necessary thickness of the ASIC and the sensor, thinning steps have to be integrated into the bump processing. The handling and processing of very thin wafers requires the use of support wafers that are attached to the actual wafer. In the special case of epitaxial sensor wafers the support is provided by the Czochralski base material of the sensor, which is after processing thinned and metallized to provide the back plane contact. The stringent thickness requirements of 50 μm for the ASIC and 100 μm for the sensor unprecedented in other experiments necessitate a detailed study of the thinning steps in the process. A first trial using specially produced dummy components with the

Monolithic Pixels

- 3 different options presented
  - MISTRAL
  - INMAPS
  - LEPIX
- Each describing concept, architecture and prototyping plans

4.2.2.2.1 Monolithic CMOS sensors with Rolling-Shutter Read-Out The sensor developed for the ITS, called MISTRAL (standing for "**MI**MOSA **S**ensor for the **TR**acker of **AL**ICE"), will extend the low power, rolling shutter, architecture of the STAR device (see Figure 4.5) in order to increase its read-out speed by a factor of at least four and to improve its radiation tolerance by one order of magnitude. While the read-out speed improvement does not present any particular difficulty, the targeted radiation tolerance at room temperature imposes to switch to a smaller feature size fabrication process. The development of the MISTRAL chip will therefore incorporate the exploration of a 0.18 μm CMOS technology, which is significantly more powerful than the 0.35 μm process used for MIMOSA sensors up to now.

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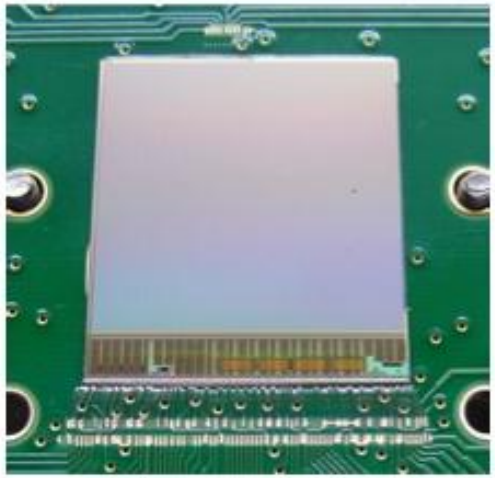

Figure 4.5: Picture of the ULTIMATE sensor.

4.2.2.2.2 Architecture With the rolling shutter architecture the charge collection inside a pixel is continuous, and the pixel matrix is read periodically row by row. This

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4.2.2.2.4 CMOS Sensors with Sparsified Readout In standard monolithic active pixel sensors (MAPS) (see Fig. 4.7 left) [?], the detecting element is formed by a reverse bias diode whose terminals are an nwell and the substrate. T he nwell acts as the collecting electrode and the diode capacitance converts the signal charge into a voltage, usually read-out with a source follower. In this approach only NMOS transistors can be located into the pixel. PMOS transistors, in fact, would need their own nwells, which would act as competing electrodes in the collection of the charge. One possibility to circumvent the problem consists in using a deep pwell placed underneath the PMOS nwells. The deep pwell "screens" these nwells, so that the charge is focused towards the collecting electrode. Shown in Fig. 4.7 right, this approach is called "INMAPS" or quadruple well. The possibility of embedding PMOS transistors close to the sensors makes it possible to design more conventional pixel cells with preamplifier-shaper-discriminator chains, as demonstrated in [?].

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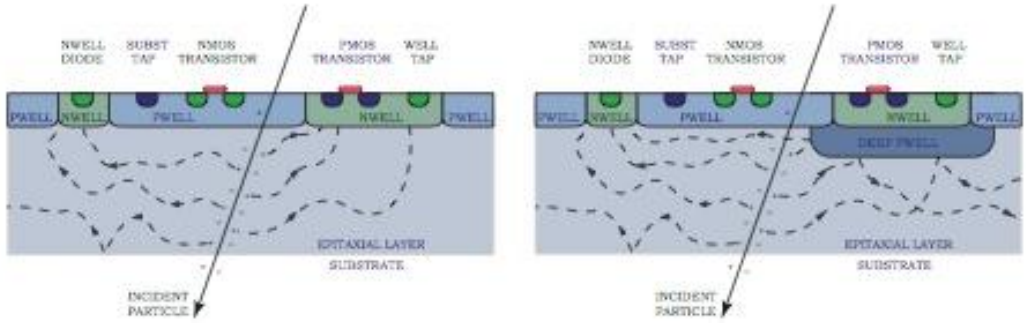

Figure 4.7: Standard monolithic approach (left) and quadruple well technology (right).

4.2.2.2.5 Architecture Using a quadruple well approach, one could develop an architecture identical to the one discussed in the hybrid pixel sensor section and shown in

4.2.2.2.7 Drift Based Monolithic Sensors in Very Deep Submicron CMOS The LePix project explores the possibility of fabricating monolithic CMOS sensors using deep submicron CMOS technologies ported on moderate to high resistivity wafers. In these devices, a relatively large depletion region (several tens of microns) could be reached with a moderate bias voltage (less than 100 V) and the charge will be collected by drift. This should minimize the impact of bulk damage due to non-ionizing radiation which still plagues standard monolithic sensors. The use of a drift field will help also in controlling the charge sharing among different pixels, and will also improve the speed of charge collection. Combined with a relatively thick depletion layer, this might allow the use of such devices also in applications in which particle identification is required. The LePix development will be therefore followed closely, since such kinds of sensors could be of great interest to ALICE if the technology reaches a sufficient maturity.

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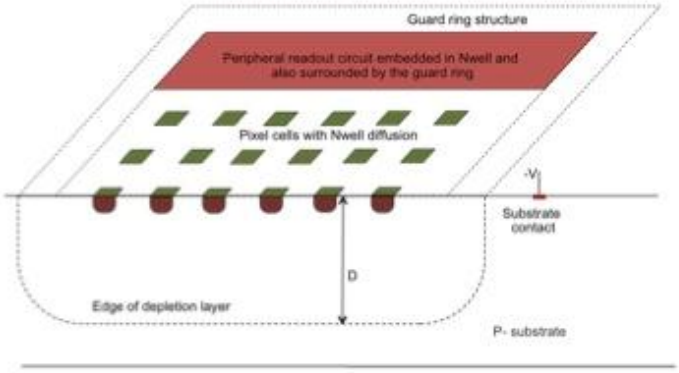

Figure 4.9: Schematic overview of the detector structure (see text).

4.2.2.2.8 Sensors principle The detector matrix (see 4.9) is formed by a two-dimensional array of Nwell diffusions into a P-type substrate of moderate resistivity (well above a few 100 Ωcm). Each of these Nwell diffusions forms the charge collection electrode of one pixel, and contains the local readout circuit for the pixel. The local readout circuit is connected to the periphery where the remainder of the readout circuit is located in an Nwell. The NMOS transistors are systematically placed in a Pwell inside the Nwell (use of triple well technology). Charge collection electrodes and readout circuit are biased near ground (a power supply of ≈1 V) with the P-type substrate negatively biased to several tens of Volt. To sustain the reverse substrate voltage readout circuit and detector matrix are surrounded by a guard ring structure. By applying a sufficient reverse substrate bias a bath-tub shaped depletion layer should be formed which is continuous underneath readout and detector matrix and ends near the outer edge of the guard ring and has a

3. Module and Interconnection

- Short discussion on the impact of the technologies used on the module design, reference to chapter 5

Strip Detectors

- Short introduction on the new conceptual design of the strip detector
  - Sensor layout:
    - advantages wrt to the present design
    - performance simulation
  - ASIC development:
    - general considerations and requirements
    - plans for on-chip ADC implementation
  - Interconnection development
    - microcable features and prototype production
  - Module assembly and interconnection tests

Readout electronics

- 2 parts:
  - On-detector electronics and detector links (e.g. GBT, etc.)
  - Off-detector electronics and interface to ALICE central systems (try to develop common parts for strips and pixels)

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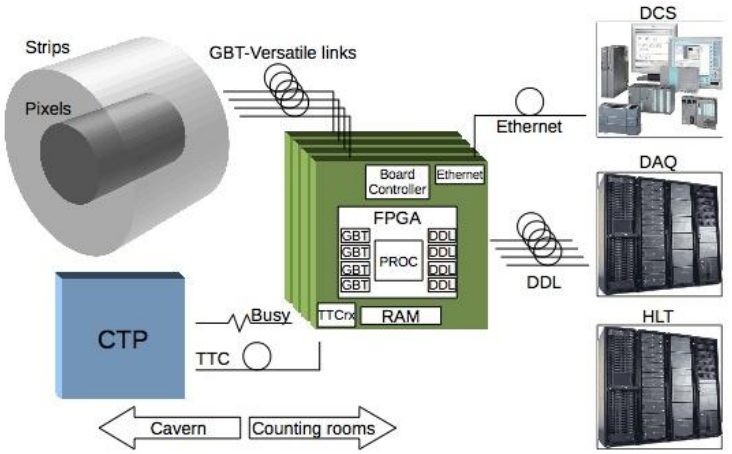

Figure 4.14: Illustration of a possible architecture for the upgraded ITS readout electronics.

4.3.1 Front-End Electronics Development

A new front-end chip for Silicon Strip Sensors will incorporate on board the analog to digital conversion, today performed outside the front-end ASIC. The ASIC will deliver to the back-end electronics digitized data serialized on a few high speed differential links. To accommodate more channel on chip, one could explore the use of commercial flip

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chip technologies as an alternative to standard wire bonding. The front-end chip will be designed in the same process (0.13 μm or 0.18 μm chosen for the pixel sensors. This will minimize the use of different technologies in the project and will favor expertise exchange and building block re-use among the different subsystems.

4.3.1.1 Requirements

The requirements for the front-end ASIC for the strips are reported in table 4.6

Table 4.6: FE requirements

ASIC spec	HAL25 (present SDD)	Upgrade chip
Input pitch	80μ	44μ
ASIC size	3.65 mm x 11.90 mm	6 mm x 6 mm
Noise (5 pF load)	300 e-	300 e-
Peaking time	1.4-2.2μs	1 - 2 μs
Power per channel	400μW	400μW
Total number of channel	128	128
Digitization	Off chip	On chip
Radiation level	30 krad	30 krad
Technology	CMOS 0.25 μm	CMOS 0.13 - 0.18μm

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Irradiation and Testbeam Plans

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- Short description of the irradiation plans: TID, NIEL
- Description of testbeam plans

4.5 Irradiation Plans

The radiation levels expected for the innermost layers of the future ALICE ITS will lead to radiation induce damage in the front-end electronics and the sensor parts as described in section 4.1.2.

Irradiation tests have started in 2011 and will be continued to investigate if the different technology options are sufficiently radiation resistant for the ALICE ITS upgrade. The tests are carried out to the respective radiation levels as described in table 4.2. A detailed annealing scenario is currently in preparation and will be based on the expected operating temperature (i.e. room temperature) and the foreseen accelerator operation schedule.

The irradiation tests can be distinguished in two groups: X-ray irradiation tests and hadron irradiation tests. While it is expected that the TID delivered during X-ray irradiation tests will lead to radiation induced damage mainly in the electronics parts, the non ionizing energy loss (NIEL) delivered by the hadrons will lead to lattice damage which manifests itself in the degradation of the sensor characteristics. Furthermore, during an

irradiation with charged hadrons (i.e. protons), there will be in addition TID effects. It is therefore necessary to carry out both types of irradiation tests to simulate the radiation environment in the ALICE experiment and to disentangle the radiation induced effects on the different components.

4.6 Testbeam Plans

The performance of the detector prototypes will be evaluated in dedicated beam test runs at the CERN SPS and PS. In addition to the electrical characterization and the irradiation measurements, the tracking performance of the detector prototypes being developed for the ITS upgrade will be evaluated by exposing them to minimum ionizing particle beams. The performance of monolithic and hybrid pixel as well as microstrip prototypes in terms of intrinsic point space accuracy, two track resolution and dE/dx capability will be evaluated and compared. We envisage also to study the detector performance in a